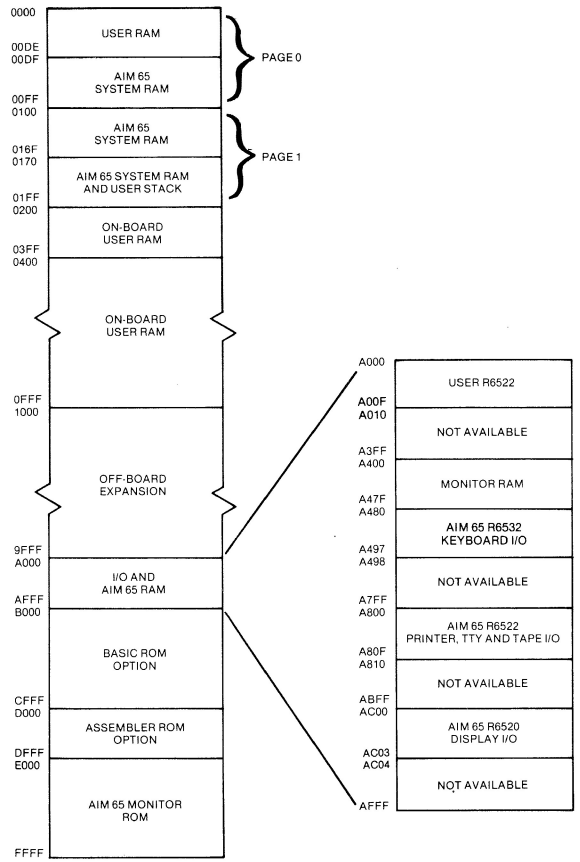
AIM 65 MEMORY MAP



AIM 65 USER-ALTERABLE ADDRESSES

Location	Name	Bytes	Description
0108	UIN	2	Vector to User Input Handler
010A	UOUT	2	Vector to User Output Handler
010C	KEYF1	3	JMP to User Function 1
010F	KEYF2	3	JMP to User Function 2
0112	KEYF3	3	JMP to User Function 3
A400	IRQV4	2	Vector to IRQ after Monitor Interrupt Routine
A402	NMIV2	2	Vector to NMI Interrupt Routine
A404	IRQV2	2	Vector to IRQ Interrupt Routine
A406	DILINK	2	Vector to Display Routine
A408	TSPEED	1	Audio Tape Speed Default = $C7 (AIM 65) Options = $5A (KIM-1 x 1) $5B (KIM-1 x 3)
A409	GAP	1	Audio Tape Gap Default = $08 = 32 SYN characters Option = $80 for Assembler input & Editor update

USER R6522 VERSATILE INTERFACE ADAPTER (VIA)

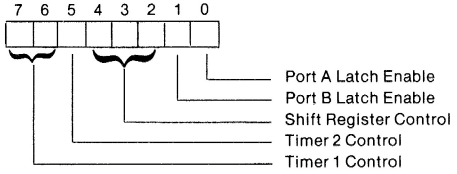
R6522 MEMORY ASSIGNMENTS

Location	Function
A000	Port B Output Data Register (ORB)
A001	Port A Output Data Register (ORA) **Controls handshake**
A002	Port B Data Direction Register (DDRB) } 0 = Input
A003	Port A Data Direction Register (DDRA) } 1 = Output

	Timer	R/$\overline{W}$ = L	R/$\overline{W}$ = H
A004	T1	Write T1L-L	Read T1C-L Clear T1 Interrupt Flag
A005	T1	Write T1L-H & T1C-H T1L-L → T1C-L Clear T1 Interrupt Flag	Read T1C-H
A006	T1	Write T1L-L	Read T1L-L
A007	T1	Write T1L-H Clear T1 Interrupt Flag	Read T1L-H
A008	T2	Write T2L-L	Read T2C-L Clear T2 Interrupt Flag
A009	T2	Write T2C-H T2L-L → T2C-L Clear T2 Interrupt Flag	Read T2C-H

A00A	Shift Register (SR)
A00B	Auxiliary Control Register (ACR)
A00C	Peripheral Control Register (PCR)
A00D	Interrupt Flag Register (IFR)
A00E	Interrupt Enable Register (IER)
A00F	Port A Output Data Register (ORA) *No effect on handshake*

R6522 AUXILIARY CONTROL REGISTER (ACR), LOC. $A00B



PORT A LATCH ENABLE

ACR0 = 1 Port A latch is enabled to latch input data when CA1 Interrupt Flag (IFR1) is set.
= 0 Port A latch is disabled, reflects current data on PA pins.

PORT B LATCH ENABLE

ACR1 = 1 Port B latch is enabled to latch the voltage on the pins for the input lines or the ORB contents for the output lines when CB1 Interrupt Flag (IFR4) is set.
= 0 Port B latch is disabled, reflects current data on PB pins.

SHIFT REGISTER CONTROL

ACR4	ACR3	ACR2	Mode
0	0	0	Shift Register Disabled.
0	0	1	Shift in under control of Timer 2.
0	1	0	Shift in under control of ø2.
0	1	1	Shift in under control of external clock.
1	0	0	Free-running output at rate determined by Timer 2.
1	0	1	Shift out under control of Timer 2.
1	1	0	Shift out under control of ø2.
1	1	1	Shift out under control of external clock.

TIMER 2 CONTROL

ACR5 = 0 T2 acts as an interval timer in the one-shot mode.
= 1 T2 counts a predetermined number of pulses on PB6.

TIMER 1 CONTROL

ACR7	ACR6	Mode
0	0	T1 one-shot mode — Generate a single time-out interrupt each time T1 is loaded. Output to PB7 disabled.
0	1	T1 free-running mode — Generate continuous interrupts. Output to PB7 disabled.
1	0	T1 one-shot mode — Generate a single time-out interrupt and an output pulse on PB7 each time T1 is loaded.
1	1	T1 free-running mode — Generate continuous interrupts and a square wave output on PB7.