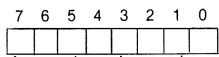


R6522 INTERRUPT REGISTER (PCR), LOC. \$A00C



CA1 Control
CA2 Control
CB1 Control
CB2 Control

CA1 CONTROL

PCR0 = 0 The CA1 Interrupt Flag (IFR1) will be set by a negative transition (high to low) on the CA1 pin.
= 1 The CA1 Interrupt Flag (IFR1) will be set by a positive transition (low to high) on the CA1 pin.

CA2 CONTROL

PCR3	PCR2	PCR1	Mode
0	0	0	CA2 negative edge interrupt (IFR0/ORC clear) mode — Set CA2 interrupt flag (IFR0) on a negative transition of the CA2 input signal. Clear IFR0 on a read or write of the ORC or by writing logic 1 into IFR0.
0	0	1	CA2 negative edge interrupt (IFR0 clear) mode — Set IFR0 on a negative transition of the CA2 input signal. Clear IFR0 by writing logic 1 into IFR0.
0	1	0	CA2 positive edge interrupt (IFR0/ORC clear) mode — Set CA2 interrupt flag (IFR0) on a positive transition of the CA2 input signal. Clear IFR0 on a read or write of the ORC or by writing logic 1 into IFR0.
0	1	1	CA2 positive edge interrupt (IFR0 clear) mode — Set IFR0 on a positive transition of the CA2 input signal. Clear IFR0 by writing logic 1 into IFR0.
1	0	0	CA2 handshake output mode — Set CA2 output low on a read or write of the Peripheral A Output Register. Reset CA2 high with an active transition on CA1.
1	0	1	CA2 pulse output mode — CA2 goes low for one cycle following a read or write of the Peripheral A Output Register.
1	1	0	CA2 low output mode — The CA2 output is held low in this mode.
1	1	1	CA2 high output mode — The CA2 output is held high in this mode.

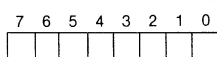
CB1 CONTROL

PCR4 = 0 The CB1 Interrupt Flag (IFR4) will be set by a negative transition (high to low) on the CB1 pin.
= 1 The CB1 Interrupt Flag (IFR4) will be set by a positive transition (low to high) on the CB1 pin.

CB2 CONTROL

PCR7	PCR6	PCR5	Mode
0	0	0	CB2 negative edge interrupt (IFR3/ORB clear) mode — Set CB2 interrupt flag (IFR3) on a negative transition of the CB2 input signal. Clear IFR3 on a read or write of the ORB or by writing logic 1 into IFR3.
0	0	1	CB2 negative edge interrupt (IFR3 clear) mode — Set IFR3 on a negative transition of the CB2 input signal. Clear IFR3 by writing logic 1 into IFR3.
0	1	0	CB2 positive edge interrupt (IFR3/ORB clear) mode — Set CB2 interrupt flag (IFR3) on a positive transition of the CB2 input signal. Clear IFR3 on a read or write of the ORB or by writing logic 1 into IFR3.
0	1	1	CB2 positive edge interrupt (IFR3 clear) mode — Set IFR3 on a positive transition of the CB2 input signal. Clear IFR3 by writing logic 1 into IFR3.
1	0	0	CB2 handshake output mode — Set CB2 output low on a write of the Peripheral B Output Register. Reset CB2 high with an active transition on CB1.
1	0	1	CB2 pulse output mode — CB2 goes low for one cycle following a read or write of the Peripheral B Output Register.
1	1	0	CB2 low output mode — The CB2 output is held low in this mode.
1	1	1	CB2 high output mode — The CB2 output is held high in this mode.

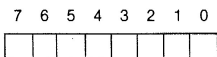
R6522 INTERRUPT FLAG REGISTER (IFR), LOC. \$A00D



CA2 Interrupt Flag
CA1 Interrupt Flag
SR Interrupt Flag
CB2 Interrupt Flag
CB1 Interrupt Flag
T2 Interrupt Flag
T1 Interrupt Flag
IRQ Has Occurred

IFR Bit	Set By	Cleared By
0	Active transition on CA2	Reading or writing the ORC (\$A001 or \$A00F)
1	Active transition on CA1	Reading or writing the ORC (\$A001 or \$A00F)
2	Completion of eight shifts	Reading or writing the SR (\$A00A)
3	Active transition on CB2	Reading or writing the ORB (\$A000)
4	Active transition on CB1	Reading or writing the ORB (\$A000)
5	Time-out of Timer 2	Reading T2C-L (\$A008) or writing T2C-H (\$A009)
6	Time-out of Timer 1	Reading T1C-L (\$A004) or writing T1L-H (\$A005 or \$A007)
7	Any IFR bit set with its corresponding IER bit also set	Clearing IFR0-IFR6 (\$A00D) or IER0-IER6 (\$A00E)

R6522 INTERRUPT ENABLE REGISTER (IER), LOC. \$A00E



CA2 Interrupt Enable
CA1 Interrupt Enable
SR Interrupt Enable
CB2 Interrupt Enable
CB1 Interrupt Enable
T2 Interrupt Enable
T1 Interrupt Enable
IER Set/Clear Control

INTERRUPT ENABLE BITS (IER0-6)

IER_n = 0 Disable interrupt
= 1 Enable interrupt

IER SET/CLEAR CONTROL (IER7)

IER7 = 0 For each data bus bit set to logic 1, clear corresponding IER bit
= 1 For each data bus bit set to logic 1, set corresponding IER bit.

Note: IER7 is active only when $R/\overline{W} = L$; when $R/\overline{W} = H$, IER7 will read logic 1.