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$Si_{1-x-y}Ge_xC_y$ Alloys: An Enabling Technology for Scaled High Performance Silicon-Based Heterojunction Devices

J.C. Sturm, C.L. Chang, M. Yang, and M.S. Carroll
Center for Photonics and Optoelectronic Materials (POEM)
Department of Electrical Engineering
Princeton University, Princeton, NJ 08544 USA
Tel: 609-258-5610, fax: 609-258-1954, sturm@ee.princeton.edu

$Si/Si_{1-x}Ge_x$ heterostructures have traditionally faced both fundamental and practical limitations in their applications of advanced device technology. These hurdles have been most significantly been the well-known critical thickness limitation for pseudomorphic growth, as well as the less-known sensitivity of devices to heterojunction process integration and the required thermal budget. In this talk, we will review how $Si_{1-x-y}Ge_xC_y$ alloys growth by rapid thermal chemical vapor deposition (RTCVD) are an enabling technology to overcome both these fundamental and practical issues, with application to both bipolar and sub-100-nm MOS devices.

Initial work on $Si_{1-x-y}Ge_xC_y$ alloys was focused on using carbon to reduce the compressive strain in pseudomorphic $Si_{1-x}Ge_x$ layers on Si(100) [1,2]. Work more recently has focused on determining the effect of C on bandgaps and more specifically band offsets, which are affected by both the chemical affect of the carbon as well as its effect on band position through its affect on strain. It now appears that while the intrinsic effect of adding C is to reduce the bandgap by ~20 meV/%C, the reduction of strain in compressively strained pseudomorphic $Si_{1-x-y}Ge_xC_y$ alloys as C is added increases the bandgap by ~40 meV/%C, with a net increase in bandgap of 20-25 meV/%C. This relatively slow rate of increase of bandgap as strain is reduced through the addition of carbon leads to higher critical thickness for a given bandgap for $Si_{1-x-y}Ge_xC_y$ compared to that for $Si_{1-x}Ge_x$. Further the bandgap for strain-free alloys lattice-matched to silicon is significantly less than that of silicon [3,4,5]. For example, for a bandgap 100 meV less than that of Si, the equilibrium critical thickness of a strained $Si_{0.87}Ge_{0.13}$ layer would be only ~ 25 nm, while that of a strained $Si_{0.83}Ge_{0.16}C_{0.01}$ layer, would have a critical thickness of ~70 nm. If the carbon fraction were increased to a level of 0.02, the critical thickness of the $Si_{0.79}Ge_{0.19}C_{0.02}$ layer would be nearly 1 micron [6]. In such strain-free alloys, band offsets predominantly in the valence band and not in the conduction band are expected. Both electrical and optical measurements will be shown to support these results [6].

For proper operation, many advanced devices depend of the placement of dopant atoms within a few nm with respect to a heterojunction. While structures with such resolution can be routinely grown in silicon-based materials by both MBE and CVD techniques at temperatures less than 700 °C, processing steps such as oxidation, anneals of ion implantation damage, etc., are typically required to integrate devices into existing VLSI processes. These steps can easily lead to dopant diffusion of 10 nm or more, even at temperatures of 750 °C or less, vastly degrading device performance. In many practical examples, this limitation on the thermal budget is far more severe than that for strain relaxation, and hence it is a major stumbling block towards the realization of large-scale circuits with silicon-based heterojunction devices. Over the last few years, it has been found that the diffusion of some dopants, especially boron, can be reduced by an order of magnitude or so (compared to pure Si or $Si_{1-x}Ge_x$) by the incorporation of only low levels of substitutional carbon to form $Si_{1-y}C_y$ or $Si_{1-x-y}Ge_xC_y$ alloys [7,8]. Even more interesting, it appears that the diffusion coefficient is reduced not only in the $Si_{1-x-y}Ge_xC_y$ layer itself, for example, but also in nearby regions of pure Si. While the exact mechanism is not well understood, it appears that substitutional C creates a sink for Si interstitials, which are required for the diffusion of dopant atoms such

as boron. By reducing the local interstitial concentration, diffusion coefficients can thus be reduced. In this way the $Si_{1-x-y}Ge_xC_y$ layer may be separated from a critical (with respect to diffusion) device region if desired. The efficiency of such layers in removing interstitials and their effect on diffusion-enhancement processes such as transient enhanced diffusion (TED) and oxidation-enhanced diffusion (TED) will be discussed [9].

Finally, the application of these layers to both bipolar and MOS devices will be discussed. In bipolar devices, the diffusion of dopant from the base layer is a critical problem in device integration due to the creation of parasitic barriers at base-emitter and base-collector interfaces. Under some processing conditions, device performance (especially output resistance) is greatly degraded already at temperatures as low as 750 °C. A diffusion length of only 5 nm is more than enough to lead to this effect. We will discuss how the application of $Si_{1-x-y}Ge_xC_y$ to the base region of the device can be engineered to overcome this problem without leading to other deleterious effects [8].

To scale MOSFET's far below 0.1 micron in channel length, vertical FET structures in which the source and drain are defined by a vertical profile (e.g. epitaxy) as opposed to the conventional lateral structure in which they are defined by photolithography are very attractive. This is especially true when thin Si pillars are considered for double-gated devices. While structures with channel length $L \ll 100$ nm can easily be grown by epitaxy, the diffusion of dopant during subsequent processing (e.g. sidewall gate oxidation) can limit the channel length to well over 100 nm in practice. We will show how the application of $Si_{1-x-y}Ge_xC_y$ layers can be used to realized vertical FET's with L as short as 40 nm [10], nearly an order of magnitude shorter than previous results for p-channel devices. The application of such layers to solve other critical CMOS integration problems will be discussed as well [11].

In summary, $Si_{1-x-y}Ge_xC_y$ layers are attractive for overcoming the longstanding critical thickness and dopant diffusion limitations which have severely limited the widespread application of the $Si/Si_{1-x}Ge_x$ material system to date. Besides their usual role in heterojunction bipolar transistors, this material system has potential applications to photonic devices and also ultra-short channel MOS transistor technology.

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