Integration of amorphous and polycrystalline silicon thin-film transistors through selective crystallization of amorphous silicon

K. Pangal,[a] J. C. Sturm, and S. Wagner
Department of Electrical Engineering, Princeton University, Princeton, New Jersey 08544

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Selective exposure of a hydrogenated amorphous silicon (*a*-Si:H) film to a room-temperature hydrogen plasma using a patterned masking layer and a subsequent anneal at 600 °C, results in patterned polycrystalline and amorphous silicon regions. However, most of the hydrogen in the amorphous silicon is lost, leading to severe degradation in its properties. In this letter, we report the rehydrogenation of amorphous silicon films following this anneal to give *a*-Si:H thin-film transistors with a mobility as high as 1.2 cm^2/V s and ON/OFF current ratios of $\sim 10^6$. This process was used to integrate amorphous and polycrystalline silicon transistors on a single substrate with only one more lithography and processing step than that required for a single type of transistor. © *1999 American Institute of Physics.* [S0003-6951(99)03340-9]

For large-area electronics, there has been considerable interest in integrating polycrystalline (polysilicon) and amorphous silicon (*a*-Si:H) thin-film transistors (TFTs). This can be done by selective laser crystallization of *a*-Si:H,[1] or by using two layers of silicon: one polycrystalline and the other amorphous,[2] both with the goal of integrating the *a*-Si:H and the poly-Si TFTs on the same substrate. In active-matrix flat panel displays, *a*-Si:H TFTs then can provide low leakage in the OFF state, and poly-Si TFTs can provide high drive currents. Integration of *a*-Si:H and poly-Si TFTs is difficult for three reasons. First, the conventional *a*-Si:H TFT fabrication process is a low temperature process (<350 °C),[3] while the poly-Si TFT fabrication requires a 500–600 °C anneal to form the polycrystalline layer, if laser processing is not used. Second, one would like to deposit only a single Si layer instead of two (*a*-Si:H and poly-Si) to save cost, and third, the structure and fabrication sequence of conventional *a*-Si:H TFTs and poly-Si TFTs are very different (bottom gate versus top gate process), so that few process steps can be shared.

In this letter we demonstrate a method for integrating such transistors together starting with a single Si layer, without laser processing. The work is based on the selective crystallization of selectively-masked *a*-Si:H to polysilicon by locally seeding the crystallization with a rf hydrogen plasma at room temperature, followed by a crystallization anneal at 600 °C. All fabrication steps for the two transistors are shared in a common top-gate process. The critical process described in this letter, which enables this result, is the rehydrogenation of the amorphous silicon after the ~600 °C anneal.

Hydrogenated amorphous silicon (*a*-Si:H) films of 150 nm thickness were deposited by plasma-enhanced chemical vapor deposition (PECVD) using pure silane, on Corning 1737 glass substrates at a substrate temperature of 150 °C and rf power of ~0.02 W/cm^2. We used 150 °C instead of the usual 250 °C[3] to raise the higher hydrogen content of the *a*-Si:H to 15 at. %, which facilitates the subsequent selective crystallization.[4–6]

Exposing *a*-Si:H to a room-temperature hydrogen plasma before a 600 °C anneal reduces the time taken to crystallize the amorphous film to 4 h from ~20 h by creating silicon crystal nuclei, which acts as seeds for grain growth during subsequent annealing.[4,7] The principle of area-selective crystallization is to protect selected areas of the *a*-Si:H precursor film from the plasma exposure by masking,[4,7–9] so that subsequent 600 °C anneal converts only the seeded areas to polycrystalline silicon. A 120 nm thick SiN_x mask film was deposited by PECVD and patterned by wet etching. Then the sample was exposed to the hydrogen plasma for seed nucleation in a parallel plate reactive ion etcher at room temperature at 0.8 W/cm^2, 50 mTorr, for 60 min. The crystallization anneal was then done at 600 °C in N_2. After ~4 h of anneal at 600 °C the portion of the *a*-Si:H film that had been exposed to the hydrogen plasma was completely crystallized (confirmed by UV reflectance measurement[8]), while the unexposed regions were still amorphous. The SiN_x capping layer was then removed by etching in dilute HF. Thus both amorphous and polycrystalline silicon were obtained in a single silicon layer.

A critical issue for the fabrication of *a*-Si:H devices in such a process is the loss of hydrogen from the amorphous regions during the ~600 °C anneal. To measure the hydrogen content, 250 nm *a*-Si:H was deposited on SiO_2/Si substrates (Si to allow infrared transmission spectroscopy measurement and thin 200 nm SiO_2 to prevent substrate interaction during the anneal). The atomic hydrogen content in the films was deduced from the integrated absorption near 630 cm^{-1}, which is due to the Si–H and Si–H_2 wagging modes,[10] using[11]

$$C_H[\text{at. \%}] = \frac{2.1\times 10^{19}\ \text{cm}^{-2}}{5\times 10^{22}\ \text{cm}^{-3}} \int \frac{\alpha(\omega)}{\omega} d\omega.$$

The atomic hydrogen content in the as-grown *a*-Si:H was ~15 at. %, which after annealing at 600 °C for 4 h had dropped to about ~0.3 at. %. A similar loss of hydrogen is

[a]Electronic mail: kpangal@ee.princeton.edu

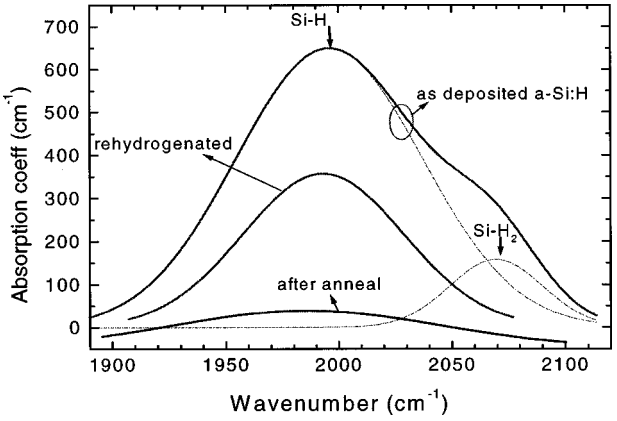

FIG. 1. Infrared absorption spectrum of the *a*-Si:H films around 2000 cm^{-1} (Si–H stretch vibration). The spectrum of the as-grown film only is decomposed into the Si–H and $Si–H_2$ components. The total H contents of the as-deposited film is ~15 at. %, of the annealed film (with SiN_x cap) ~0.3 at. %, and of the rehydrogenated film ~4.4 at. %.

evident in the Si–H stretching mode absorption at ~2000 cm^{-1} (Fig. 1). The mid-gap defect state density increased from $<6\times10^{17}$ to $\sim4\times10^{19}$ cm^{-3} after the anneal, as deduced from the absorption coefficient at 1.3 eV measured by photothermal deflection spectroscopy (PDS) (Fig. 2).[12] The dangling bond densities as measured by PDS are rather high in this case as the films used were only 300 nm thick and the measurement is sensitive to the presence of surface states. The *a*-Si:H top-gate transistors made with this film had electron mobilities of only 0.01 cm^2/V s with an ON/OFF current ratio of only $\sim10^4$.

Rehydrogenation was thus necessary to reduce the defect state density in both the amorphous and polycrystalline silicon. This was done after stripping the patterned SiN_x cap layer with dilute HF and exposing the sample to a low ion-energy hydrogen plasma. The conditions were a substrate temperature of 350 °C, a rf power density of ~0.2 W/cm^2, and a pressure of 1 Torr. Rehydrogenation for 75 min increased the hydrogen content of the film to ~4.4 at. % as measured by the IR absorption at 630 cm^{-1}. The increase in hydrogen content resulted in the passivation of the Si dangling bonds to $\sim6\times10^{18}$ cm^{-3} and therefore led to a decrease in subgap absorption as can be seen in Fig. 2.

Rehydrogenation, in addition to increasing the hydrogen

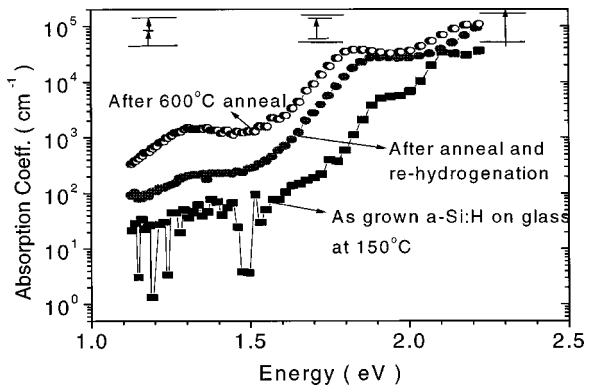

FIG. 2. Photothermal deflection spectra of the optical absorption coefficient of *a*-Si:H films in the as-deposited, annealed with SiN_x cap layer at 600 °C, and rehydrogenated states. The inset shows the relevant transitions at different energies in a band diagram.

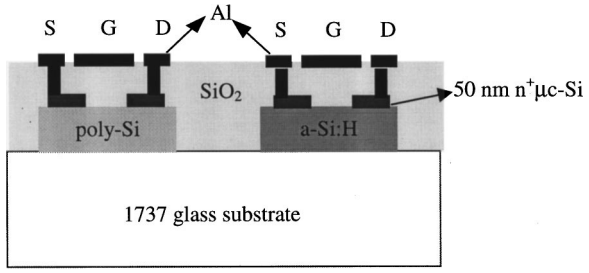

FIG. 3. Cross section of top-gate integrated *a*-Si:H and poly-Si TFTs on glass substrate.

content of the *a*-Si:H, improves the electrical characteristics of the film. It is expected to improve its stability as the hydrogen predominantly bonds in the form of Si–H, in contrast to the as-grown *a*-Si:H film deposited at 150 °C, which had a considerable $Si–H_2$ content (Fig. 1). The Tauc optical gaps E_{opt} calculated from the optical transmission spectra above the band gap show that the E_{opt} drops to 1.6 eV from 1.8 eV during annealing, and that rehydrogenation raises E_{opt} to 1.7 eV. Dark conductivity σ_d measurement shows that σ_d of the *a*-Si:H film increases after the anneal and that σ_d has a low thermal activation energy, indicating conduction through defect states. Rehydrogenation brings the activation energy of the film closer to $E_g/2$, indicating a reduced defect density. Overall the data are consistent with a largely amorphous silicon film after the anneal and rehydrogenation.

The TFT fabrication required optimization of several parameters including deposition temperature of the precursor *a*-Si:H film and crystallization anneal temperature, which are discussed elsewhere.[5] Following the rehydrogenation step, ~50 nm of n^+ microcrystalline (μc-Si:H) silicon for source/drain contacts, was deposited by PECVD. Device islands were then defined by dry etching in a SF_6/CCl_2F_2 plasma, and future channel regions were defined by dry etching just the n^+ μc-Si:H layer in a separate etching step.

The gate dielectric, ~180 nm of SiO_2, was then deposited by PECVD at a substrate temperature of about 250 °C using SiH_4 and N_2O. Etching in dilute HF opened contact holes to the source/drain regions. Aluminum was then evaporated and patterned to form the gate and source and drain contacts (Fig. 3). The samples were then annealed at 200 °C in forming gas. The same top-gate process was simultaneously applied to both the amorphous and the polycrystalline silicon regions, with the only difference between the two types of devices being the mask which determines the pattern of the SiN_x layer for masking the hydrogen plasma seeding process. Note this is not a self-aligned process; the source/drain contact process is similar to that for standard inverted-staggered *a*-Si:H TFTs.

The properties of the *a*-Si:H TFTs were critically dependent on the rehydrogenation conditions.[5] The best *a*-Si:H TFT performance was achieved for a crystallization anneal at 625 °C and rehydrogenation time of 75 min at rf power density of 0.2 W/cm^2, resulting in a field-effect mobility of ~1.2 cm^2/V s and ON/OFF current ratio of $>10^6$ [Fig. 4(a)].

Integration constraints the processing parameters, so that the integration of both *a*-Si:H and polysilicon TFTs together resulted in field-effect mobilities of ~0.7 and ~15 cm^2/V s for the *a*-Si:H and poly-Si TFTs, respectively. The I_{OFF} was

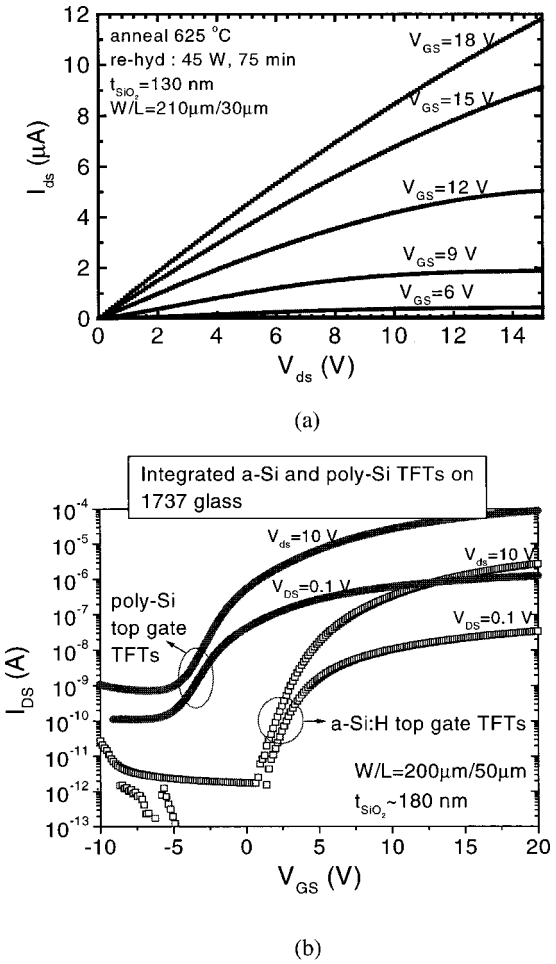

FIG. 4. TFT characteristics of: (a) the best *a*-Si:H top-gate TFT fabricated after 600 °C anneal with linear field-effect mobility of ~1.2 cm^2/V s, and (b) optimized integrated *a*-Si:H and poly-Si TFTs on the same glass substrate.

~10 fA/μm at $V_{DS}=10$V for the *a*-Si:H TFT. The ON current of the poly-Si TFT was $\geqslant 0.75$ μA/μm, with ON/OFF ratios of both types of devices $\geqslant 10^5$ [Fig. 4(b)]. These results compare favorably with other work on integrated *a*-Si:H and poly-Si TFTs using laser processing, which resulted in *a*-Si TFTs with field-effect mobility of ~0.9 cm^2/V s and poly-Si TFTs with field-effect mobility of ~20 cm^2/V s.[1] Note that conventional bottom-gate *a*-Si:H TFTs have field-effect mobility of ~1 cm^2/V s,[3] and the typical result for top-gate *a*-Si:H TFT with SiN_x as the gate dielectric, is a field-effect mobility of ~0.4 cm^2/V s and ON/OFF current ratio of $\sim 10^5$.[13] We know of no other comparable results of *a*-Si:H TFTs after such a high temperature (600–625 °C) anneal step.

In summary, we have successfully integrated *a*-Si:H and polysilicon TFTs on the same substrate in a single silicon layer without laser processing. Only a single extra mask step beyond that for a single type of TFT is required. The critical process steps are the selective crystallization of *a*-Si:H by patterned plasma exposure and the rehydrogenation of the *a*-Si:H.

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