Doped and Undoped SiGeC Layers for Dopant Profile Control in sub-100 nm Vertical MOSFET's

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Introduction/Abstract

Vertical FET structures are of interest because they allow short channel lengths to be defined without lithography, and can be gated from two-sides if the pillar is thin. Such double-gated (or wrap-around) gates offer the possibility of low off-currents at room temperature and allow one to eliminate channel doping (and the resulting statistical fluctuation problems) [1,2]. In this work the use of $Si_{1-x-y}Ge_xC_y$ layers is explored to make vertical structures stable to thermal processing (e.g. sidewall gate oxide growth or implantation annealing), and the method is demonstrated with sub 100-nm p-channel FET's.

Diffusion Control and Device Results

Fig. 1 shows a process simulation of how severely a 750°C wet oxidation step causes boron to diffuse from a pre-defined vertical FET structure with a channel length of 110 nm, which clearly makes any device impossible. If one artificially turns off the oxidation-enhanced diffusion (OED) in the simulator, sub-100nm devices become possible. Similar results would occur from transient-enhanced-diffusion (TED) during low-temperature annealing of conventional ion implantations performed above the FET structure due to defect migration. Over the last few years, it has been shown that low levels of C in $Si_{1-y}C_y$ or $Si_{1-x-y}Ge_xC_y$ (<1%C) are effective at gettering Si interstitial atoms, and thus reducing the OED and TED effects [3,4]. The diffusion of B can be reduced some distance from the actual $Si_{1-x-y}Ge_xC_y$ layers (Fig. 2).

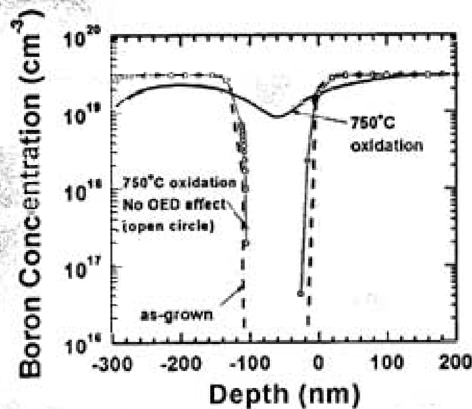
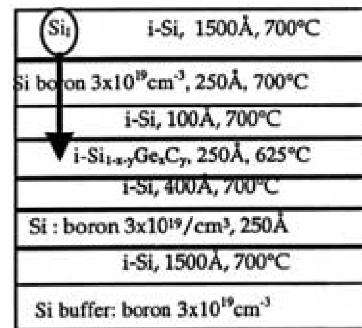


Fig.1. Simulation of boron diffusion in a 110nm vertical p-channel FET with oxidation enhanced diffusion turned on and off (750°C, 40min).



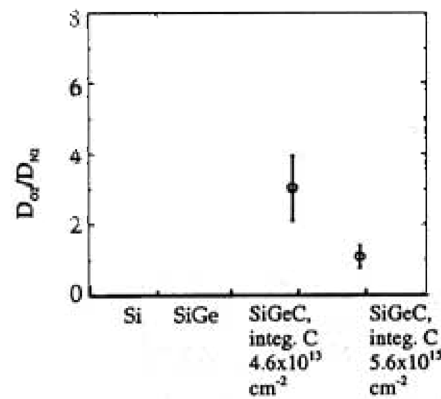


Fig. 2. (a) Buried marker structure to study ability of SiGeC to getter interstitials and reduce OED; (b) relative B diffusion coefficient in O_2 vs. N_2 in lower B layer under 850°C oxidation as function of C levels in the SiGeC blocking layer.

Therefore undoped 20nm SiGeC layers (20% Ge, ~0.4%C) were inserted into the channel next to S/D (Fig. 3) or p^+ doped SiGeC layers were inserted into the S/D itself to curb boron diffusion. The device structures were made by growing the entire source/channel/drain structure by RTCVD epitaxy at 625-750°C, since the channel length is then directly controlled and does not depend on etch times, etc. Only wide pillar devices with phosphorus-doped channels ($\sim 2\times10^{18} cm^{-3}$ with ~15nm/decade profile control) have been made to date. Various tradeoffs of doped vs. undoped SiGeC and channel designs will be discussed. Nearly ideal devices can be made at channel lengths well under 100 nm, far shorter than previous bests for p-channel devices of 200 nm for S/D implantation after gate oxidation[6] and 140nm for 600°C oxides at high pressure with epitaxially grown S/D's [7]. Note leakage currents remain very low even with the SiGeC (Fig. 4). Devices with L of 25 nm are reasonable above threshold, but suffer from punchthrough below threshold.

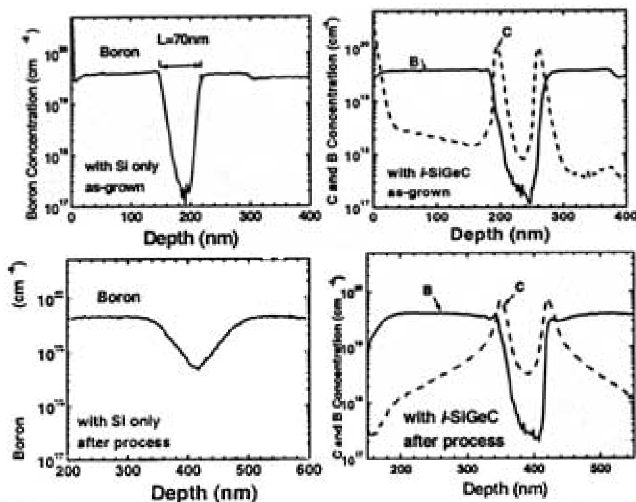


Fig. 3. SIMS profiles of vertical p-channel FET structures both before and after sacrificial and gate oxidation (750°C, 40min total) for all silicon and undoped $Si_{1-x-y}Ge_xC_y$ boron barriers (20nm) just outside the S/D in the channel.

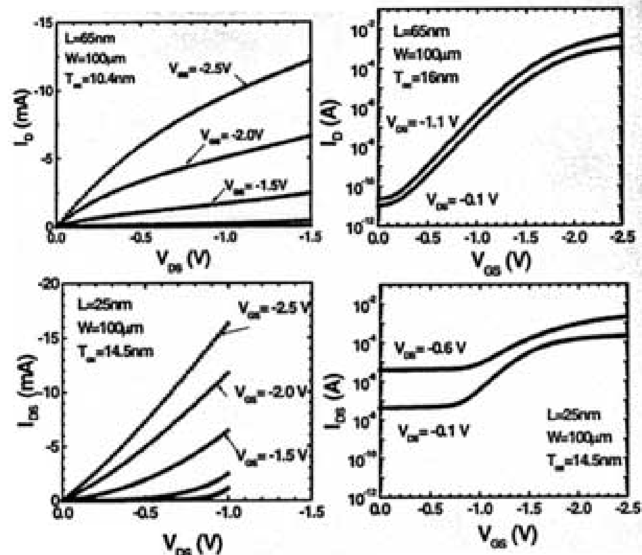


Fig. 4. Linear and subthreshold characteristics for L = 65 nm and L = 25 nm vertical p-channel FET's.

Summary

$Si_{1-x-y}Ge_xC_y$ layers can be effectively used to dramatically improve control of dopant profiles in short-channel devices, making them more tolerant of thermal processing. This can be achieved without a penalty of increased leakage. Current work in progress is attempting to combine these results with dual-gate structures, and to exploring the ability to minimize the diffusion of n-type dopants as well. The support of ONR and DARPA is gratefully acknowledged.

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