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Boron Segregation in Polycrystalline $Si_{1-x-y}Ge_xC_y$ Alloys

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Polycrystalline $Si_{1-x-y}Ge_xC_y$ gates have been previously shown to greatly reduce the penetration of boron through thin gate oxides in PMOS structures[1]. PMOS capacitors made with a layer of poly $Si_{1-x-y}Ge_xC_y$ in the heavily boron doped ($\sim 10^{21}/cm^3$) gate electrode had greater resistance to boron penetration through the gate oxide than those with all polycrystalline Si or polycrystalline $Si_{1-x}Ge_x$ gate electrodes. Boron readily diffused out of the poly Si and poly $Si_{1-x}Ge_x$ gates and through the gate oxide during high temperature anneals (900°C). In the structures with poly $Si_{1-x-y}Ge_xC_y$ gates, however, boron accumulated in the $Si_{1-x-y}Ge_xC_y$ layer, significantly reducing diffusion through the gate oxide. This effect appears to be due to boron preferentially remaining in poly $Si_{1-x-y}Ge_xC_y$ layers, possibly because it has a lower chemical potential in $Si_{1-x-y}Ge_xC_y$ than in Si or $Si_{1-x}Ge_x$, not due to the lower diffusion coefficient of boron in crystalline SiGeC as has recently been reported[2].

In this abstract we report, to the best of our knowledge, the first independent evidence of boron segregation into both polycrystalline and crystalline $Si_{1-x-y}Ge_xC_y$ from Si. Layers of poly $Si_{1-x}Ge_x$ and poly $Si_{1-x-y}Ge_xC_y$ were grown on a wet chemically oxidized p-type substrate by Rapid Thermal Chemical Vapor Deposition(RTCVD). Each SiGe(C) layer was isolated by polycrystalline silicon spacer layers on both sides. The poly $Si_{1-x}Ge_x$ and $Si_{1-x-y}Ge_xC_y$ layers were grown at 625°C and $x \approx 0.2$; the poly Si spacer layers were grown at 700°C. All layers were doped in-situ with boron at $\sim 1x10^{20}/cm^3$. Silane, germane, diborane, and methylsilane were used as source gases in a hydrogen carrier gas at 6 torr. Oxygen levels in all layers were much less than boron or carbon levels. These structures were then annealed at 800°C for 18 hours in nitrogen. Concentration vs. depth profiles of all relevant materials in the structure were obtained by Secondary Ion Mass Spectroscopy (SIMS).

Boron clearly segregated from the silicon into the $Si_{1-x-y}Ge_xC_y$ layers during the anneal. In the poly $Si_{1-x}Ge_x$ layers, boron outdiffused into the adjacent poly Si layers,

causing concentration profiles to flatten out. In the poly $Si_{1-x-y}Ge_xC_y$ layers with significant carbon content(>0.1%), boron concentrations actually increased after annealing, with boron levels decreasing in the adjacent poly Si layers. In the $Si_{1-x-y}Ge_xC_y$ layer with 1% (~$5x10^{20}/cm^3$) carbon, the boron levels after annealing were approximately four times higher than in the adjacent silicon layers. Any tendency of boron to segregate to polycrystalline $Si_{1-x}Ge_x$ layers without carbon was an order of magnitude weaker, consistent with observations in crystalline $Si_{1-x}Ge_x$/Si samples[3]. We have also observed large segregation of boron to $Si_{1-x-y}Ge_xC_y$ in crystalline $Si_{1-x-y}Ge_xC_y$ /Si samples.

Initial electrical data suggests that the boron is still electrically active after segregation to $Si_{1-x-y}Ge_xC_y$, and does not segregate to electrically inactive defect sites. This is fortuitous for device applications such as polycrystalline gates. Existing models for boron segregation in the $Si_{1-x}Ge_x$/Si system are based on lattice strain and valence band offset arguments[4]. From both of these arguments, less boron diffusion to $Si_{1-x-y}Ge_xC_y$ than $Si_{1-x}Ge_x$ would be expected. A new model to explain our data will be presented.

References

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