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Doped vs. undoped $Si_{1-x-y}Ge_xC_y$ layers in sub-100 nm vertical p-channel MOSFETs

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Abstract

By introducing $Si_{1-x-y}Ge_xC_y$ layers in vertical p-channel MOSFETs, boron diffusion from the source/drain regions into the channel region has been suppressed to enable sub-100 nm scaling. The trade-off of doped and undoped $Si_{1-x-y}Ge_xC_y$ layers has been studied. Due to detrimental effects from oxide grown on $Si_{1-x-y}Ge_xC_y$ layers, doped $Si_{1-x-y}Ge_xC_y$ diffusion barriers are preferable, and have allowed vertical p-channel MOSFETs with channel lengths down to 25 nm to be demonstrated. No excess leakage current due to the $Si_{1-x-y}Ge_xC_y$ layers is observed. © 2000 Elsevier Science S.A. All rights reserved.

Keywords: Vertical MOSFETs; Chemical vapor deposition; Diffusion

1. Introduction

Vertical MOSFETs have generated great interest because of potential savings in chip area and because it provides an alternative way to achieve short channel length, which may be determined by the epitaxial layer thickness [1]. However dopant diffusion from the source/drain into the channel region during gate oxidation limits the device scaling of vertical MOSFETs. Many groups have used low temperature (≤650°C) to fabricate the gate oxide on both p- and n-channel vertical MOSFETs [2–4]. We have demonstrated sub-100 nm vertical p-channel MOSFETs with channel lengths down to 25 nm using conventional oxidation conditions (750°C), which may offer higher oxide quality, by adding thin $Si_{1-x-y}Ge_xC_y$ epi-layers to suppress the boron oxidation enhanced diffusion (OED) effect [5]. In this paper, both doped and undoped $Si_{1-x-y}Ge_xC_y$ layers in the source/drains of vertical p-channel MOSFETs are presented. Due to thicker sidewall gate oxide grown on $Si_{1-x-y}Ge_xC_y$ layers, doped $Si_{1-x-y}Ge_xC_y$ in the source and drain is preferable. No excess leakage current after adding $Si_{1-x-y}Ge_xC_y$ layers is observed.

2. Device fabrication and results

Vertical p-channel MOSFETs were fabricated on the etched side-walls of epitaxial layers grown by rapid thermal chemical vapor deposition (RTCVD) [6]. Twenty-six sccm dichlorosilane (DCS) is the silicon source, carried by 3 lpm hydrogen. Dopant gases are phosphine and diborane. The growth pressure is maintained at 6 Torr. After a p^+ silicon buffer layer, the channel region is grown at 700°C and doped to $\sim 10^{18} cm^{-3}$ (n-type) in order to suppress punch-through in the center of the mesa. Special steps are taken to eliminate auto-doping so that the top edge of the phosphorus decays at <17 nm/decade [7]. The top p^+ silicon is grown at 750°C. The side-walls (50–100 μm × 50 μm mesa) were formed by photo-lithography and reactive ion etching. Then the gate oxides are grown at 750°C in wet oxygen after a sacrificial oxidation. Gate poly-silicon is deposited at 700°C using silane and in situ doped with boron. Deposited oxide and metal contacts completed the processing.

The introduction of $Si_{1-x-y}Ge_xC_y$ layers can stop the oxidation-enhanced diffusion of boron during the sidewall gate oxidation, as substitutional carbon atoms behave as a sink for interstitials [5,8,9]. To investigate the effect of $Si_{1-x-y}Ge_xC_y$ layers on the device performance of vertical p-channel MOSFETs, four epitaxial structures were grown, with 200 Å undoped $Si_{0.8}Ge_{0.2}$ (Fig. 1b), undoped $Si_{0.796}Ge_{0.2}C_{0.004}$ (Fig. 1b), doped $Si_{0.796}Ge_{0.2}C_{0.004}$ (Fig. 1c), and all silicon (Fig. 1a). The $Si_{0.8}Ge_{0.2}$ and $Si_{0.796}Ge_{0.2}C_{0.004}$ epitaxial layers were grown at 625°C using 1 sccm germane and/or 0.05 sccm methylsilane. The channel lengths (L) are 70 nm for the all-silicon device, 100 nm for the undoped SiGe (C) devices and 80 nm for the doped SiGeC device. The channel doping is $\sim 1.0 \times 10^{18}$ cm^{-3}. The subthreshold characteristics of the four devices are shown in Fig. 2. Devices with only silicon or undoped SiGe layers are

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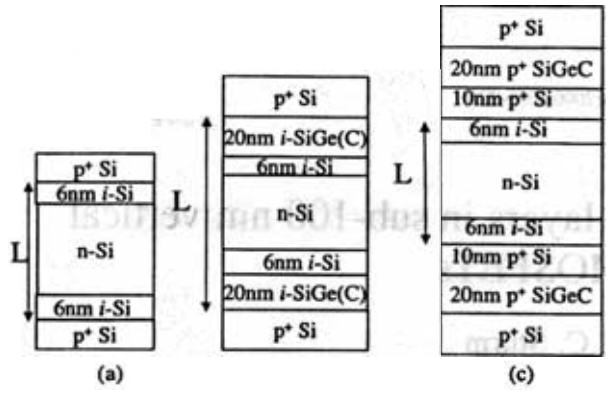

Fig. 1. Vertical p-channel MOSFET epitaxial layers grown by RTCVD for various structures: (a) with silicon only, (b) with 200 Å undoped $Si_{0.8}Ge_{0.2}$ and $Si_{0.796}Ge_{0.2}C_{0.004}$ layers, (c) with 200 Å doped $Si_{0.796}Ge_{0.2}C_{0.004}$. Channel lengths are (a) 70 nm, (b) 100 nm and (c) 80 nm, respectively.

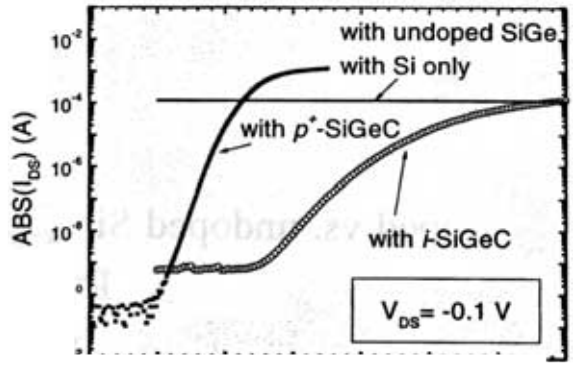

Fig. 2. Subthreshold characteristics of devices shown in Fig. 1. Vertical p-channel MOSFETs are shorted for devices made with silicon only and with undoped $Si_{0.8}Ge_{0.2}$ layers.

shorted between source and drain. However, devices with doped and undoped SiGeC have a reasonable on/off current ratio. Boron diffusion from the source/drain into the channel region during gate oxidation in devices with all silicon was confirmed by secondary ion mass spectroscopy (SIMS) (Fig. 3a) [5]. In contrast, the device with undoped SiGeC layers kept its sharp boron profile after the high temperature processes of 750°C in O_2 for 40 min and 700°C for 30 min (Fig. 3b) [5].

Placing undoped $Si_{1-x-y}Ge_xC_y$ layers near the channel is

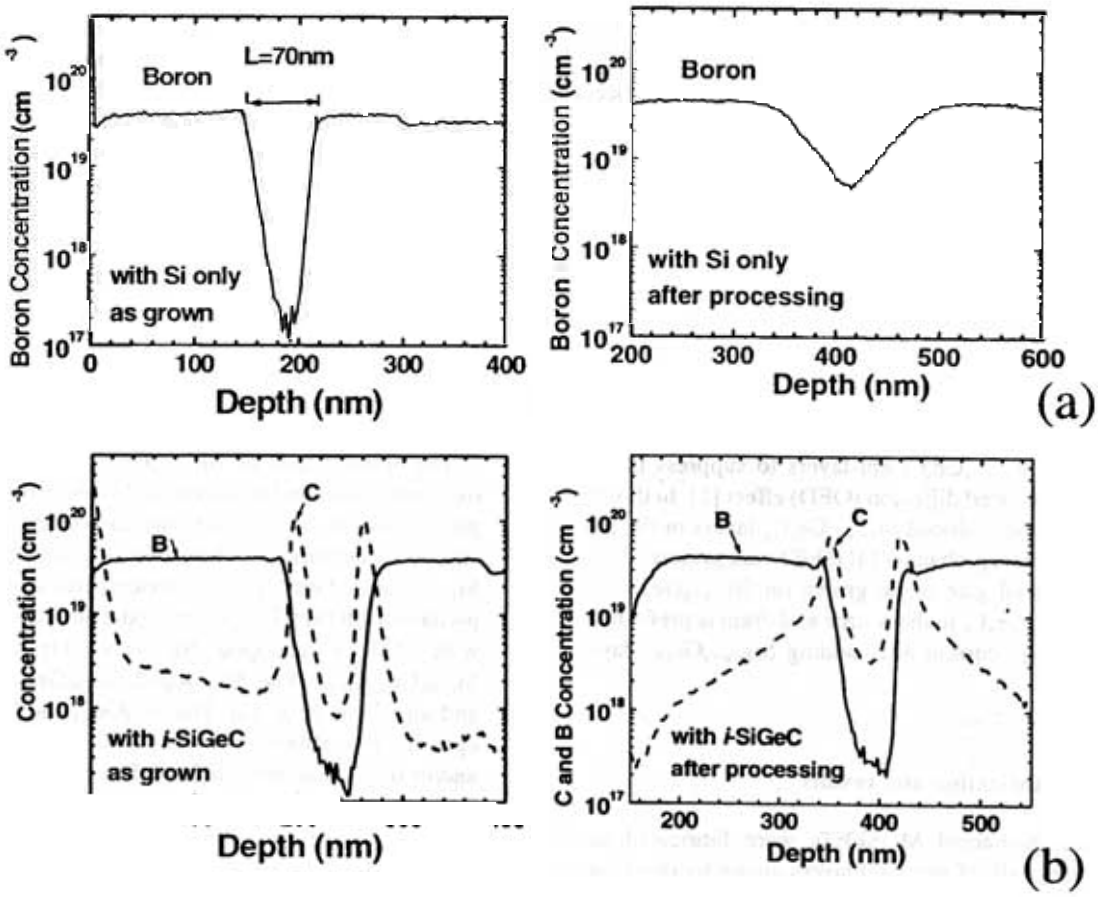

Fig. 3. SIMS results of devices shown in Fig. 1, (a) with silicon only and (b) with undoped $Si_{0.796}Ge_{0.2}C_{0.004}$ before and after all the high temperature processing (sacrificial and gate oxidation (750°C 40 min total) and poly-Si deposition (700°C 30 min)) [5]. Reprinted with permission of IEEE.

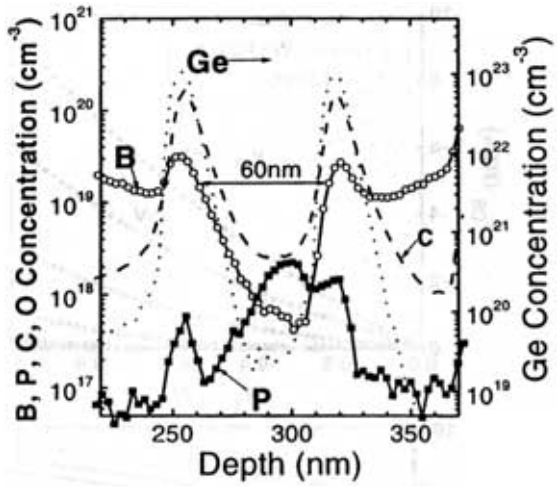

Fig. 4. SIMS results of vertical p-channel MOSFETs with doped $Si_{0.796}Ge_{0.2}C_{0.004}$ layers after all the high temperature processing. The boron diffusion from source/drain and the 10 nm p^+ Si region are also suppressed, similar to the results from undoped SiGeC (Fig. 3b).

very effective to prevent boron diffusion during oxidation. However, there is concern whether the channel properties are dependent on $Si_{1-x-y}Ge_xC_y$ and the $Si_{1-x-y}Ge_xC_y/SiO_2$ interface. As plotted in Fig. 2, the threshold voltage magnitude and subthreshold slope of the devices with undoped SiGeC layers are much larger than expected. It is known that Ge greatly enhances the oxidation rate and that oxide quality on $Si_{1-x}Ge_x$ is inferior to that on Si [10–12]. Thus we conclude that undoped SiGeC layers in part of the channel and resulting poor oxide interface qualities lead to the higher threshold voltages and poor subthreshold slopes.

To eliminate the oxidation problem of Ge and possible deleterious effects from C, devices with heavily doped $Si_{0.796}Ge_{0.2}C_{0.004}$ ($\sim 3\times10^{19}\ cm^{-3}$) have also been made. In addition, 10 nm p^+ Si are inserted between the SiGeC and the channel in order to prevent the depletion region from penetrating into the SiGeC layers. In this case, the channel is totally constrained in silicon layers. As shown in Fig. 2, devices with doped $Si_{0.796}Ge_{0.2}C_{0.004}$ have much lower threshold voltage magnitude and sharper subthreshold slope compared to those with undoped SiGeC. SIMS measurement confirms that using doped SiGeC, oxidation enhanced boron diffusion from the source/drain, and even from the p^+ Si regions outside SiGeC, is still suppressed (Fig. 4). This is thought to be because the SiGeC lowers the excess interstitial concentration in nearby Si regions [9].

The characteristics of various device structures are listed in Table 1. By optimizing the location of SiGeC regions, vertical p-channel MOSFETs could be scaled to a channel length deep under 100 nm for the first time. Vertical p-channel MOSFETs with channel length (L) 80 nm and $N_{channel} = 1\times10^{18}$ cm^{-3} are demonstrated with well behaved characteristics at room temperature (Fig. 5). Working devices have been made with L down to 25 nm (Fig. 6), although they have large leakage current from punch-through, as the peak channel doping is only 3×10^{18} cm^{-3} (as measured by SIMS). However, without SiGeC to stop boron diffusion, the channel length is limited to $>>100$ nm [3,4,13]. In this work the gate oxides are relatively thick (>100 Å). Estimations of the subthreshold slopes with a thinner gate oxide (3 nm), extracted from our current experimental data, are also listed in Table 1 for comparison. To reduce the short channel effects in sub-100 nm especially sub-50 nm MOSFETs, thin pillar structures (<100 nm) instead of a wide mesa (as in our work) have been proposed to seek better still gate control through double-gate or surrounding-gate with a fully depleted channel region [14,15].

It is known that carbon atoms may act as scattering or recombination centers and affect carrier transport. Recently it has been reported that $Si_{1-x-y}Ge_xC_y$ or $Si_{1-y}C_y$ used to control boron diffusion leads to larger leakage current for heterojunction bipolar transistors [16] and lateral nMOS-

Table 1
Comparison of device performance of various vertical p-channel MOSFETs with 200 Å doped and undoped $Si_{0.796}Ge_{0.2}C_{0.004}$ diffusion barriers, along with all silicon devices and undoped $Si_{0.8}Ge_{0.2}$ devices[a]

Structure	L (μm)	t_{ox} (nm)	Peak channel doping N_D (cm^{-3}) after processing	V_T (V)	I_{off} (A/μm) at $V_{DS} = -1$ V	Subthreshold slope S_t (mV/dec) at $V_{DS} = -0.1$ V	Predicted S_t (mV/dec) for $t_{ox} = 3$ nm
All Si	0.5	17	9×10^{17}[b]	−1.4	5×10^{-12}	90	65
i-SiGeC	0.5	17	1.4×10^{18}[b]	−3.5	10^{-12}	180	81
p-SiGeC	0.5	17	1.4×10^{18}[b]	−2.0	5×10^{-12}	150	76
All Si	0.07	23	1.2×10^{18}	Source/drain shorted			
i-SiGe	0.1	23	1.2×10^{18}	Source/drain shorted			
i-SiGeC	0.1	23	1.5×10^{18}	−4.0	6×10^{-12}	400	104
p^+-SiGeC	0.08	10.4	1.0×10^{18}	−1.3	10^{-12}	88	68
	0.065	16	2.5×10^{18}	−1.7	10^{-13}	190	84
	0.025	11.5	4×10^{18}	Punch-through			

[a] Channel dopings are from SIMS after all the high temperature processing, except where indicated. The prediction of subthreshold slopes for devices made with thinner gate oxides are also listed.
[b] Estimated.

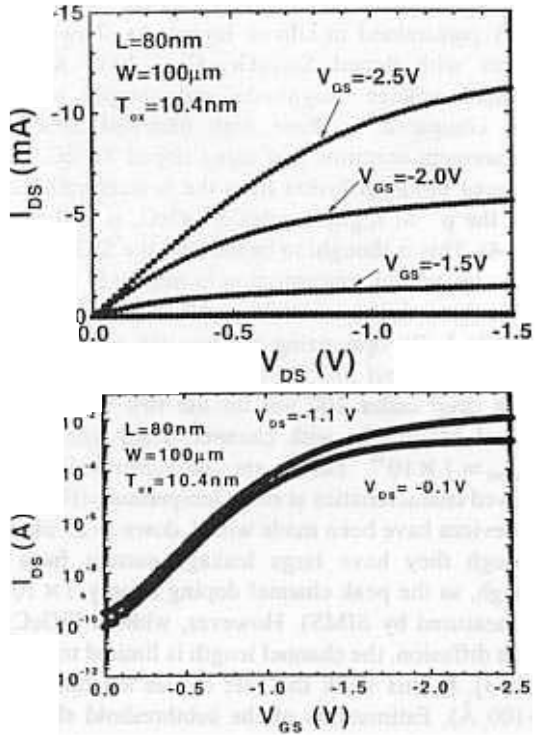

Fig. 5. Current-voltage and subthreshold characteristics of vertical p-channel MOSFETs with $L = 80$ nm.

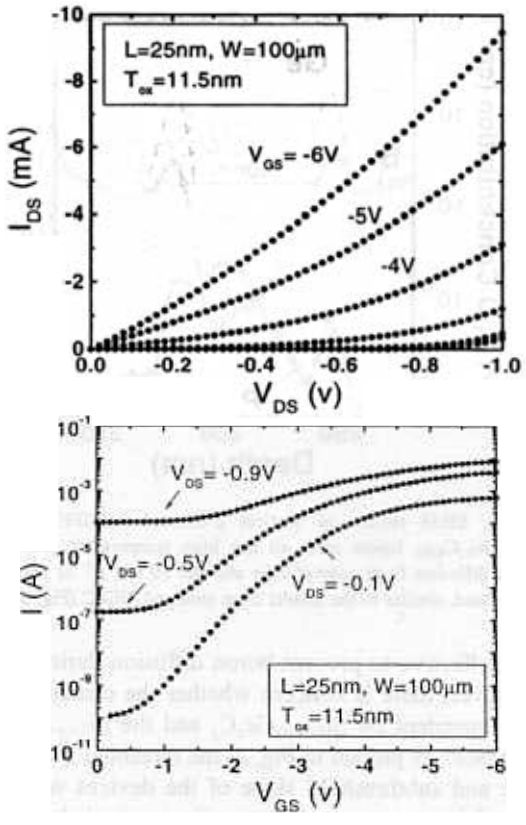

Fig. 6. Current-voltage and subthreshold characteristics of vertical p-channel MOSFETs with $L = 25$ nm.

FETs [17,18]. However, it is also reported that for carbon concentration less than 0.1%, there is no obvious adverse effect from carbon [19,20]. In this work, both for the devices with undoped and doped $Si_{0.796}Ge_{0.2}C_{0.004}$ layers, the leakage current is as low as in all-silicon control devices (Table 1), suggesting that all the carbon atoms in the $Si_{0.796}Ge_{0.2}C_{0.004}$ layers are substitutional and that 0.4% carbon is low enough not to induce any excess leakage current. Note that in our process, we kept the temperatures lower than 800°C to avoid SiC precipitation and $Si_{0.796}Ge_{0.2}C_{0.004}$ strain relaxation.

3. Conclusion

In summary, by introducing doped and undoped $Si_{1-x-y}Ge_xC_y$ layers in the vertical p-channel MOSFETs, boron diffusion from the source and drain into the channel region during gate oxidation is suppressed. Junction leakage current, hole mobility and subthreshold slopes are not adversely affected by the p^+ $Si_{1-x-y}Ge_xC_y$ layers, which are best for device scaling. Sub-100 nm vertical p-channel MOSFETs have been demonstrated.

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