6.2 GHz Digital CMOS Circuits in Thin SIMOX Films

G. K. Celler, Avid Kamgar, H.-I.Cong, R. L. Field, S. J. Hillenius,
W. S. Lindenberger, and L. E. Trimble
AT&T Bell Laboratories, Murray Hill, NJ 07974

and

J. C. Sturm
Dept. of Electrical Engineering, Princeton University, Princeton, NJ 08544

CMOS dual-modulus prescaler circuits were built in very thin SIMOX films. They operate at 6.2 GHz, the highest speed ever reported for a digital CMOS circuit and 50% faster than the control circuits built in bulk Si. The high speed is obtained by taking advantage of the intrinsic properties of the SOI structure combined with the symmetric CMOS technology that optimizes simultaneously the characteristics of both the p and n-channel transistors.

The SOI structure was formed by implanting 4-inch n-type (100) wafers with 1.7×10^{18} oxygen ions at 200 keV while holding the substrate temperature at 615 °C. The wafers were then coated with 0.5μm of LPCVD oxide and annealed for 30 min in a lamp furnace. Wafers were heated from the back side up to their melting temperature so that the optical properties of Si would provide an intrinsic feedback necessary to keep the device side precisely at 1405 °C [1]. After annealing the structure consisted of 2400 Å of crystalline Si with some dislocations but no oxide precipitates, on 3500 Å of synthesized SiO_2, with atomically abrupt interfaces. Subsequently, the Si overlayer was thinned by oxidation to 1200 Å to obtain films that are fully depleted in the transistor channel regions. Full depletion eliminates a kink in the I-V curves that is characteristic of floating channel effects in SOS and thicker SOI devices [2].

Device fabrication processes were optimized for bulk Si and not for SOI structures. Lateral isolation was achieved by local oxidation through the Si film thickness. Gate oxide thickness was 125 Å and $CoSi_2$ was used in the source, drain, and gate areas. The prescalars, designed as dual modulus divide-by-128 or 129 counters, consisted of a high speed divide-by-4 or 5 counter, and a lower speed divide-by-32 counter [3]. To reduce the capacitive loading, 0.75μm wide aluminum lines and 0.5μm metal salicide runners were used.

Current-voltage characteristics for both n- and p-channel devices with the effective channel lengths, L_{eff}, down to 0.4μm, show no trace of the kink effect. The threshold voltages for -6V substrate bias are 0.24V and -0.30 V, and the mobilities are 740 $cm^2/Vsec$ and 185 $cm^2/Vsec$, in n- and p- channel transistors, respectively. The delays per stage measured in 49 stage ring oscillators are shown in Fig. 1 for the SOI and bulk monitor wafers. The SOI structure increases the oscillation frequency by at least 40%.

Prescalar circuits were built with L_{eff} ~0.4μm. The best circuits were fully functional at 6.2 GHz, as shown in Fig. 2, consuming 210 mW at V_{dd} of 3.5 V. Identical circuits built in bulk Si wafers were operational up to 4.2 GHz. To optimize threshold voltage for n- and p-type channels simultaneously, a substrate bias of -4 to -6.5 V was applied. The dependence of the maximum operating frequency on the supply voltage is shown in Fig. 3. At $V_{dd} = 1.4V$, the prescalars are still operational at 2 GHz and dissipate only 11 mW of power.

[1] G. K. Celler, P. L. F. Hemment, K. W. West, and J. M. Gibson, Appl. Phys. Lett. **48,** 532 (1986).

[2] J.-P. Colinge, IEEE Electr. Dev. Lett. **EDL-9,** 97 (1988).

[3] H.-I. Cong, J. M. Andrews, D. M. Boulin, S. C. Fang, S. J. Hillenius, and J. A. Michejda, IEEE J. Solid State Circuits, **23,** 1189 (1988).

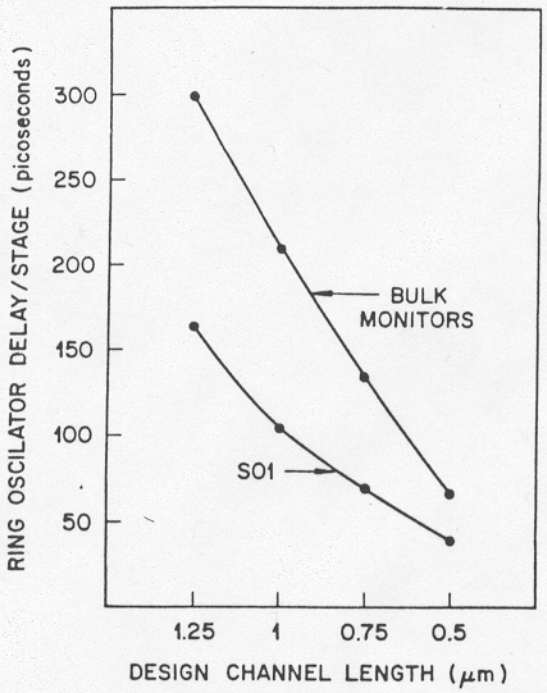

Fig. 1. Ring oscillator delay vs. channel length for SOI and bulk Si circuits.

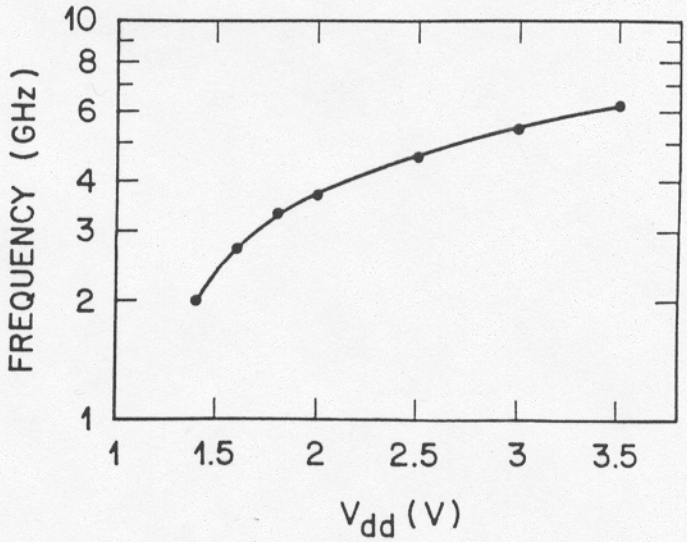

Fig. 3. Maximum operation frequency of the SOI prescalar as a function of the supply voltage.

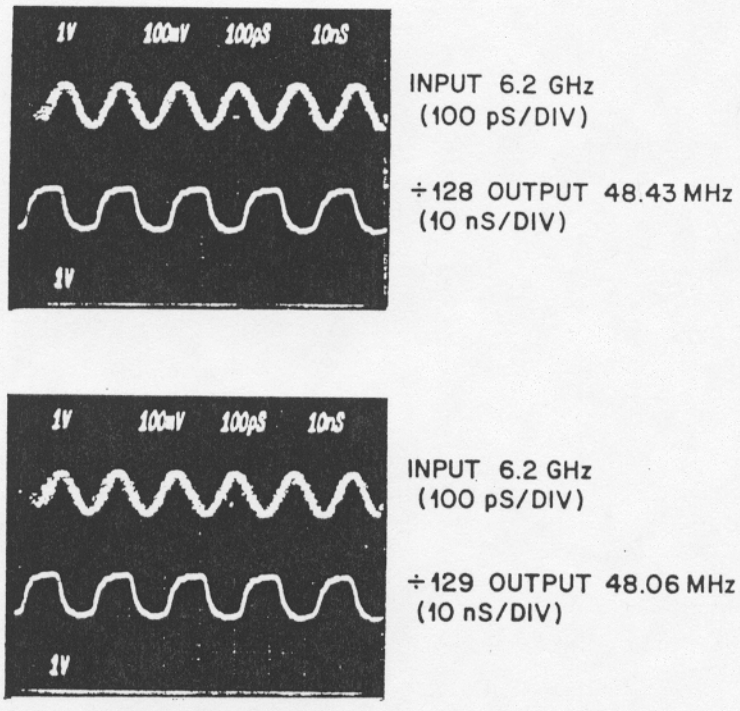

Fig. 2. Oscilloscope traces for the input and output signals for the SOI prescalar; (a) divide-by-128, and (b) divide-by-129.