Relaxation Dynamics and Electrical Properties of SiGe Islands on BPSG

Haizhou Yin, J. C. Sturm, and K.D. Hobart*
Department of Electrical Engineering
Center for Photonics and Optoelectronic Materials
Princeton University, Princeton, NJ 08544
609-248-6624, fax: 609-258-1954, hyin@ee.princeton.edu

*Naval Research Lab, Washington, DC 20357

There has been increasing interest in compliant substrates for integration of heterogeneous epitaxial materials. In this talk, borophosphorosilicate glass (BPSG) on silicon is used as a compliant substrate to allow the relaxation of strained SiGe layers. The talk will focus on the dynamics of the relaxation process and initial results of high mobility strained silicon structures grown on top of the relaxed SiGe.

The SiGe layers are first grown in a strained state on a (100) silicon wafer by CVD, and then bonded to the BPSG wafer. After the silicon substrate under the SiGe is removed by the Smart-Cut process, the SiGe is patterned into islands. The samples are then annealed at 800 ^{o}C to allow the SiGe to relax. The progress of the relaxation is followed by X-ray diffraction from the (400) peak of the SiGe layers. Small islands (10-micron edges) relax quickest, with full relation occurring in less than 17 minutes. 20-micron islands required between 17 and 90 minutes to fully relax. These small islands remained planar, and the rate of their relaxation is in good agreement with quantitative models which will be presented. Islands of larger sizes (40 microns) relaxed through a buckling process, as opposed to a simple planar expansion, and hence X-ray diffraction peaks of the relaxed layer could not be observed.

Rapid Thermal Chemical Deposition was used to selectively grow epitaxial SiGe/Si structures on top of the relaxed islands but not on the exposed oxide. As a probe of the relaxed layer quality, modulation doped 2-D electron gas structures were fabricated with the electron transport occurring in tensilely-strained Si were. The electrical results from these structures will be reported at the meeting.

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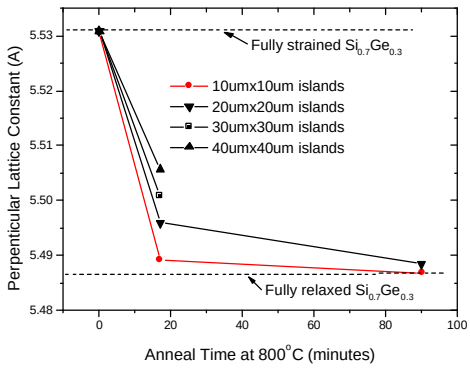

Perpendicular lattice constant of $Si_{0.7}Ge_{0.3}$ as a function of anneal time at 800^{o}C