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Large-Grain Polysilicon Films with Low Intragranular Defect Density by Low-Temperature Solid-Phase Crystallization

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ABSTRACT

Solid phase crystallization (SPC) of *a*-Si: H at 600 °C was investigated by transmission electron microscopy (TEM) and Raman spectroscopy in a cantilever structure, where the underlying SiO_2 was removed prior to the crystallization. The absence of the underlying oxide leads to both a higher grain size and a lower intragranular defect density. The grain size increases from 0.6 μm in regions with the underlying oxide to 3.0 μm without the underlying oxide, and the intragranular defect density decreases one order of magnitude from ~ 10^{11} cm^{-2} to ~ 10^{10} cm^{-2}. The improvements in material quality without the lower *a*-Si/SiO_2 interface are thought to be due to a lower nucleation rate and a lower tensile stress with an easier silicon atomic rearrangement at the lower silicon interface.

INTRODUCTION

Polysilicon thin film transistors (TFTs) are used in active-matrix-liquid-crystal displays (AMLCD) [1] and as upper-layer devices for three-dimensional VLSI [2]. For such active layers of TFTs, polycrystalline silicon crystallized from amorphous silicon by solid-phase crystallization (SPC) has attracted much interest. The electrical characteristics of polysilicon TFTs are strongly dependent on the polysilicon microstructure. The electron carrier mobility in polysilicon TFTs is typically < 100 cm^2/Vs, which is much less than that in single-crystalline silicon MOSFETs. Grain boundaries and intragranular defects (microtwins and dislocations) are electrical potential barriers and scattering sites, which decrease the mobility. Polysilicon films with a larger grain size and lower intragranular defect density have been a continual goal [3-6].

To date, there are two methods to decrease the density of intragranular defects of polysilicon films crystallized from *a*-Si: high-temperature (>750 °C) annealing [7] and laser crystallization [8]. However, high-temperature processing cannot be used in AMLCD TFTs, which are fabricated on glass substrates with a strain point less than 650 °C. Compared with the furnace annealing, laser crystallization has the potential disadvantages of high-cost and poor film uniformity. This paper examines how removing the underlying oxide before crystallization step can increase grain size and reduce defect density within grains, while maintaining the process temperature ≤ 600 °C.

EXPERIMENT AND RESULTS

Figure 1 shows the fabrication process of the cantilever structure of suspended *a*-Si. After depositions of 100nm-thick Si_3N_4 and 2μm-thick SiO_2 on a <100> silicon substrate, *a*-Si was

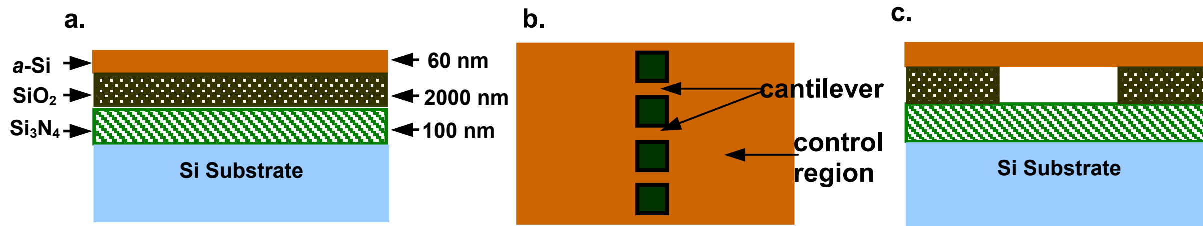

Figure 1. Fabrication process: (a) layer structure; (b) top view of cantilever structure after optical lithography and dry etching; (c) underlying oxide etch through the holes between the cantilevers. The cantilever width and length are ~ 5 μm and ~ 20 μm, respectively.

deposited at 150 °C by plasma-enhanced chemical-vapor-deposition (PECVD). The amorphous silicon was then patterned into islands with cantilever structures [Fig. 1(b)], and subsequent oxide etching in diluted HF through the holes created the *a*-Si cantilevers [Fig. 1(c)]. Furnace annealing at 600 °C transformed the film into polycrystalline. SEM observations confirmed the cantilevers did not collapse onto the substrate before or after furnace anneal. The microstructure of the polysilicon films was investigated by TEM and Raman scattering spectra, with the cantilever region (without underlying oxide) compared with the control region (with underlying oxide) in the same sample. The grain size of polysilicon was defined by the formula of $d = \sqrt{4A/\pi}$, where A is the area of a grain. The intragranular defect density was defined as the reciprocal of the defect-free area within a polysilicon grain.

TEM observations in Fig. 2 show the grain size of fully-crystallized polysilicon in (a) the control area with underlying oxide and (b) the cantilever area without underlying oxide after annealing at 600 °C for 24 hr. The average grain size increases from ~ 0.6 μm to ~ 3.0 μm. Comparison of the intragranular defect density in the control area with the cantilever area was also made by high-magnification TEM observations. Both of the grains in Fig. 3(a) and (b) have <110> crystal orientation. Defects from diffraction contrast are clearly seen in the control area [Fig. 3(a)]. Though the film in the cantilever area [Fig. 3(b)] is not defect free, the average

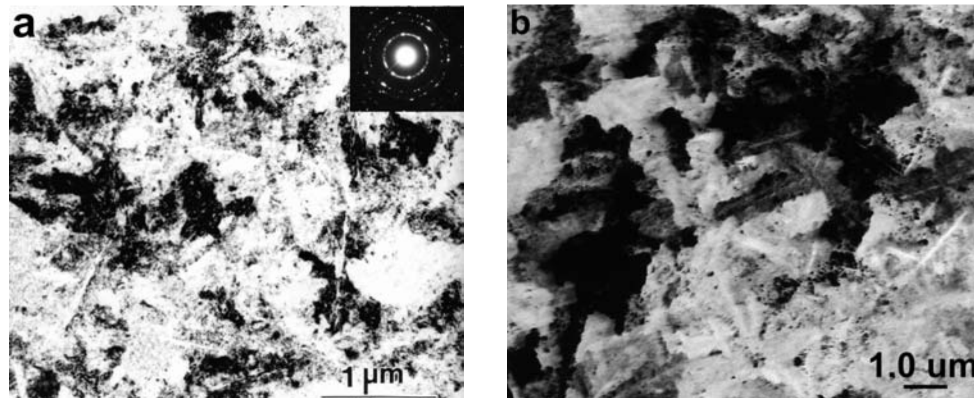

Figure 2. TEM micrograph of fully crystallized polysilicon films in (a) the control region with underling SiO_2 (grain size ~ 0.6 μm) and (b) the cantilever region without underlying SiO_2 (grain size ~ 3.0 μm) after furnace anneal at 600 °C for 24 hr.

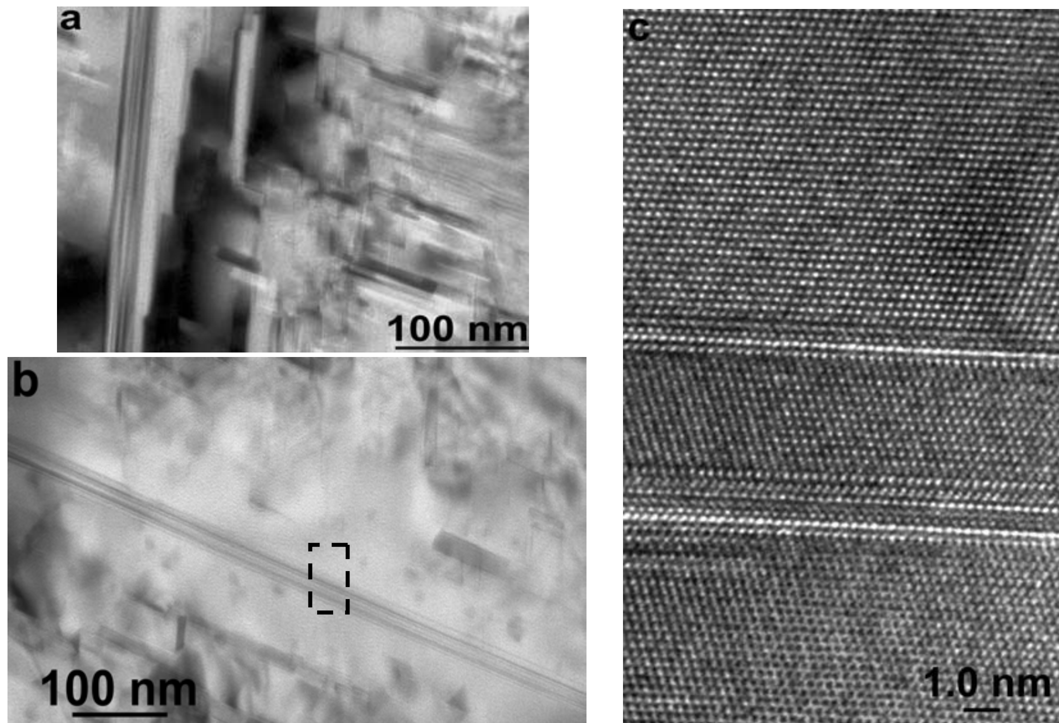

Figure 3. Microstructure of polysilicon grains oriented with <110> to show the defect density in (a) the control region and (b) the cantilever region. High-resolution TEM observation of (c) is from the marked area in (b) to show the perfect atomic arrangement on both sides of the microtwins.

defect-free area increases from ~ 25 nm [Fig. 3(a)] to ~ 100 nm in diameter, and the defect density is correspondingly reduced from ~ 10^{11} cm^{-2} to ~ 10^{10} cm^{-2}. The high-resolution TEM image [Fig. 3(c)] from the area marked by the dash line in Fig. 3(b) shows silicon atom periodic arrangements without any defect on both sides of the microtwins.

DISCUSSION

Nucleation Density and Grain Size

The SPC of *a*-Si involves two steps: nucleation and growth. The final grain size of polysilicon is related to the nucleation rate *N* and growth velocity v_g, expressed by the formula $d \propto \left[v_g / N \right]^{1/3}$, where *d* is the grain size [9]. It has been found that the lower *a*-Si/SiO_2 interface is the preferred nucleation site of SPC [10]. High nucleation rate at the *a*-Si/SiO_2 interface in the control area of silicon films results in many grains and thus a small size. By removing the *a*-Si/SiO_2 interface in the cantilever region, the nucleation density decreases. This can be observed before full crystallization (Fig. 4), where films were annealed at 600 °C for 14 hr *vs.* 24 hr in

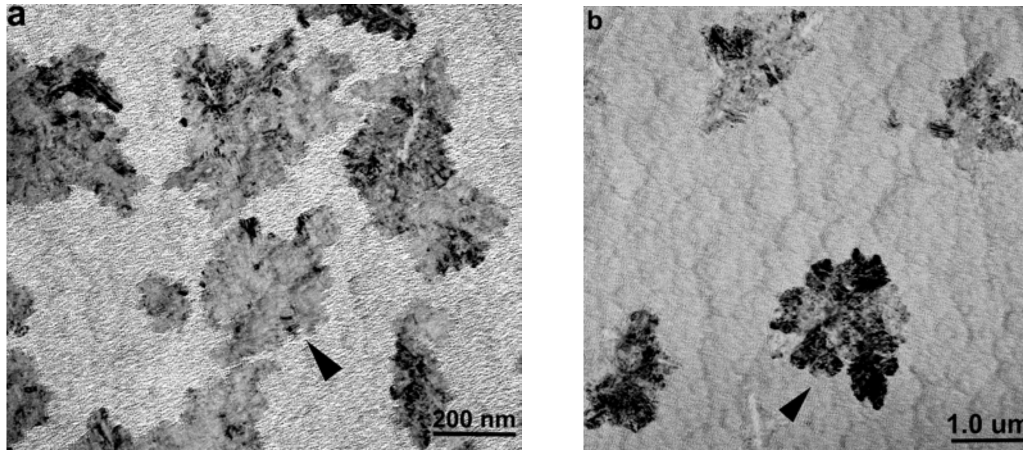

Figure 4. Plan-view TEM observation of polysilicion grain in (a) control region and (b) the cantilever region after annealing at 600 °C for 14 hr before complete crystallization, showing the grain density (~10^8 cm^{-2} vs. ~ 10^7 cm^{-2}) and grain size (~ 0.4 μm *vs.* ~ 1.0 μm).

Figure 2. The nucleation density in the cantilever area [Fig. 4(b)] is ~ 10 times lower than that in the control area [Fig. 4(a)] (~10^7 cm^{-2} *vs.* ~10^8 cm^{-2}). This lower nucleation rate in the free-standing films leads to larger grain size.

Stress during Solid-Phase Crystallization

It should also be noted that the grain size in Fig. 4(b) is ~ 1.0 μm, larger than the grain (~ 0.4 μm) in Fig. 4(a). This means the crystalline grains in the cantilever area have a higher growth rate than in the control area. Grain growth is driven by the Gibbs free energy difference between *a*-Si phase and crystalline phase. It is known (and we will show) that the crystallization leads to stress in the crystallization films [5]. The high stress accumulated during SPC decreases the driving force for grain growth. The stress in the polysilicon films can be measured by Raman scattering, in which tensile stress leads to Raman peak shifting to a smaller wave number. Higher stress leads to a larger peak shift, calculated by the formula [11] σ(MPa) = $-250\ \Delta\omega$(cm^{-1}), where $\Delta\omega = \omega - \omega_0$ with ω_0 = 519.5 cm^{-1}. Figure 5 (a) shows Raman spectra of 200nm-thick polysilicon films (annealed at 600 °C for 24 hr) in control region and cantilever regions, and a single crystalline silicon substrate, along with the Raman shifts and FWHMs in Fig. 5(b). Note that both of the polysilicon films are under tensile stress. The stress in the cantilever polysilicon films is half of the ~ 300 MPa in the control area. This may be the reason for the higher growth rate leading to larger grain size in the cantilever films [6].

The stress during SPC is due to inability of silicon atoms to freely rearrange near the a-Si/SiO_2 interface due to the bonding of *a*-Si atoms to the oxide, or due to volume contraction during *a*-Si to poly-Si phase transition [5]. The stress is largest at the *a*-Si/SiO_2 interface, where the nucleation preferably starts, as the silicon atoms in the *a*-Si are strongly bound to the surface atoms of the underlying SiO_2 layer after deposition. To relieve this tensile stress, crystalline defects (microtwins, dislocations, etc) develop during the nucleation and growth. When the

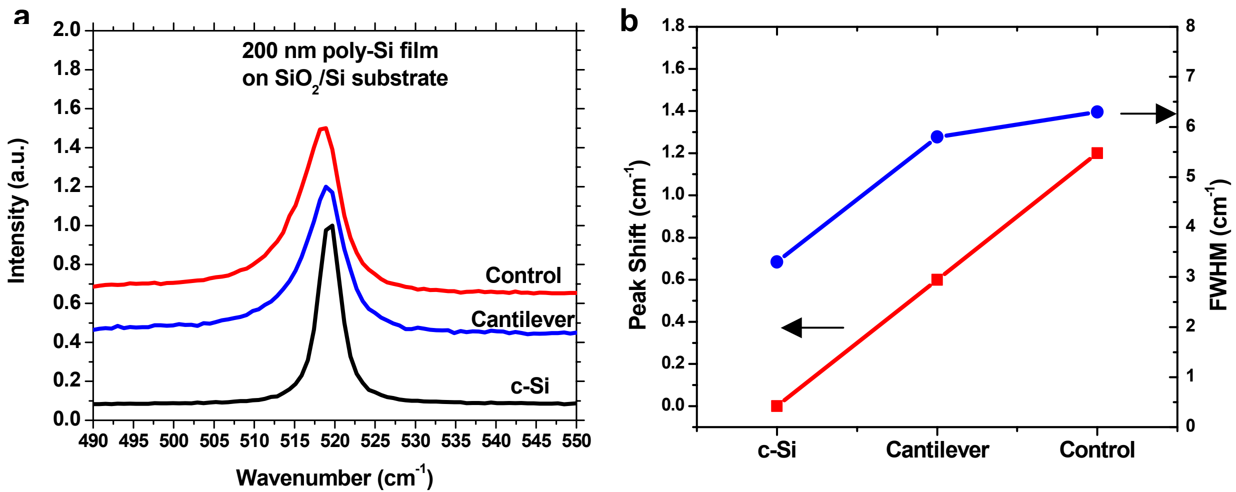

Figure 5. (a) Raman spectra of 200nm-thick fully crystallized polysilicon films in control and cantilever regions, and a (100)- orientated single-crystalline silicon substrate. (b) Raman peak shift and FWHM by fitting curve in (a).

underlying oxide is removed, silicon atoms can freely move themselves to form a crystalline lattice. As shown in Fig. 5(b), there is less stress in free-standing polysilicon films than in as-controlled films with an underlying oxide, leading to a lower intragranular defect density in the cantilever samples. It is also well known that small crystallites and high defect densities in polysilicon films cause asymmetry and broadening of the Raman spectrum due to phonon scattering from the microcrystallite boundaries and intragranular defects [12]. The defect scattering destroys the lattice translational symmetry and relaxes the momentum conservation rule during phonon-photon interaction, so that smaller size of the defect-free crystallite increases the Raman FWHM [13]. In Fig. 5(b), the values of FWHM of Raman spectra in various regions are: cantilever polysilicon region, 5.8 cm^{-1}; control polysilicon region, 6.3 cm^{-1}; and single-crystalline silicon substrate, 3.3 cm^{-1}. This narrower peak in the cantilever region suggests a lower density of intragranular defects compared with that in the control region in qualitative agreement with our TEM observations.

CONCLUSIONS

By removing the underlying oxide before annealing, the quality of polysilicon films crystallized from *a*-Si at 600 °C was greatly improved, with a 5× increase in the grain size and a 10× reduction in the intragranular defect density compared to a silicon film with underlying SiO_2. We hypothesize that this improvement is because the removal of the *a*-Si/SiO_2 interface results in a lower grain nucleation rate and an easier release of stress accumulated at the interface during SPC.

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