Silicon Epitaxial Regrowth Passivation of SiGe Nanostructures Pattered by AFM Oxidation

Xiang-Zheng Bo, Leonid P. Rokhinson, and J. C. Sturm
Center for Photonics and Opto-Electronic Materials, Department of Electrical Engineering
Princeton University, Princeton, NJ 08544, USA, Email: boxz@princeton.edu

ABSTRACT

SiGe quantum devices were demonstrated by AFM oxidation and selective wet etching with features size down to 50 nm. To passivate the devices and eliminate the interface states between Si/SiO_2, low temperature regrowth of epitaxial silicon over strained SiGe has been tested. The silicon regrowth on $Si_{0.8}Ge_{0.2}$ was done by rapid thermal chemical vapor deposition (RTCVD) at 700 ºC using a hydrogen pre-cleaning process at 800 ºC and 10 torr. SIMS analysis and photoluminescence (PL) of strained SiGe capped with epitaxial regrown silicon show a clean interface. Nano-gaps between doped SiGe filled and overgrown with epitaxial silicon show an electrical insulating property at 4.2 K.

INTRODUCTION

Si/SiGe heterostructures attract much interest in past due to their higher carrier transport mobility than that in Si MOSFETs [1-2]. Nanodevices on Si/SiGe are of growing interest. SiGe quantum dot devices may provide a physical route to achieve quantum computing [3-4]. However, how to fabricate a quantum dot with free from interface states is still a great challenge. Silicon quantum dots with MOSFET structures suffer from the interface states between Si (channel) and SiO_2 (gate oxide) [5]. Epitaxially grown strained SiGe on silicon can have a defect-free interface with atomic correspondence. Transport carriers can be confined by band offsets at Si/SiGe heterojunctions. The goal of our work is to apply them to fabricate “clean” quantum dot devices.

In this paper, we first show that SiGe quantum dots can be fabricated by AFM oxidation and selective wet etching. We then test the epitaxial regrowth of Si on strained SiGe to passivate the device with a maximum process temperature ≤ 800 °C, showing a “clean” interface.

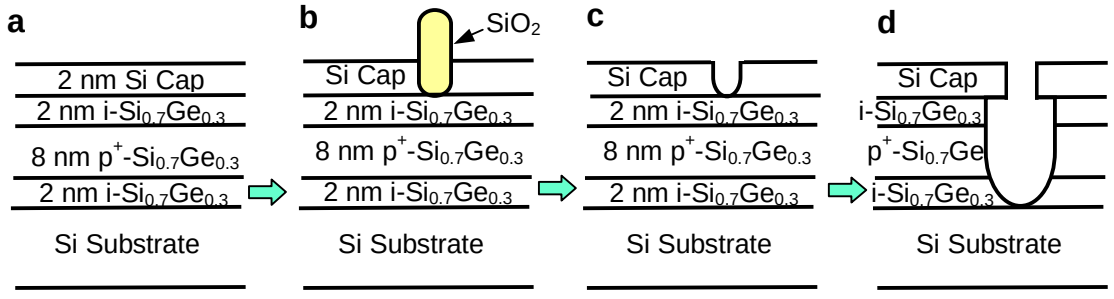

Figure 1. Process to pattern Si/SiGe nanostructures: (a) Layer structure; (b) Si cap AFM oxidation; (c) HF dip to remove SiO_2; (d) selective wet etching to pattern SiGe.

NANOPATTERING OF Si/SiGe BY AFM OXIDATION

Semiconductor nanodevices are usually patterned by electron-beam lithography and reactive-ion etching. However, these high-energy processes may induce defects which could affect nano-devices. AFM local oxidation with bias voltages smaller than 30 volts on AFM tip is a low-energy process and has a minimum feature width smaller than 20 nm on strained SiGe [6-7]. The maximum oxidation height on Si and SiGe is less than 3 nm, which means that layers with thickness greater 3 nm cannot be patterned. Therefore, the following nanopatterning technique (Figure 1) has been developed. A 2nm-thick silicon cap on strained $Si_{0.7}Ge_{0.3}$ was first oxidized by AFM, and then the pattern was transferred into Si and SiGe by selective wet etching of HF and a solution of HF: H_2O_2: CH_3COOH = 1: 2 :3 (vol.), respectively [8]. The minimum feature size increases to 50 nm due to the isotropic etching.

A SiGe quantum dot device with layer structure shown in Fig. 1(a) has been fabricated by AFM oxidation and wet etching. Figure 2(a) shows the dot structure after AFM oxidation with lateral gates insulated from the central dot structure. The holes in p^+-SiGe layer are prevented from tunneling into the silicon substrate by the valence band offset of ~ 220 meV at the heterojunction. Two narrow regions can form potential barriers for hole transport under the application of gate voltage, which also tunes Fermi-energy of the dot. The dot shows the conductance oscillation with gate voltage at T = 0.53 K (Fig. 2b), which may be due to a coulomb blockade effect [7]. Note that the device is open to air, and thus passivated by native oxide. The high densities of trapping/detrapping states at the interface cause the electrical characteristics not to be reproducible. To remove the influence of the surface, we seek to passivate the structure by epitaxial silicon regrowth.

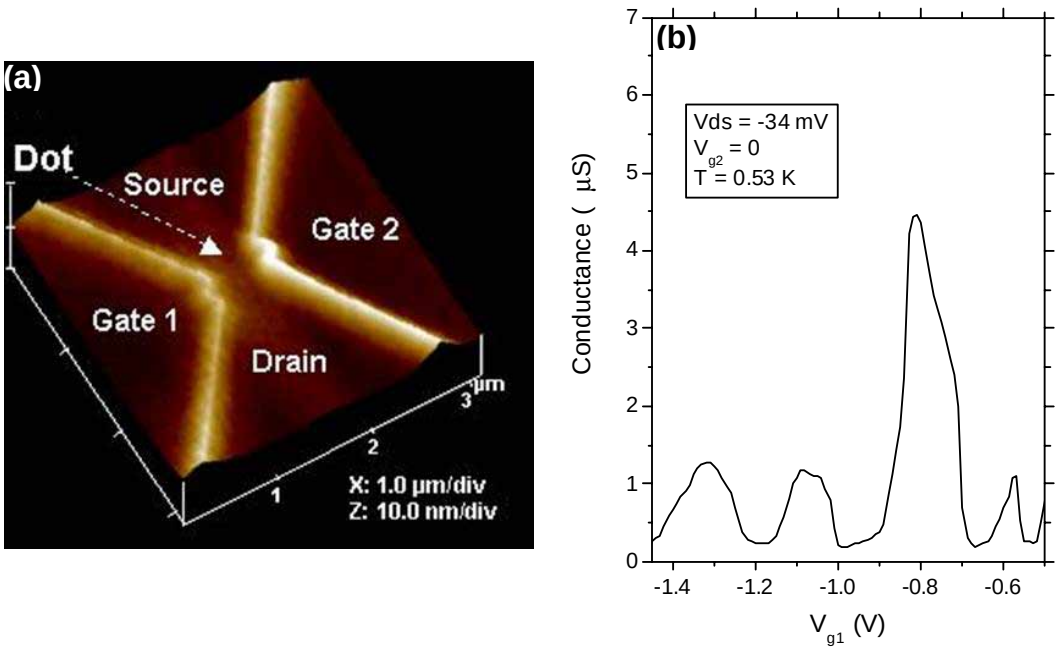

Figure 2. (a) AFM image of a SiGe quantum dot after AFM oxidation; (b) Differential conductance of the dot (after two-step wet etching) as a function of one planar gate voltage at V_{ds} = -34 mV and T = 0.53 K, showing coulomb blockade oscillation.

SILICON EPITAXIAL REGROWTH ON STRAINED SiGe

Preparing "clean" silicon surface for successive epitaxial growth is very important for high quality layer structures. Traditionally, CVD growth requires high temperature *in-situ* cleaning, such as hydrogen baking at 1000 °C, to remove contamination from the surface. Such temperatures are often unacceptable if the pre-existing devices have dopant profiles. Pre-cleaning process with low thermal budget has been studied by many groups [9-11]. Recently, Carroll *et al* [11] has achieved a carbon-free and oxygen-free silicon surface with hydrogen baking at 800 °C, upon which SiGe was then grown. However, less work has been done to clean SiGe for further Si growth.

In our experiment, after first growing a 1µm-thick silicon buffer at 1000 °C, psuedomorphically strained $Si_{0.8}Ge_{0.2}$ layer with thickness of ~ 20 nm was grown at 625 °C by RTCVD. The wafer was then unloaded from the CVD reactor, and left in a fume hood for ~ 24 hr. Before loading back into CVD chamber, the sample was chemically cleaned by mixture of H_2SO_4: H_2O_2 = 1: 1 for 15 min. and dipped in diluted HF with DI water (1: 1000) for 2 min [11]. The wafer surface was then cleaned by baking in hydrogen flowing at 3 lpm and 10 torr and temperature at 800 °C for 2 min. 100nm-thick silicon was successively regrown at 700 °C with dichlorosilane. Note that the diffusivity of boron in SiGe at 800 °C is ~ 4×10^{-17} $cm^{-2}s^{-1}$ [12]; thus the diffusion length is < 1 nm for 2 min. The boron diffusion is insignificant in our regrowth process. No patterning was done on this sample.

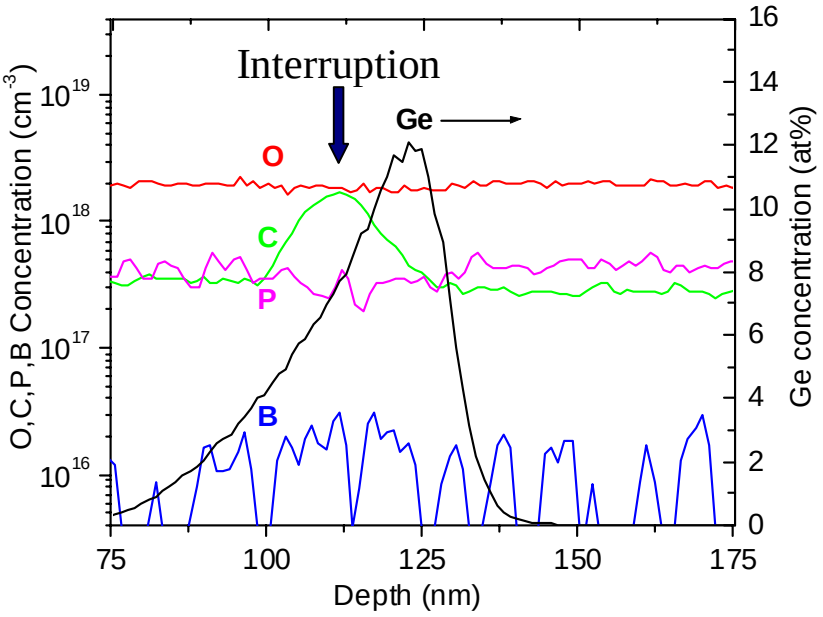

Figure 3. Oxygen, carbon, phosphorous, boron and germanium SIMS profile of a sample with epitaxial regrowth of silicon on strained SiGe layer. Before regrowth, an *in situ* hydrogen bake was at 10 torr and 800 °C for 2 min.

The interface quality of regrowth was characterized by secondary ion mass spectroscopy (SIMS) and photoluminescence (PL). SIMS was done at Evans East using a 3 keV Cs^+ primary ion beam. The carbon and oxygen detection limits are approximately 10^{17} and 10^{18} cm^{-3}, respectively. Figure 3 shows SIMS results on the regrown sample. At the interruption interface between SiGe and Si cap, no concentration increase of oxygen, phosphorous, and boron was detected, which means 800 °C is high enough to remove the native oxide on SiGe surface. The integrated carbon concentration at the regrowth interface was ~ 1.2×10^{12} cm^{-2}. This corresponds to < 0.1% of a SiGe monolayer.

Photoluminescence was performed at 77 K with a pump of an argon laser with λ = 514 nm and intensity on the sample of 10 W/cm^2. Most of excited carriers are generated at the silicon substrate, and then diffuse into SiGe quantum well. The luminescence intensity from strained SiGe quantum well is extremely sensitive to the carrier lifetime. Any defects or contamination at the interface will increase the non-radiative recombination rate, and thus decrease the luminescence intensity emitted from the strained SiGe. Therefore, the ratio of luminescence intensity from the SiGe over that from the Si is used to characterize the regrowth quality. In our CVD system, a SiGe quantum well grown without interruption and presumably with clean interface has the intensity ratio > 20 [11].

Figure 4 shows the PL spectra from the sample of regrown silicon on strained $Si_{0.8}Ge_{0.2}$ with a pre-cleaning temperature of 800 °C before the top Si layer. The two strong peaks are from SiGe TO phonon replica and no-phonon assisted transitions, respectively [13]. Both of them have 30 times greater intensity than that from the silicon TO peak, which indicates the regrowth interface between Si and SiGe is comparable to the “clean” system.

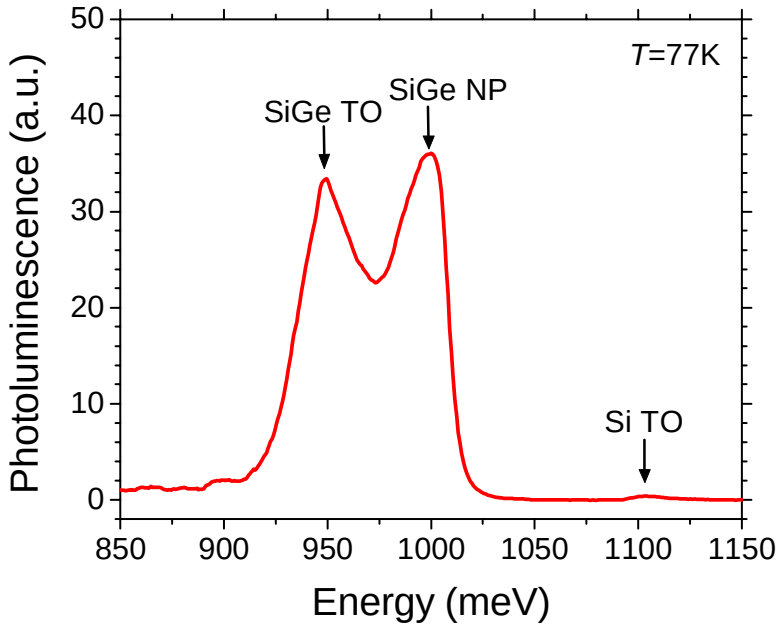

Figure 4. Photoluminescence spectrum at T = 77 K of regrown silicon on strained $Si_{0.8}Ge_{0.2}$. During regrowth, *in situ* hydrogen pre-baking was at 10 torr and 800 °C for 2 min.

ELECTRICAL NANOSTRUCTURE PASSIVATED BY Si REGROWTH

A simple nanostructure device to test the electrical effects of regrowth was fabricated by AFM oxidation and silicon epitaxial regrowth, using the layer structure of Fig. 1 (a), where the p^+-SiGe is the conducting layer in a Hall bar structure at 4.2 K. First, a nano-line was cut through a Hall bar (inset of Figure 5) by AFM oxidation and selective wet etching of the conducting SiGe. We previously demonstrated [8] that this breaks the electrical conducting of the Hall bar at 4.2 K. In this work, epitaxial Si regrowth at 700 °C was performed on this Hall bar with a hydrogen pre-bake at 800 °C. Electrical characteristics at T = 4.2 K of Hall bars with and without the cutting line are shown in Fig. 5. After the regrowth, the current in the structure increased, but for bias less than 2 V, the resistance is still > 10^4 times higher than that without cutting the line at all. The increase of the leakage current when the bias voltage $|V| > 4$ volts is attributed to the tunneling between p^+-$Si_{0.7}Ge_{0.3}$ and the regrown Si and is under further investigation.

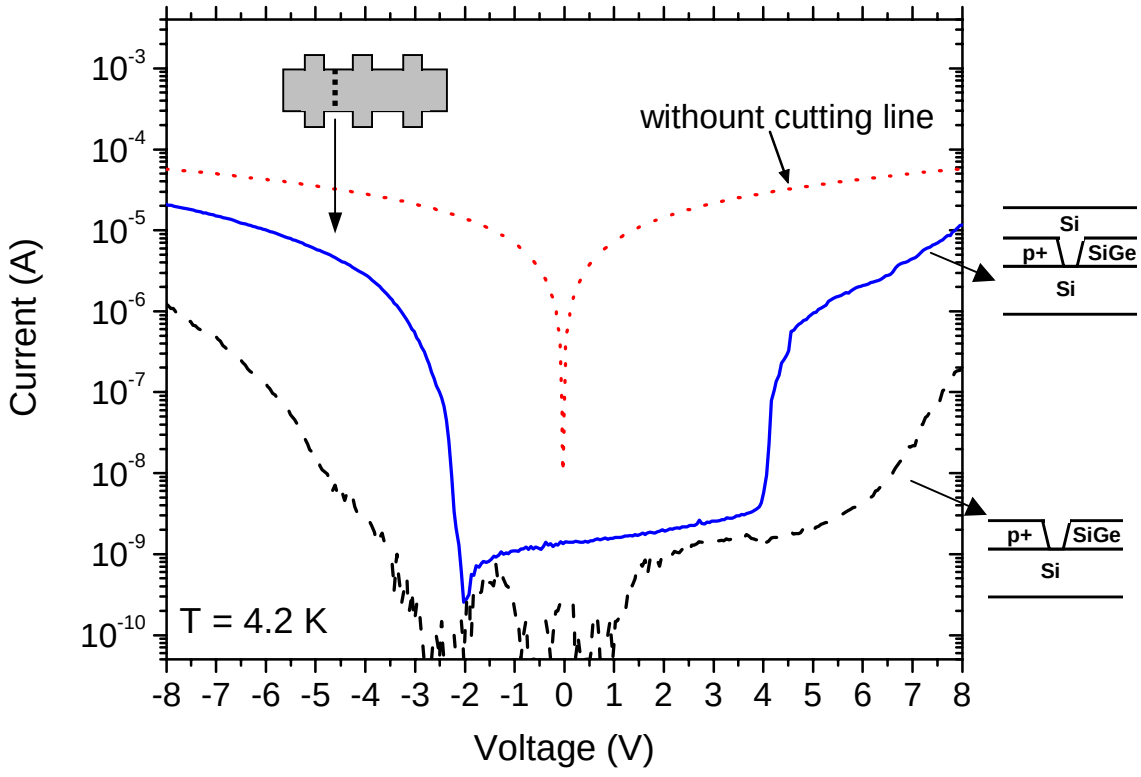

Figure 5. Electrical *I-V* curves at T = 4.2 K from the Hall bar (inset) without cutting line (dotted line), and with a cutting nano-line patterned by AFM oxidation and wet etching with (solid line) and without (dashed line) silicon regrowth at 700 °C.

CONCLUSIONS

A SiGe quantum dot was fabricated by AFM oxidation and selective wet etching. The dot exhibited coulomb blockade oscillation. To passivate the quantum devices, low-temperature silicon epitaxial regrowth on strained SiGe has been developed. SIMS and PL tests show the hydrogen baking at 800 °C and 10 torr is sufficient enough to remove the native oxide and most of the carbon at a SiGe surface before epitaxial Si regrowth. The interface quality between strained SiGe and Si overgrown at 700 °C is comparable to a clean interface grown without interruption. Electrical measurements demonstrate that the epitaxial regrowth of silicon on top of separate SiGe structures does not destroy the electrical isolation between them. This work suggests "clean" quantum devices can be fabricated by AFM oxidation and silicon epitaxial regrowth.

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REFERENCES

[1] K. Ismail, S. F. Nelson, J. O. Chu, and B. S. Meverson, Appl. Phys. Lett. **63**: 660 (1993).
[2] K. Rim, J. L. Hoyt, and J. F. Gibbons, IEEE Trans. Electron Devices, **47**: 1406 (2000).
[3] D. Loss and D. P. DiVincenzo, Phy. Rev. A **57**: 120 (1998).
[4] C. Tahan, M. Friesen, and R. Joynt, Phy. Rev. B **66**: 035314 (2002).
[5] L. P. Rokhinson, L. J. Guo, S. Y. Chou, and D. C. Tsui, Appl. Phys. Lett. **76**: 1591 (2000).
[6] E. S. Snow and P. M. Campbell, Appl. Phys. Lett. **64**: 1932 (1994).
[7] X.-Z. Bo, L. P. Rokhinson, H. Yin, D. C. Tsui, and J. C. Sturm, Appl. Phys. Lett. **81**: 3263 (2002).
[8] X.-Z. Bo, L. P. Rokhinson, H. Yin, D. C. Tsui, and J. C. Sturm, Proc. Mat. Res. Soc. Symp. **686**: A6.5 (2002).
[9] M. K. Sanganeria, M. C. Öztürk, K. E. Violette, G. Harris, C. A. Lee, and D. M. Maher, Appl. Phys. Lett. **66**: 1255 (1995).
[10] K. Oda and Y. Kiyota, *J. Electrochem. Soc.*, **143**: 2361 (1996).
[11] M. S. Carroll, J. C. Sturm, and M. Yang, J. Electrochem. Soc. **147**: 4652 (2000).
[12] M. S. Carroll, L.D. Lanzerotti, and J.C. Sturm, Proc. Symp. Mat. Res. Soc., **527**: 417 (1998).
[13] J. C. Sturm, H. Manoharan, L. C. Lenchyshyn, M. L. W. Thewalt, N. L Rowell, J.-P. Noel, and D.C. Houghton, Phys. Rev. Lett. **66**: 1362 (1991).