

SiGe Single-Hole Transistor Fabricated by AFM Oxidation and Epitaxial Regrowth

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Silicon single-electron devices are of great interest for future logic, memory and quantum computing. However, their usefulness is limited by the existence of traps related to the Si/SiO₂ interface, which interfere with the desired operation and lead to undesired characteristic features [1]. In this work, we report a new method for the fabrication of Si-based quantum dot device with an all low-energy patterning process based on AFM lithography (to avoid defects from e-beam and RIE) and Si/SiGe heterojunctions with epitaxial regrowth to confine holes in three-dimensions (to avoid Si/SiO₂ interface states). Single-hole transistor, which is the first reported SiGe quantum device with heterojunction passivation/carrier confinement, shows remarkably clean Coulomb blockade oscillations.

Figure 1 shows the nanopatterning process of Si/SiGe [2]. By applying a negative bias to a scanning AFM tip, a 2nm-thick Si cap was first oxidized [3]. The minimum feature size is < 20 nm. By the next two selective wet etching steps, 10nm-thick p⁺-SiGe, which is the only conducting layer at low temperature, was patterned. The SiGe structure passivated by low-temperature silicon epitaxial regrowth at 700 °C has been demonstrated to yield a clean interface of SiGe/regrown Si.

The device (Fig 1e) consists of a p⁺-Si_{0.7}Ge_{0.3} strained layer on Si, which was patterned by the process of Fig. 1. The valence band offset (~ 220 meV) confines carriers to the SiGe at low temperatures, so that they see no surfaces or potential traps. A single-hole tunnels from source to a dot through a narrow opening, where there is a potential barrier due to confinement effects and side-gate voltages, through the dot, and then through another barrier to drain. Due to over-etching, the final dot size is estimated < 100 nm. The side SiGe regions, separated by the etched pattern and regrown Si, serve as planar gates to modulate the dot and barrier potentials. Current flows when the dot energy levels are between the source and drain Fermi-energies.

Typical Coulomb blockade (CB) conductance oscillations are shown in Fig 2a at $T = 0.3\text{K}$ and $V_{ds} = 100 \mu\text{V}$ (both gates connected together). Most significantly, the oscillations are extremely clean and narrow (FWHM ~12 meV) (Fig 3), without spurious side peaks caused by oxide states [1]. With such a simple structure and initial results, the peaks are already among the best reported for any Si-based single electron device. For example, in our earlier work on similar unpassivated structures (no Si regrowth), the peak width was >100 meV at $T = 0.6 \text{K}$ [2]. The new device has peaks which are repeatable with different bias and temperature scans. The oscillation peaks are well fit by $G \propto \text{csh}^{-2}[\alpha(V_g - V_p)e / 2.5k_B T]$.

This indicates weak coupling between the dot and the source/drain ($\Gamma \ll k_B T \ll e^2 / C_{Total}$) [4]. A contour plot of conductance vs. gate and drain voltages shows the expected diamond shape from the loss of low conductance regions at higher drain voltages [4]. Work is in progress to quantitatively determine device parameters from Fig. 2 and 4, and to further improve the device characteristics (e.g. suppressed peak at 0.35V in Fig. 2).

In summary, extremely clean conductance oscillations have been observed in the first Si-passivated SiGe single hole device. This work was supported by ARO-MURI DAA655-98-1-0270 and DARPA.

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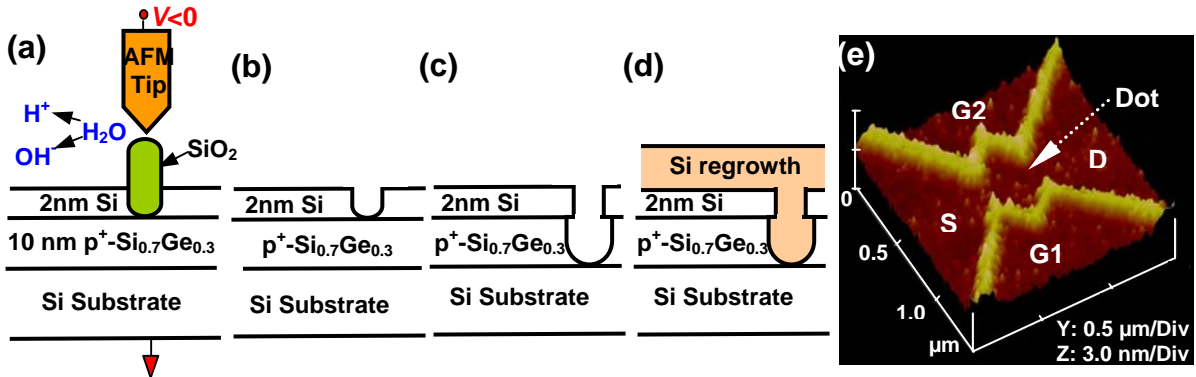


Figure 1. Nanopatterning process of Si/SiGe heterostructures: (a) Si cap AFM oxidation; (b) HF dip to remove SiO₂; and (c) selective wet etching to pattern SiGe layer; (d) silicon epitaxial regrowth. (e) Quantum dot device after AFM oxidation. S, D, G1,G2 indicate source, drain, side gates, respectively.

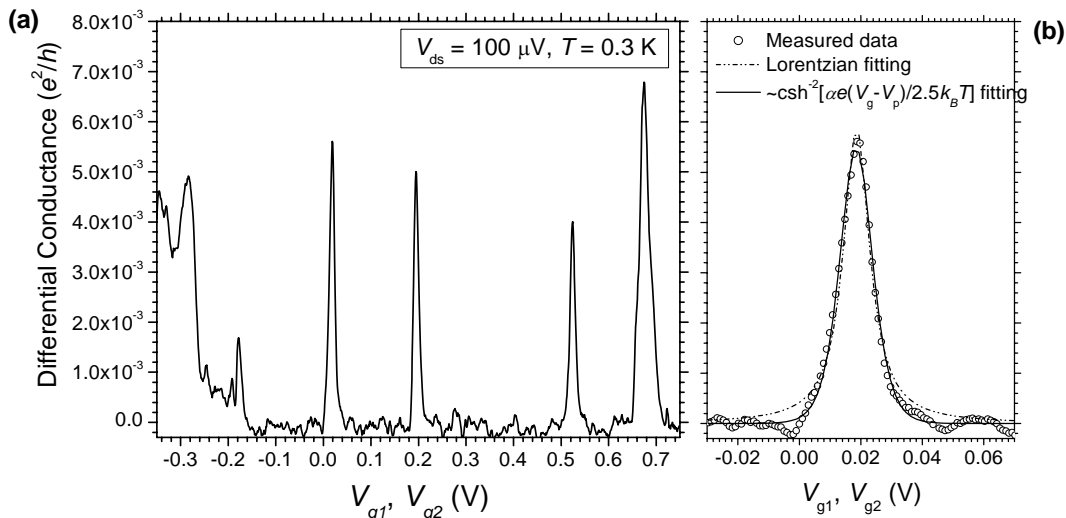


Figure 2. (a) Quantum dot conductance *v.s.* two connected gate voltages at source/drain bias of 100 μ V and temperature of 0.3 K; (b) conductance peak (scattered circle) at $V_g \sim 0.02$ V fitted to Lorentzian (dot line) and a thermal broadened CB resonance (solid line)

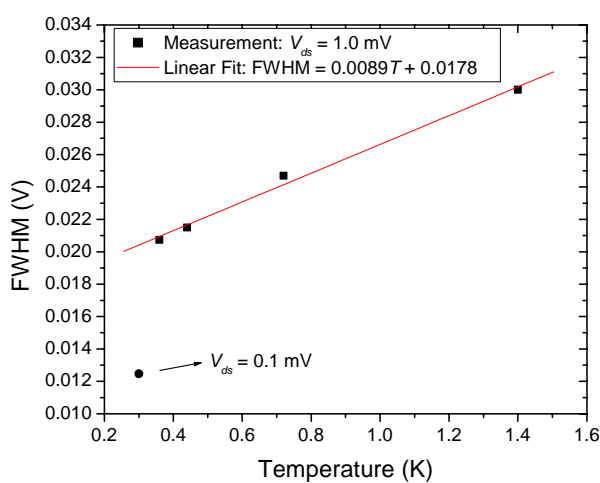


Figure 3. Temperature dependence of FWHM of conductance peak at $V_g \sim 0.02$ V and bias $V_{ds} = 1.0$ mV

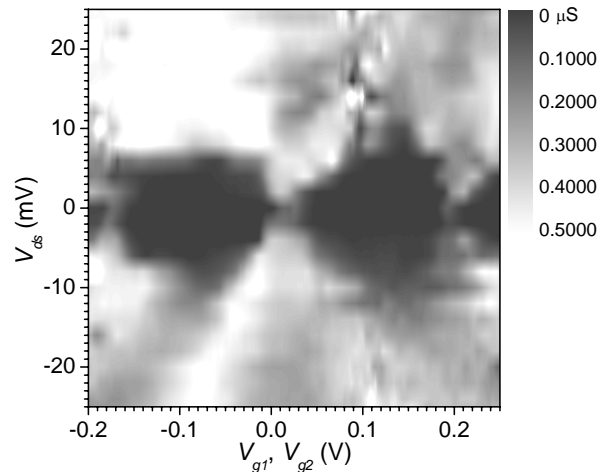


Figure 4. Differential conductance $\partial I / \partial V_{ds}$ on a linear gray scale as a function of V_{g1}, V_{g2} for different bias voltages of V_{ds} . Edge bluntness is thought to be due to the noise from gate voltages.