DEFORMABLE ELECTRONIC SURFACES

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In this paper a technological approach for the fabrication of deformable electronic surfaces is reviewed. The approach consists of the fabrication of thin film devices on a flat but deformable substrate such as a plastic or glass foil using conventional processing tools. After the fabrication, the foil can be deformed to other shapes by air pressure or stamping. A spherical cap shape is used as a model system. This deformation induces large stress in the substrate, which is plastically deformed. To avoid damage to the thin film devices, they are built on top of "hard" islands, which limit the strain in the devices to manageable levels. Amorphous silicon TFT's on silicon nitride islands show little qualitative change in characteristics after a plastic deformation of the substrate to strain levels over 5%. Interconnect lines between islands are subjected to a large strain if they are deposited and patterned before the substrate deformation, and require novel approaches.

1. Introduction

Microelectronics and conventional large-area electronics (e.g. flat panel displays) are fabricated on flat rigid surfaces such as semiconductor wafers or glass. There is a large interest, however, in having an integrated electronic functionality over large-area surfaces which have a three-dimensional shape. Applications of such surfaces include displays on furniture, spherically-shaped focal "plane" arrays, intelligent medical bandages, and sensor skins for robots [1-3]

To create such integrated electronics, one could fabricate devices directly on a complex surface, or first fabricate the electronics on a planar surface and then deform the planar surface into a 3-D shape. This paper reviews the latter option. TFT's are first fabricated on a thin deformable foil substrate, which is subsequently deformed into a spherical dome shape as a model system. Large strains are induced which will permanently damage devices if not properly engineered. Section 2 of this paper describes the approach of hard islands on a soft substrate to address the strain issue. Section 3 discusses the effects of strain induced from deformation on the TFT's. Section 4 addresses the issue of metallization between the device islands, and presents simple circuit results. Finally, Section 5 describes some future directions of this technology.

2. Deformation, Strain, and its Mitigation

Recently several groups have demonstrated thin film devices (amorphous silicon TFT's, organic LED's, …) on flexible substrates[4-9]. In these cases, the demonstrated flexibility is the cylindrical deformation, e.g. rolling of the substrate. Fig. 1(a) shows a cross section of such a substrate. In this case, the outer surface is in tension and the lower surface is in compression, with the magnitude of the surface strain ε is given by $\varepsilon = t/2\rho$, where t is the substrate thickness and ρ is the radius of curvature. For a given radius of curvature, the strain can be reduced by simply reducing the substrate thickness. For example, for a radius of curvature of only 2 mm, the strain can be reduced to 0.5% by reducing the substrate thickness to 20 microns. At the level of 0.5% strain, most inorganic device materials (e.g. silicon, silicon nitride, etc.) will not crack, but for substantial higher levels of strain, films will crack leading to permanent device

failure. Indeed, using plastic and metal foil substrates as thin as 25 microns, TFT's have been deformed to a radius of under 2 mm with no permanent effects [4, 9].

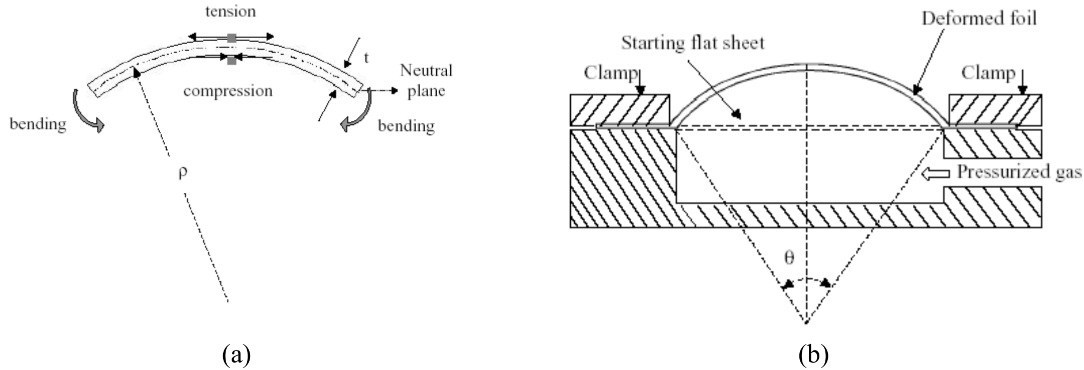


Fig. 1. (a) schematic diagram of strain components in thin film substrate under cylindrical deformation, and (b) schematic approach for spherical deformation of electronics first fabricated on thin foil substrates.

In this work, devices on a planar foil substrate are deformed into a spherical cap shape by clamping the foil around a circular perimeter (6-cm diameter), and then applying gas pressure to one side of the foil (Fig. 1(b)). Both plastic (Kapton ®) and stainless steel foils are used with thicknesses of 50 microns and 12-25 microns, respectively. Typical pressures are 20-50 psi, and as a goal we seek the angle subtended by the dome after pressure is released to be on the order of ~ 65° (height at center of ~9 mm) corresponding to one steradian of solid angle subtended by the dome. For steel, the deformation depends critically on pre-annealing to adjust the polycrystalline grain size [10]. One notes in Fig. 1(b) that both the top and bottom surface of the foil have an increased length compared to that before deformation. The entire foil is in tension, and to first order the strain cannot be reduced by reducing the substrate thickness. Thus, spherical deformation is fundamentally a much harder problem than cylindrical deformation, and cannot be solved just by using thinner substrates. A critical point is that to first order, the problem is caused by the tensile strain due to the increased arc length of the foil, not by the curvature, as was the case with cylindrical deformation. Thus, the problem is not one of curvature, but of simple stretching.

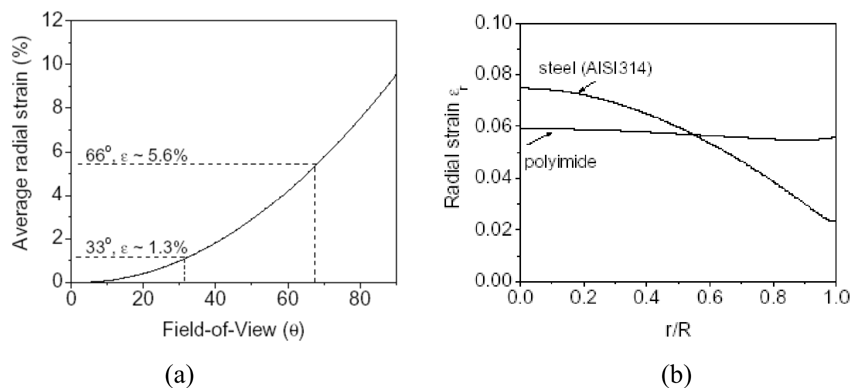


Fig. 2. (a) Average radial strain vs. field of view (angle θ) for spherically deformed foils (from geometric calculations, Eq'. (1)) and (b) radial strain vs. radius r for actual foils calculated by numerical mechanical modeling. R is the radius of the clamped region [10].

We will use this spherical cap shape as a model system to explore the fundamental materials issues associated with deformable electronic surfaces. The average radial strain across the surface of a foil deformed into a spherical cap shape can be shown by geometrical considerations to be

$$\varepsilon_{r,avg.} \approx \frac{\theta^2}{24} \approx \frac{2}{3}\left(\frac{Rh}{R^2+h^2}\right)^2 \quad (1)$$

where θ is the angle subtended by the cap (Fig. 2), R is the foil radius before deformation (3 cm), and h is the height of deformation at the center. For an angle of 65°, the average tensile strain is near 5%, which is beyond the failure point of most inorganic materials. The exact strain distribution depends on the material involved and its stress-strain relationship (Fig. 2(b)). Fig. 3 shows images of an 0.5-µm silicon dioxide film (spin-on-glass) on a stainless steel foil, and of a 0.1-µm amorphous silicon (a-Si) film on top of 0.4-µm silicon nitride (SiN) (both deposited by PECVD) on a polyimide plastic substrate (Kapton ®), both after deformation to a ~65° field of view. Both films have cracked, but one notes that the intact regions on the plastic substrate are about five times larger than those on the steel substrate (25 vs. 5 microns, respectively).

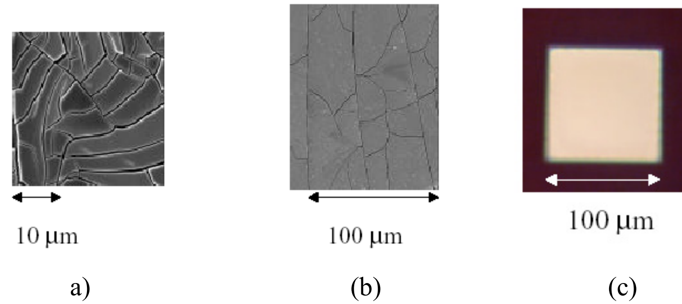


Fig 3. Image of three structures after deformation to 65° field of view: (a) 0.5-µm silicon dioxide on 25-µm stainless steel foil, (b) 0.1-µm a-Si on top of 0.4-µm Si_3N_4 on top of 50-µm of Kapton® polyimide, and (c) the same sandwich on polyimide but patterned before deformation.

This suggests that by patterning the inorganic device films before deformation, one might be able to avoid their cracking from the deformation. This concept of a "hard" island on a "soft" substrate was then explored in detail. Because the problem is one of stretching, not curvature, one can think of the deformation as elongating the film (Fig. 4(a)). A soft substrate can undergo elastic deformation (with low Young's modulus) or plastic deformation (with low yield strength). A "hard" device island (inorganic device materials with high Young's moduli) will tend not to deform, therefore, the strain will be higher than average in the areas between the device islands. Kapton® has a low Young's modulus (~ 5 GPa) compared to that of device materials (a-Si and SiN), ~100 GPa). While one might not think of stainless steel as soft, with annealing it can have a yield stress on the order of only 0.1 GPa [Hsu, JAP]. In contrast, we have found the failure stress for cracking in device structures with a-Si and SiN to be over 0.5 GPa.

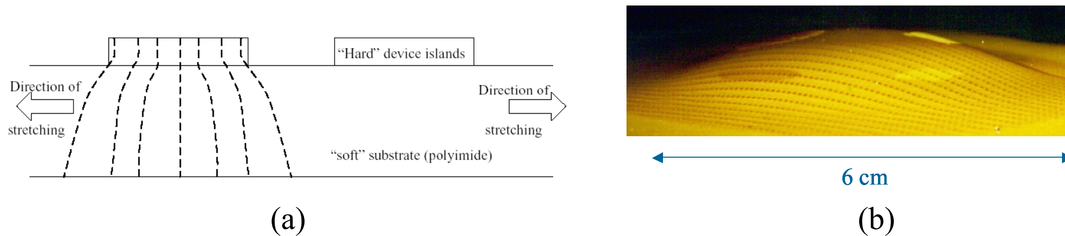


Fig. 4. (a) Island concept for realizing devices on hard islands on soft deformable substrates and (b) image of Kapton® film deformed to ~65° field of view with a-Si/SiN islands [10].

By patterning the a-Si/SiN layers before deformation, islands of sufficiently small size do not crack after deformation (Fig. 4(c). For room temperature deformation, only 20-µm square islands remained intact – larger islands were all cracked (Fig. 5(a)). The temperature during the deformation process was then raised to 150 ^{o}C because the polyimide softens considerably at that temperature, while there is little effect on the mechanical properties of the device layers. 50-µm islands could then be achieved, and even a few islands as large as 100-µm survived. It was expected that for a high surface coverage of islands, cracking would start at a smaller island size. This was not observed, however, up to surface area coverages of islands of 44%.

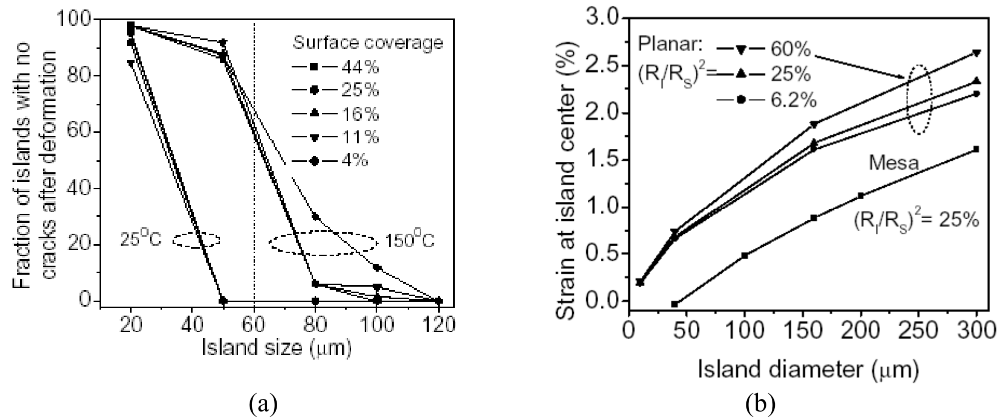


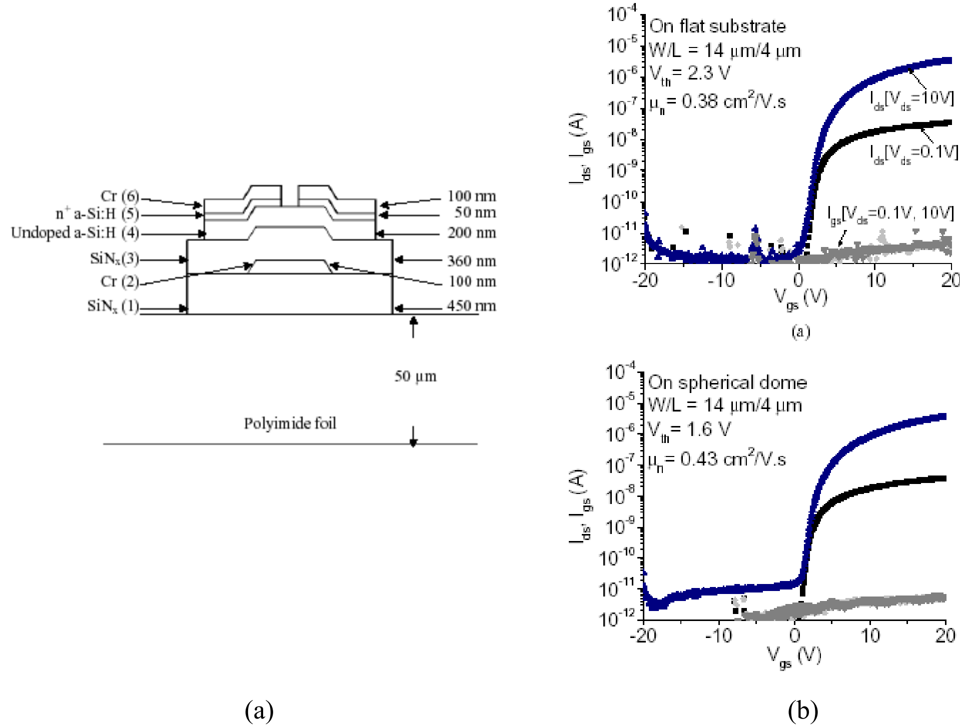
Fig. 5. (a) Yield of square planar islands with no cracks as a function of island edge length for a structure of 0.1-µm a-Si on top of 0.4-µm SiN on top of 50-µm polyimide (Kapton®), for room temperature and 150°C deformation to a spherical cape shape with a field of view of ~65° with island surface coverages up to 44% (b) Maximum strain in islands by finite element modeling in round islands as function of diameter for 6% stretching (corresponding to ~65°C field of view) at room temperature, for up to 60% surface coverage. Also shown is strain vs. island size for mesa islands where the polyimide was etched 10-µm deep around the island. [10].

Finite element modeling of the stretching of a single island was performed using 150 ^{o}C parameters for the polyimide. The effective surface coverage of islands was varied by changing the distance from the island edges to the circumference where the stretching force was applied. Round islands were modeled for simplicity, with surface area coverages up to 60%. The modeling shows that the strain is largest at the center of the islands, and that this maximum strain level increases with the island size (Fig. 5(b)). By comparing the onset of failure in the islands in experiments (25-µm island edge length) to simulations (25 micron island diameter), one finds the expected maximum strain the island can withstand before failure is ~0.5%. The lack of dependence on the spacing between islands was found to be due to the plastic deformation of the substrate. Once the plastic deformation condition is reached, it takes little further stress to induce a larger deformation. Therefore, the substrate plastically deforms fairly easily between the islands, and there is little strain change in the island itself as the spacing between the islands becomes smaller (increasing island coverage).

Two additional modifications can be used to further increase the maximum island size. These are etching the polymide into a mesa structure (e.g. 10-µm deep) around the island to further decouple the island from the substrate, and using a thicker SiN buffer layer to increase the island strength. For the same a-Si/SiN stack as above, the mesa process allowed room temperature deformation with intact island sizes up to 90 µm, vs. only 20 µm with the planar island process [10].

3. Effect of Deformation on Transistor Performance

Before deformation, staggered bottom-gate back-channel-etch amorphous silicon TFT's were fabricated using the a-Si layer on top of the 0.4-µm SiN buffers (Fig. 6(a)) on 50-micron Kapton®. The process was typical of that used by other researchers in the area of amorphous silicon TFT's on plastic [11]. The maximum process temperature was ~150 °C and the gate material (SiN) was deposited in the same pumpdown as the a-Si. The devices were placed on SiN islands etched down to the substrate. All contact pads were put on the islands, and no device materials or metallization extended off of the islands.



(a) (b)

Fig. 6. (a) Cross section of a-Si FET's on SiN islands on polyimide and (b) I-V curves for the same FET before deformation and after plastic deformation at 150 °C to a spherical cap shape with field of view of ~60° [12, 13].

First substrates were deformed to a maximum average strain level of 3%, and then pressure was released. The deformation was elastic in this case, so that the substrate returned to its flat shape, and no significant changes in the FET mobility were observed. In islands without cracking, there was nothing remarkable about the TFT's after deformation. After a larger deformation at 150 °C resulting in plastic (permanent) substrate deformation, devices on average exhibited an 8% mobility increase [12]. The leakage current (<10 pA) and subthreshold slopes (~550 mV/decade) were roughly unchanged (Fig. 6 (b)).]. The estimated strain at the island center (from mechanical modeling) is 0.3% biaxial tension. Tensile uniaxial strain is known to increase the mobility of a-Si FET's, although the mechanism is not understood, and data is lacking on the effect of biaxial (vs. uniaxial) strain [14, 15]. This is unlike the case with crystalline silicon, where piezoresistive effects have been extensively explored both theoretically and experimentally in bulk transport and in FET's. Further work is necessary to quantitatively understand the effects of strain on amorphous silicon TFT's.

4. Interconnections and Circuits

There is a large increase in the average length from one side of the substrate to the other after plastic deformation (e.g. 5%). On the other hand, the island approach limits the expansion to <1% in the islands. Thus, the expansion between the islands must be very large. In the case of square islands, with a spacing between the islands equal to the edge length of the square, the spacing between the islands increases by twice the average amount if the strain in the islands is small. Thus, for our model system, the interconnects would undergo ~10% expansion. In all cases this led to cracks in metal interconnect lines between islands (Fig. 7(a)).

To create interconnects using conventional materials, it was necessary to deposit the metal after the deformation process. Normally, this would require lithography to be done on the curved and deformed surface, which would be a technological challenge. Therefore, an alternative process was developed. After the transistor fabrication on islands but before deformation, photoresist was spun-on and patterned to pattern a single metal layer by "lift-off" (Fig. 7). The substrate was then deformed to a spherical cap shape with ~5% average strain. The photoresist was soft and deformable enough that it did not crack between islands despite the large strain in that region. Aluminum was then evaporated onto the curved surface, and was patterned by lift-off. In this way, the cracks in the aluminum could be avoided, and interconnects between devices in separate islands could be fabricated.

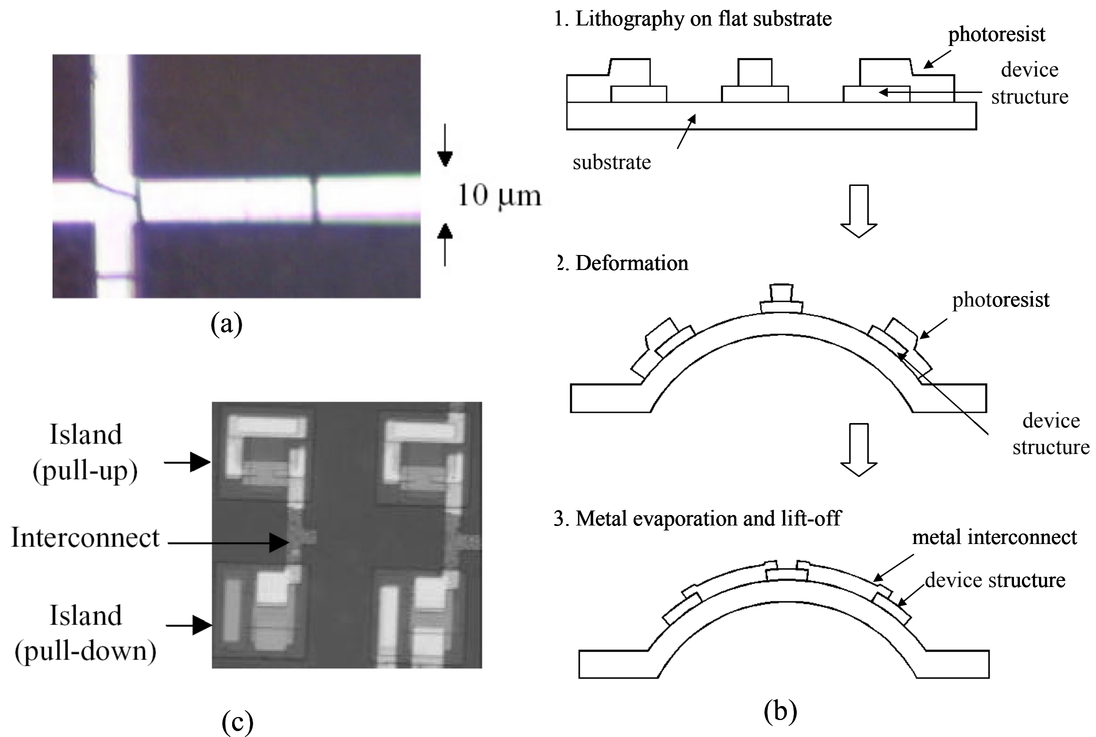


Fig. 7. (a) image of cracked interconnect line after expansion to ~5% average strain, with metal deposited and patterned before expansion; (b) lift-of f process for interconnections between islands with photoresist patterned before deformation and aluminum evaporation after deformation; and (c) image of interconnects between islands in inverter circuit [13].

This approach for metal interconnect fabrication is limited to a single level of interconnects. As a minimum, in many array circuits, two levels of metallization are desired – one each for row and column lines. One approach towards full metal interconnects in both horizontal and vertical directions with a single level of metallization in the highly-deformed region is shown in Fig. 8. The row and column lines are made out of the same single level of metallization, which is deposited after deformation by liftoff patterned before deformation as in Fig. 7. The cross-overs of the row and column lines is done using multiple levels of metal on the hard islands. Multiple levels of metal in these islands can be deposited and patterned by conventional lithography before deformation, because the strain in these islands is small.

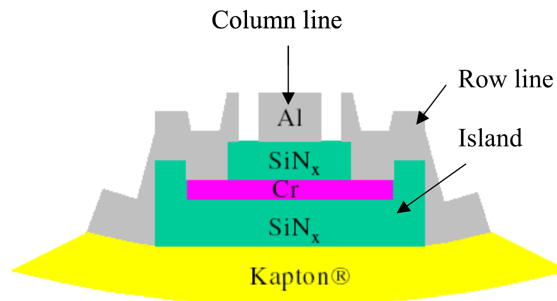


Fig 8. Crossover approach for x-y matrix with single level of metal in the highly deformed region between islands. [16].

5. Future Directions and Summary

This paper has demonstrated a technology path towards electronics on deformable surfaces which does not require lithography on curved surfaces Shapes other than rolled foils (cylindrical deformation) and cones are inherently harder to create because of the large strain created by the deformation. The approach shown in this paper uses hard islands on soft substrates to minimize the strain in device materials on the islands, and was demonstrated with a-Si TFT's on plastic foil substrates. The level of strain between islands is higher than the average level, which makes the fabrication of interconnects difficult if they are deposited before the deformation.

There are several directions for future work. The first is development of different devices besides FET's on the device islands. For example, organic LED's on hard islands have recently been shown to withstand deformation to dome-type shapes [17]. A second goal would be more complicated circuits spanning several islands, beyond the simple inverters we have demonstrated to date. Finally, the work shown in this paper described FET's on substrate foils which were deformed once, not multiple times. An exciting goal would be a three-dimensional surface which could be deformed multiple times. Such deformation would place a severe requirement on the interconnects, as they would then be subjected to a high (and changing) level of average strain, which would crack interconnects deposited by conventional processes and lead to open circuits. Several groups have recently developed interconnect structures which can withstand high strain, with stretching levels of up to ~100% [18-21]. Such types of interconnects would allow the development of a deformable electronic surface with many types of applications.

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