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Nanopatterning of Si/SiGe Two-dimensional Hole Gases by PFOTS-aided AFM Lithography of Carrier Supply Layer

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ABSTRACT

The nanopatterning of Si/SiGe layers by PFOTS (perfluorooctyl trichlorosilane) -aided AFM (atomic force microscopy) lithography is demonstrated. We use self-assembled PFOTS monolayers as a resist for AFM exposure and then transfer patterns in to underlying SiGe layers by a two-step selective wet etching. Minimum linewidths of 100nm can be achieved with improved uniformity and repeatability compared to AFM lithography without PFOTS. This lithography technique was used to pattern the carrier supply layer in Si/SiGe 2-D hole gases to localize holes for epitaxially passivated quantum dot applications.

INTRODUCTION

For Si-based quantum dots for single-electron devices, dots with zero surface states are desirable, since one surface state can greatly alter a single electron device. This is difficult to achieve with oxide passivation. We have previously shown the approach of defining SiGe quantum dots for holes by AFM lithography and wet etching (to avoid radiation damage defects from e-beam and RIE) and epitaxial regrowth of Si to passivate the SiGe dot surface with ideally zero interface states [1]. This work was limited, however, by fact that (i) lithography and pattern transfer from AFM oxidation by wet etching were very non-reproducible, and (ii) the inevitability of interface contamination on the dot surface during regrowth, resulting in defect states. In this work, we report two significant advances to overcome these limitations: (i) the use of a self-assembled monolayer PFOTS [2] as an etch resist to improve the uniformity and repeatability of AFM lithography and pattern transfer, and (ii) the patterning of the carrier supply layer of a 2-D hole gas (2DHG) by this method, rather than the SiGe conducting layer itself, so that a dot in the SiGe can be achieved without ever exposing its surface.

AFM lithography can be used to pattern Si (or SiGe) by anodic oxidation of silicon under the tip with applied negative voltage [3]. Because the oxide thickness is limited to ~4nm, only about 2nm silicon in thick can be oxidized [4]. To pattern thicker SiGe layers, a two-step wet etching can be used (Fig. 1). A thin silicon cap op top of the SiGe is first oxidized by AFM, then with a dilute HF dip to remove the oxide, followed by a selective wet etching (CH_3COOH: H_2O_2: HF=1:2:3) [5] to transfer the pattern into underlying SiGe. This is difficult to control in practice since the thin silicon is not a perfect barrier for the selective etching.

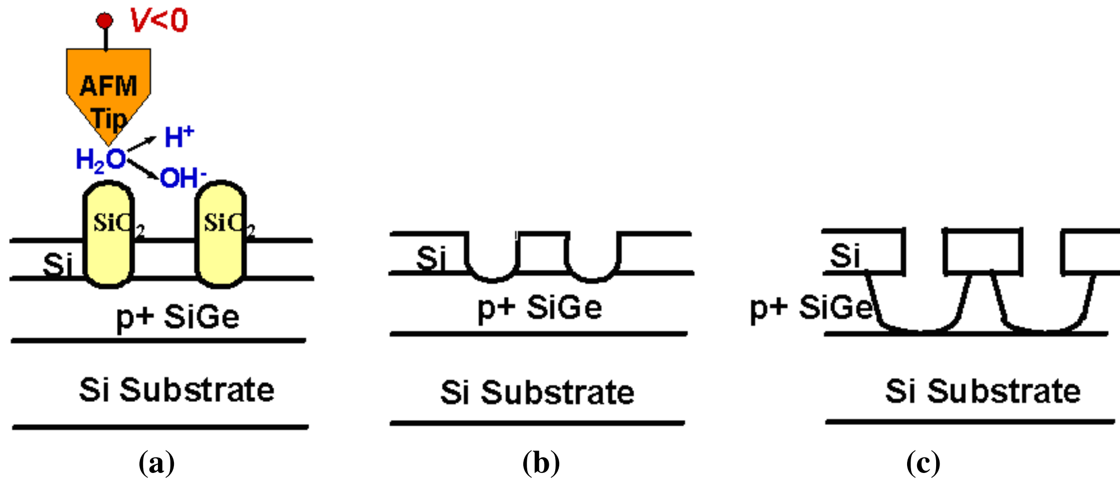

Figure 1. Process of nanopatterning Si/SiGe layers with two-step wet etching: (a) AFM local oxidation, (b) Remove oxide by HF, (c) SiGe selective wet etching.

In this paper we add self-assembled PFOTS monolayers on top of the silicon before AFM oxidation. The AFM process can oxidize the silicon through the organic resist, and the patterned PFOTS serves as a resist for the later SiGe wet etching. Previous work has shown that the AFM can oxidize though both PFOTS and thin silicon layers [6].

EXPERIMENT

Preparation of self-assembled monolayer films

Recently there has been considerable interest in the reaction of n-octadecyltrichlorosilane (OTS) with silicon to form self-assembled monolayers [7]. PFOTS is used in our work. Since only a 2-nm silicon surface layer will be oxidized by AFM oxidation, ultrasmooth PFOTS monolayers need to be obtained before the AFM lithography. We first removed native oxide on silicon substrates by an HF dip. Then the silicon substrates were heated in a 1:3 solution of hydrogen peroxide and sulfuric acid at 80 ^{o}C for 30 min, to provide a smooth oxide surface for the film growth. This acid treatment was followed by an extensive DI water rinse and nitrogen blow dry. For growth, the substrates were immersed at room temperature in a 1mM solution of PFOTS in dodecane for 3 hours in a nitrogen glove box environment with minimal exposure to the ambient. The long immersion time can ensure a complete monolayer formation [2]. After growth of the self-assembled monolayers, the surface roughness was measured by AFM to be 1.8Å. The monolayer thickness is estimated to be ~2.6nm.

AFM lithography of Si/SiGe heterostructures

AFM lithography was performed on PFOTS-coated substrates at room temperature in tapping mode. The relative humidity was kept at ~40% by bubbling nitrogen through water into an environmental chamber surrounding the scanning tip. By applying a negative bias (~ -20V) to the tip at a scanning speed of 0.4μm/sec, a 2-nm silicon surface layer underlying the PFOTS is

locally oxidized. Linewidths well under 100 nm can be achieved. By a dilute HF dip and a selective SiGe wet etching ($HF:H_2O_2:CH_3COOH$ = 1:2:3), the pattern is transferred to the underlying SiGe layer and stops at the silicon layer (Fig. 2). Figure3 shows a pattern of Si/SiGe by the PFOTS-aided AFM lithography. The FWHM of the linewidth is on the order of 100nm, which is comparable to the resolution of AFM lithography without PFOTS. High-resolution can be achieved by optimizing the bias voltage and writing speed [8].

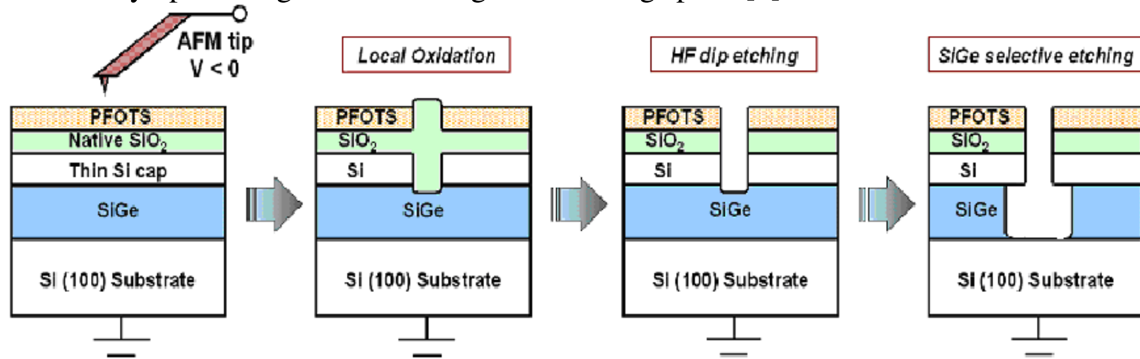

Figure 2. Process of PFOTS-aided AFM lithography. PFOTS is deposited on native oxide (for bonding) to prevent etching through 2-nm silicon surface layer during SiGe patterning for improved uniformity. The two-step etching process is used to pattern SiGe thicker than ~ 2nm.

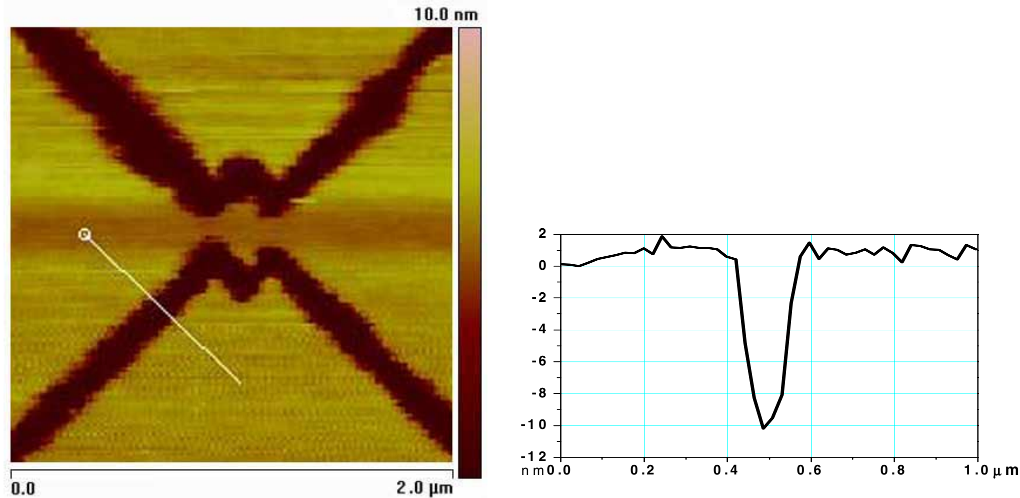

Figure 3. Surface image and profile along the labeled white line of a pattern of Si/SiGe by the PFOTS-aided AFM lithography, showing a minimum linewidth on the order of 100nm.

Compared with the previous direct AFM lithography of Si/SiGe layers, the use of PFOTS monolayers as an etch resist greatly improved the pattern transfer uniformity and repeatability. When only the thin silicon cap layer itself was used as the selective etch barrier, the pattern transfer from AFM oxidation by wet etching were very non-reproducible, and the etch was limited to a short time (~ 20 sec). An increased surface roughness after the wet etch was also observed. With this additional PFOTS film as a resist, now the selective etch can be several minutes long, so now thicker SiGe layers with lower Ge content can be patterned with far

improved uniformity than without PFOTS. Figure 4 shows a comparison of the etching profile without and with additional PFOTS. When etching time is 40 seconds or longer, undesirable pinholes were found on the silicon surface without PFOTS.

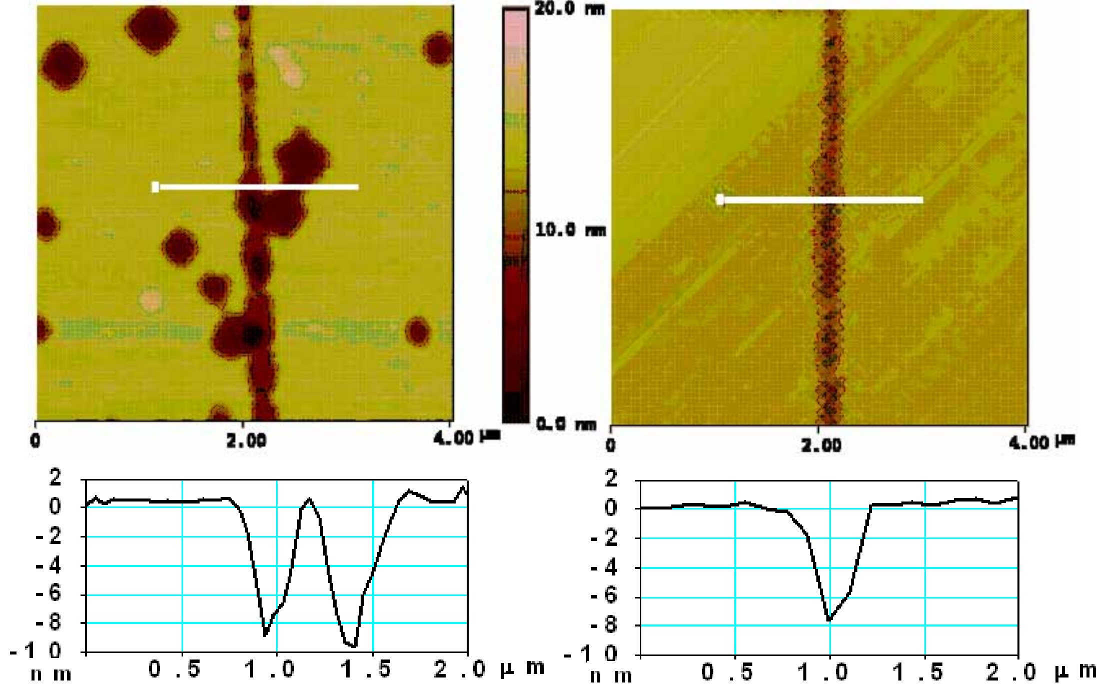

Figure 4. Surface image and profile along the labeled white line for a Si/SiGe patterned with (right) and without (left) PFOTS as a resist, the HF dip to remove silicon oxide and the SiGe selective wet etch for ~40 sec.

Growth and patterning of Si/SiGe 2D hole gases

The 2-D hole gases were grown by rapid thermal chemical vapor deposition [9]. A 15nm strained $Si_{0.7}Ge_{0.3}$ was grown on top of silicon buffer as the 2-D gas channel. A 10nm boron doped $Si_{0.9}Ge_{0.1}$ is used as the carrier supply layer with a setback of 8nm Si from the $Si_{0.7}Ge_{0.3}$ quantum well. The Si and SiGe layers were grown at 700 ^{o}C and 625 ^{o}C, respectively. The supply layer was made of $Si_{0.9}Ge_{0.1}$ as opposed to the usual Si, because this enables the later removal of only the $Si_{0.9}Ge_{0.1}$ supply layer without removal of the barrier Si layer. Ohmic contacts are made to the 2DHG by aluminum evaporation and subsequent annealing at 450 ^{o}C. The mobility and hole density are 1300 cm^2/Vs and $6\times10^{11}cm^{-2}$ at T=4.2K.

The PFOTS-aided AFM lithography was used to pattern the carrier supply layer in Si/SiGe 2-D hole gases, with a goal of creating dots by laterally localizing the holes into a dot by removing the supply layer outside the dots. The 2-D hole gas is localized according to the supply layer patterns. Previously, with the SiGe layer patterned, epitaxial regrowth was necessary to passivate the SiGe dot edges [10]. In this new approach (Fig. 5), with only the doped supply layer patterned, throughout the whole process the dot surface (location of holes in the SiGe) is not exposed, since it is still covered by the undoped Si barrier layer. This avoids the potential creation on defects of the surfaces of the resulting quantum dots. This approach should eliminate the requirement of subsequent epitaxial regrowth to passivate the dot surfaces.

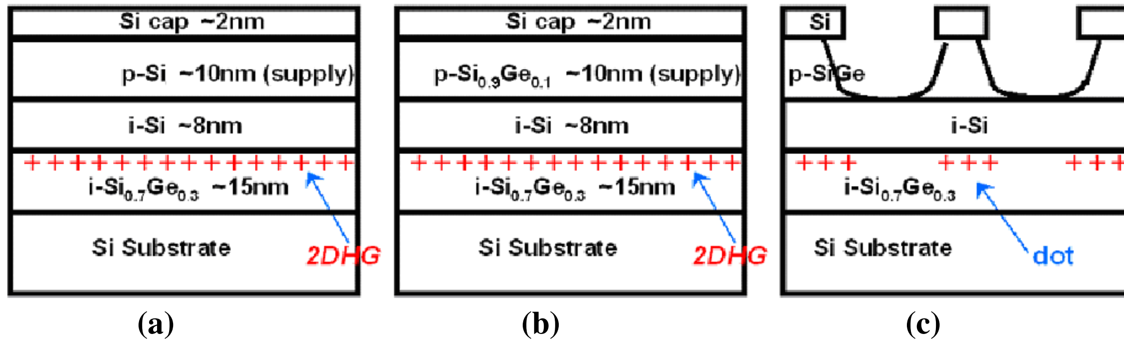

Figure 5. Schematic structures of (a) a typical 2D hole gas in strained $Si_{0.7}Ge_{0.3}$ on Si(100) substrate, (b) modified 2D hole gas structure with $Si_{0.9}Ge_{0.1}$ supply layer for patterning by AFM lithography, (c) after AFM oxidation and selective wet etching, holes localized according to the supply layer patterns.

As a demonstration of the process to localize holes, we first fabricated a Hall bar mesa on the Si/SiGe 2D hole gas. Then we cut a line through the Hall bar as shown in Fig. 6. The two-terminal resistance after the line cutting raised from 300 kΩ without cutting to larger than 10 GΩ, after the AFM oxidation and etching process to remove the supply layer.

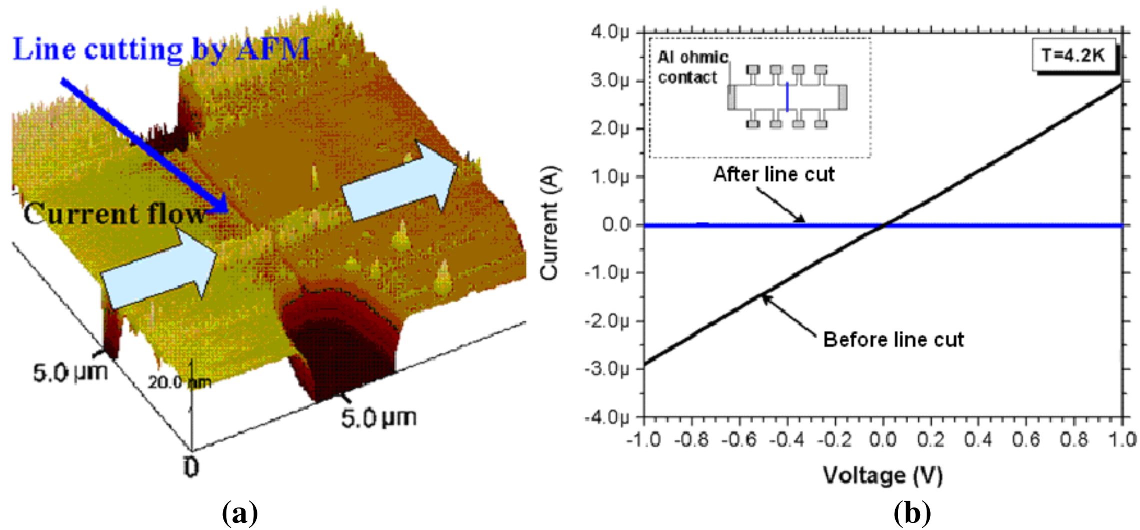

Figure 6. (a) AFM image of Hall bar showing conducting path cut by PFOTS-aided AFM lithography of supply layer in 2-D hole gas, and (b) I-V curve showing increased resistance at 4.2K after the cut. The insert is a schematic of the patterned Hall bar.

CONCLUSIONS

In summary, PFOTS-aided AFM lithography has been demonstrated to improve the nanopatterning of Si/SiGe layers by improving the ability to transfer pattern from the oxidized silicon to the underlying SiGe layer. This process has been applied to create a novel 2D hole gas

structure to localize the 2D hole gas without exposing the SiGe surfaces. This process could be used to create dual SiGe-gated single-hole transistors without surface states.

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