High retention-time nonvolatile amorphous silicon TFT memory for static active matrix OLED display without pixel refresh

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Existing a-Si floating gate TFT (FG-TFT) nonvolatile memory suffers from two drawbacks: (i) short retention time [1] and (ii) strong dependence of drain saturation current ($I_{D,SAT}$) on drain voltage [2]. In this study, we present (i) a new device structure that eliminates $I_{D,SAT}$ dependence on drain voltage; (ii) room-temperature retention time of >10 years; and (iii) the integration of this new TFT memory into AMOLED pixels, enabling displays without refresh.

The structure of previous a-Si FG-TFTs are shown in Fig. 1. The fabrication process flow can be found in [2]. In this structure, the drain electrode is capacitively coupled to the floating gate, by the overlap of the floating gate and the drain resulting from a non-self-aligned process. As a result, the voltage on the floating gate increases with increasing drain bias [3]. This is manifested as a strong dependence of drain current on the drain voltage in the device saturation regime. Our new SiN_x Trap TFT (ST-TFT) memory (Fig. 2) utilizes an insulating layer with high defect density as the charge trapping medium, instead of the floating gate, as in VLSI SONOS nonvolatile structures [4]. Since the charge traps do not form a conductor, the regions that overlap the S/D do not contribute to the parasitic coupling, which affect device saturation behavior. This can be clearly seen in a comparison of the IV characteristics of the two devices (Fig. 3). The ST-TFT has a clear a saturation regime while the FG-TFT does not.

The ST-TFT works based on electrons tunneling into the SiN_x traps from the channel and out from the SiN_x traps into the channel under the applied gate field. No drain field or hot electron effects are involved. Fig. 4 shows the DC transfer characteristics of a ST-TFT before programming, after programming and after erase. Clear reversible V_T shifts can be observed. The programming and erasing characteristics of the ST-TFT are shown in Fig. 5 and Fig. 6 respectively. The room-temperature retention characteristic of the ST-TFT is shown in Fig. 7. The programmed state decays over time as the trapped electrons leak out of the traps. The erased state remains unchanged over time, because there are no trapped charges to leak out. The memory window of the device is extrapolated to be 80% of its initial value after 10 years of storage at room temperature, a significant improvement over the 1 hour retention of previous work [1].

The ST-TFT memory can be directly integrated into an AMOLED display. In a conventional AMOLED pixel, the desired brightness level is achieved by varying the data voltage, which sets the gate voltage on the driver TFT and the current through the OLED. The data voltage is maintained by a storage capacitor and requires periodic refresh, which consumes power. In our AMOLED pixel with integrated memory, we replace the driver TFT with a memory ST-TFT, whose threshold voltage can be changed by programming through the data line voltages (Fig. 8). We can set the pixel currents (OLED brightness levels) by changing the V_T of the driver TFTs, while holding all the select lines high and all the data lines at a fixed voltage. We can precisely control the OLED current this way, because $I_{D,SAT}$ of the ST-TFT does not depend on drain voltage (Fig. 3). The programmed brightness level remains stored in the ST-TFT, eliminating the need for storage capacitors and pixel refreshes, which improves pixel fill factor and reduces power consumption. Fig. 9 shows a 10x10 AMOLED display with integrated memory.

We have successfully fabricated a non-volatile a-Si memory device with excellent programming/erase and retention characteristics, and it is fully compatible with conventional TFT fabrication process. The new structure has flat saturation characteristics and was successfully integrated into an AMOLED display, giving it the capability to display and store images without pixel refresh.

[1] Y. Kuo et al., *Applied Physics Letters*, vol 89, pp 173503-6, October
[2] Y. Huang et al, Proceedings of 67th Annual Device Research Conference, Conference Digest, p 135-136, June 2009
[3] S. T. Wang, *IEEE Transactions on Electron Devices*, Vol. ED-26, No. 9, pp. 1292-1293, September 1979
[4] S. J. Wrazien et al, Solid State Electronics vol 47, pp 885-891, 2003

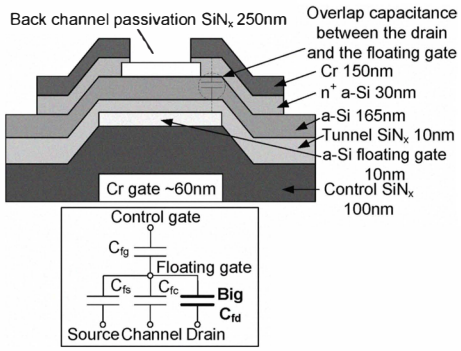

Figure 1. Structure of the a-Si floating gate TFT (FG-TFT) memory. Large overlap between FG and drain results in strong capacitive coupling.

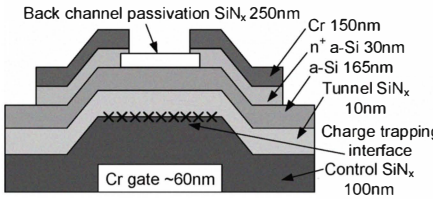

Figure 2. Structure of the a-Si SiN_x Trap TFT (ST-TFT) memory. Charge trapping medium is a layer of defects formed by RIE. Since the charge traps do not form a conductor, the overlapping regions between the S/D and the charge trapping layer do not contribute to parasitic capacitance that affect device behavior.

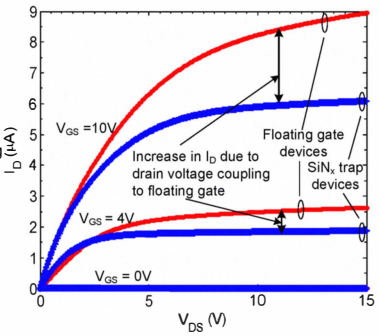

Figure 3. I_{DS} vs V_{DS} for an FG-TFT and a ST-TFT fabricated on the same wafer with the same W/L (60/5) and gate dielectric thickness (270nm).

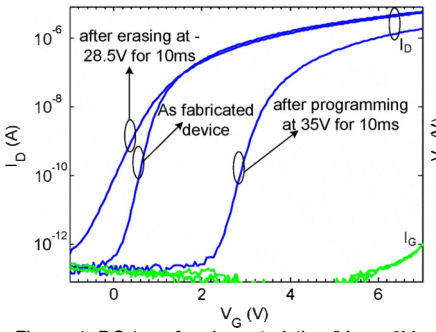

Figure 4. DC transfer characteristics (V_{DS} = 8V and V_G swept from 7 to -1V in 50mV increments) of the ST-TFT at various stages of the program/erase cycle. Program: V_G held at 35V for 10ms with S/D grounded. Erase: V_G held at -28.5V for 10ms with S/D grounded

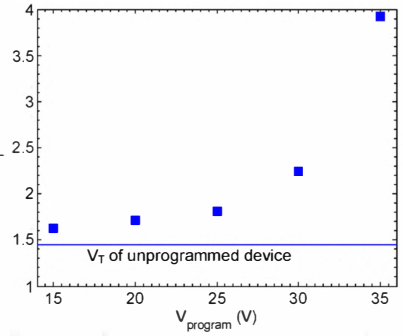

Figure 5. Programming characteristics of the ST-TFT. Devices are programmed with S/D grounded, and $V_{program}$ applied to the gate for 10ms.

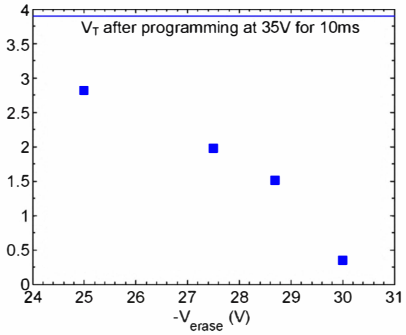

Figure 6. Erasing characteristics of the ST-TFT. Devices are first programmed with S/D grounded, and 35V applied to the gate for 10ms. Then erased by applying V_{erase} to the gate for 10ms with the S/D grounded.

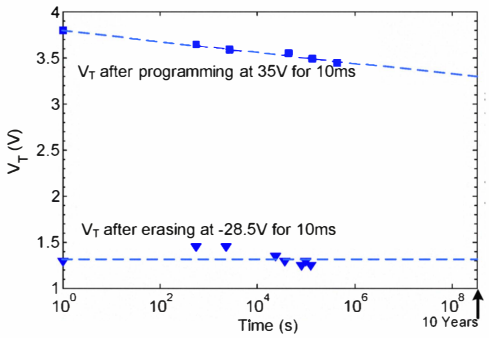

Figure 7. The room-temperature retention characteristics of the ST-TFT. Devices are programmed/erased and stored at room temperature with all electrodes floating. The shown dotted lines are extrapolations of measured data points (solid sqaures and triangles).

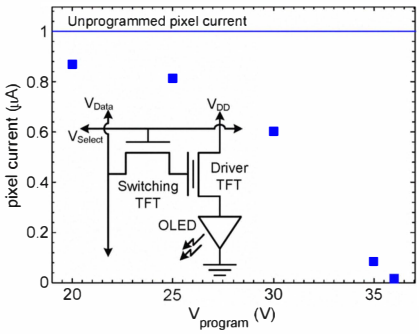

Figure 8. Current through the driver TFT after pixel programming. Inset shows the circuit schematic of an AMOLED pixel with integrated ST-TFT memory. Note the absence of the storage capacitor that is common in conventional AMOLED pixels. Pixels are first programmed by applying $V_{program}$ to the data line for 10ms, with V_{DD} electrode grounded the select line high. Pixel currents are then measured with V_{data} = 8V and V_{DD} = 10V.

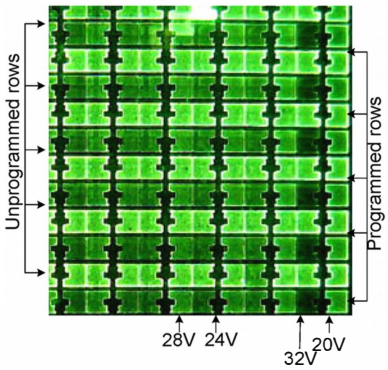

Figure 9. 10x10 AMOLED display driven with V_{data} = 8V and V_{DD} = 10V. The odd rows have unprogrammed pixels. The even rows have programmed pixels. Within each programmed row, the pixels are programmed to 4 intensity levels as indicated by the arrows. Note that the entire display is driven with with a single DC data voltage. No pixel refreshes are being performed. The image remains the same after display powers off and on again.