A new method for predicting the lifetime of highly stable amorphous-silicon thin-film transistors from accelerated tests

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***Abstract*— We present a new method for predicting the lifetime of highly stable amorphous-silicon thin-film transistors (a-Si TFTs) from accelerated tests at elevated temperatures. The rate of DC saturation current drop can be accelerated by a factor of ~10^4 when the test temperature is raised to 160°C. This ability is particularly significant for predicting the stability and lifetime of a-Si TFTs as analog drivers in active-matrix organic light emitting diode (AMOLED) displays.**

Keywords- Accelerated lifetime tests, a-Si TFTs, stability, current degradation, stretched hyperbola

I. INTRODUCTION

Because conventionally-fabricated a-Si TFTs are unstable, they are usually used only as digital switches at low duty cycle in active-matrix liquid crystal displays (AMLCDs). Ultra-stable a-Si TFTs have been recently reported and proposed for analog drivers of the OLEDs in AMOLED displays [1,2]. This application requires a reliable method for evaluating their stability and predicting their lifetime. a-Si TFTs in AMOLEDs are driven at low gate voltage, where defect creation in a-Si dominates the degradation. The concurrent threshold voltage shift causes a reduction of the TFT's drain current [1,3]. In this work, we obtain the distribution of defect creation energies and the "attempt-to-break" frequency in the a-Si from drain current vs. time data taken at elevated temperatures. We relate these parameters, which characterize the stability of a-Si, to the acceleration factor for TFT current degradation. This work then enables one to predict the room temperature lifetime of devices from accelerated tests at elevated temperatures using a physically-based model.

II. THEORETICAL FRAMEWORK

A. Defect Creation

The threshold voltage shift of a-Si TFTs under gate bias leads to reduced drain current and thereby reduced OLED brightness in AMOLED displays. At the low gate fields appropriate for driving OLEDs, defect creation by bond-breaking in a-Si is the mechanism [1,3] that we need to accelerate to predict the lifetime of a-Si TFTs. The degradation of TFT drain current is accelerated at elevated temperatures, where strained bonds are thermally activated and more easily broken. The amorphous nature of a-Si results in a range of Si-Si bond energies. The distribution of electron energies E on strained (weak) bonds is modeled with an exponential function $n(E) \propto e^{E/kT_0}$, where the characteristic temperature T_0 reflects the disorder broadening of the a-Si structure, and a high value of T_0 reflects a broad distribution of strained bonds [4]. Therefore, the conventional Arrhenius model for thermally activated failure of electronic devices cannot be applied directly to a-Si TFTs. Wehrspohn et al. proposed a stretched hyperbola model [5-8] for the defect creation process in the form of

$$\Delta N_{DB}(t) = N_{BT}^{0}\left\{1 - \left[1 + \left(\frac{t}{t_0}\right)^{T/T_0}\right]^{-1/(\alpha-1)}\right\}\} \quad (1)$$

$\Delta N_{DB}(t)$ is the number of created defects, N_{BT}^{0} is the initial number of carriers in the band-tail at $t = 0$, the fitting parameter α takes into account a superlinear bias dependence, ranging from 1 to 2, and $t_0 = \nu^{-1}\exp(E_{act}/kT)$. ν is the "attempt to break" frequency in the model for the bond-breaking frequency $1/t_0$, and the effective activation energy E_{act} is related to the weighted average energy barrier for defect creation under gate bias [5,8]. E_{act} differs from the conventional activation energy in an Arrhenius model, in that it is a weighted average energy for the distribution of electron energies E on strained (weak) bonds in a-Si, instead of a single energy as in crystalline silicon.

B. Acceleration of Drain Current Degradation

At low gate fields, defect creation in a-Si leads to a threshold voltage shift of a-Si TFTs, with

$$\Delta V_T(t) = q\Delta N_{DB}(t)/C_{ins} \quad (2)$$

where C_{ins} is the capacitance of the gate insulator.

Since

$$N_{BT}^{0} = (V_G - V_{T0}) \times C_{ins}/q \quad (3)$$

by substituting (2) and (3) into (1), the threshold voltage shift as a function of time under bias can be expressed as [5]

$$\Delta V_T(t) = (V_G - V_{T0})\left\{1 - \left[1 + \left(\frac{t}{t_0}\right)^{T/T_0}\right]^{-1/(\alpha-1)}\right\} \quad (4)$$

In this work we combine the stretched hyperbola model for the defect creation with the current-voltage relation for a-Si TFTs in the saturation regime

$$I_D(t) = \frac{1}{2}\mu_n C_{ins}\frac{W}{L}[V_G - (V_{T0} + \Delta V_T(t))]^2 \quad (5)$$

Since the changes of mobility are much less significant to the drain current degradation than the changes of threshold voltage (shown in section IV. A.), we neglect the mobility changes in our analysis. By substituting (5) into (4), the reduction with time of the normalized drain current $I_{D,nor}(t) \equiv I_D(t)/I_D(t=0)$ caused by threshold voltage shift can be expressed as

$$I_{D,nor}(t) \equiv \frac{I_D(t)}{I_D(t=0)} = \left[1 + \left(\frac{t}{t_0}\right)^{T/T_0}\right]^{-2/(\alpha-1)} \quad (6)$$

Equation (6) shows that the normalized drain current degradation is temperature dependent, with temperature T appearing in parameter $t_0 = \nu^{-1}\exp(E_{act}/kT)$ and the exponential term T/T_0. Thus, accelerated lifetime tests can be carried out by simply monitoring the drain current degradation at elevated temperatures.

Note that the normalized drain current degradation in the saturation regime can be directly used to characterize the stability of a-Si TFTs, without having to be converted to a threshold voltage shift ΔV_T as in the conventional stretched-hyperbola method [5-8]. Also note that while the term $(V_G - V_{T0})$ in (4) can vary from transistor to transistor, the current degradation method based on (6) has the advantage that it is independent of $(V_G - V_{T0})$.

III. EXPERIMENTAL PROCEDURE

A. Sample Preparation

The samples in our measurements are back-channel passivated TFT structures (Fig. 1). A standard bottom-gate non-self-aligned process was used.

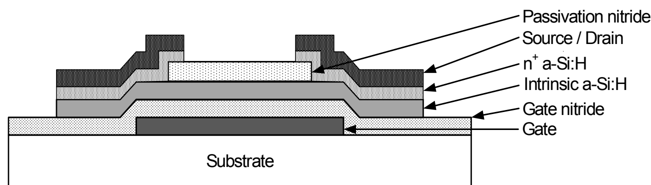

Figure 1. Schematic cross-section of back-channel passivated TFT structure.

The silicon nitride and amorphous silicon were grown in a standard plasma-enhanced chemical vapor deposition (PECVD) system. 300-nm gate nitride, 200-nm intrinsic hydrogenated a-Si and 300-nm passivation nitride were deposited sequentially at 350°C, 250°C and 250°C, respectively. The silicon nitride and a-Si were patterned with dry etching. Before measurements, all samples were annealed at 200°C to remove the damage induced by the dry-etching plasma.

B. Accelerated Lifetime Testing

For accelerated lifetime testing, the TFTs were biased in the saturation regime with a constant gate voltage of 5V (a gate field of ~1.5×10^5V/cm) and a constant drain voltage of 7.5V. We raised the substrate temperature from 20°C to 160°C in steps of 20°C. At each temperature we biased a fresh TFT without any prior stress in the saturation regime and measured the drain current as a function of time. This measurement was done without any interruption, for example to measure I_D-V_G characteristics at intermediate points. At the end of the continuous bias stress period, a gate-bias voltage sweep was applied to measure the I_D-V_G characteristics of the TFTs. To minimize structural rearrangement and hydrogen diffusion in the a-Si, in the testing we did not exceed 160°C, which is much lower than the a-Si silicon deposition temperature at 250°C and the 200°C annealing temperature.

IV. RESULTS AND DISCUSSION

A. Shifts of Transfer Characteristics after Stress

For our 150μm wide and 15μm long channel TFTs, at 20°C and in the saturation regime, the initial drain current $I_D(t=0)$ was 2.12±0.09μA, with the initial threshold voltage 0.44±0.22V and the field-effect mobility 0.99±0.12cm^2/V·s. Higher extracted mobilities were correlated with higher extracted threshold voltages to give the tight current distribution.

The transfer characteristics for samples before and after stress were recorded at 20°C and 160°C. To avoid defect creation during the gate-bias voltage sweep, at 20°C we took a fast sweep, with V_G swept from 5V to -3V in 3 sec. V_D was kept at 10V in order to stress the TFT in the saturation regime, which is consistent with the bias stress condition in the accelerated lifetime tests. The $\sqrt{I_D}$-V_G plots before and after a 5×10^4 sec bias stress at 20°C are shown in Fig. 2(a), from which we can see that the bias stress leads to a 12% drop of the drain current when V_G=5V. The slope of $\sqrt{I_D}$-V_G is almost constant before and after the bias stress, with the extracted field effect mobility changing from 0.88cm^2/V·s before the bias stress to 0.89cm^2/V·s after the bias stress (~1% change). The threshold voltage increased from 0.30V to 0.62V with ΔV_T=0.32V.

Similar $\sqrt{I_D}$-V_G plots before and after a 1.0×10^4 sec bias stress at 160°C in Fig. 2(b) show that the bias stress leads to a 86% drop of the drain current when V_G=5V. The two I_D-V_G sweeps were also taken at 160°C. From the slope of $\sqrt{I_D}$-V_G, the extracted field effect mobility changing from 3.46cm^2/V·s before the bias stress to 3.57cm^2/V·s after the bias stress (~9% change). The threshold voltage increased from 0.48V to 3.12V with ΔV_T=2.64V.

At both temperature extremes (20°C and 160°C) in our accelerated lifetime testing, the effect of the threshold voltage

shifts was the dominant one on the TFT current degradation, validating our modeling approach to derive (6).

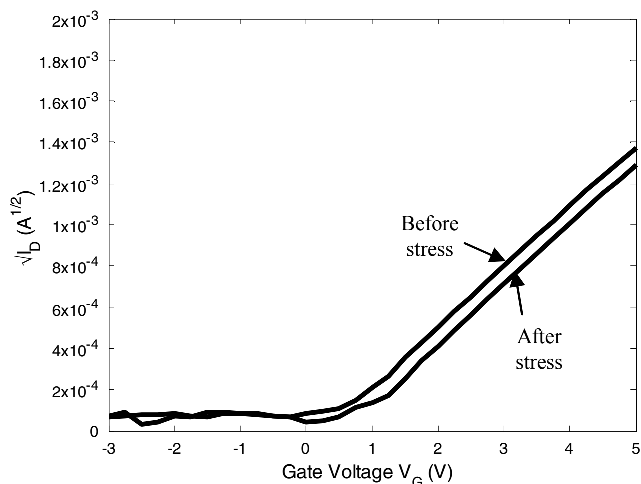

Figure 2(a). $\sqrt{I_D}$-V_G plots before and after a 5×10^4 sec bias stress at 20°C.

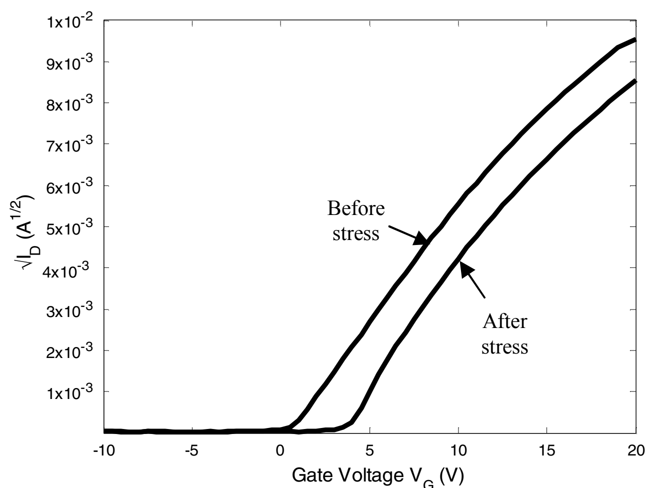

Figure 2(b). $\sqrt{I_D}$-V_G plots before and after a 1×10^4 sec bias stress at 160°C.

B. *Dependence of Drain Current Degradation on Temperature*

The experimental data of normalized drain current $I_{D,nor}$ as a function of time at different temperatures are shown with open squares in Fig. 3.

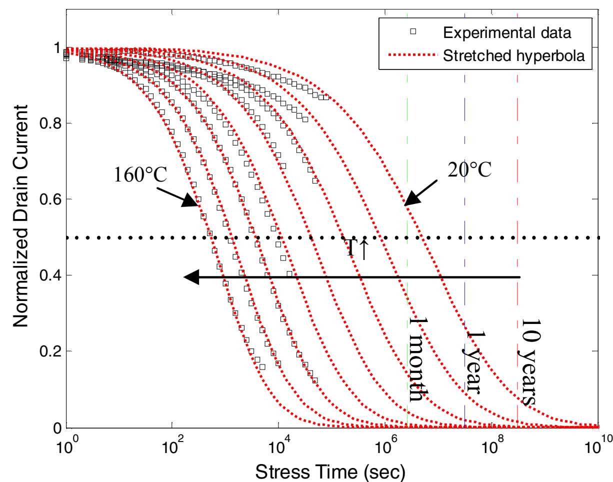

Figure 3. Normalized drain current degradation data (open squares) of the a-Si TFTs at temperature stepped by 20°C from 20°C to 160°C. The dotted lines are stretched hyperbola fits described in Fig. 4 and (7).

We can represent all sets of current vs. time data with a single curve by replacing the time axis with the "thermalization energy" [5-8], which is defined as $E_{th} = kT\ln(\nu t)$. That all experimental data (open squares in Fig. 4) cluster so closely on a single curve with $\nu = 4\times10^5$Hz gives us confidence in this method to predict the drain current degradation at low temperatures with high temperature data. From (6), the relation for $I_{D,nor}$ with E_{th} can be reformulated as

$$I_{D,nor}(E_{th}) = \{1 + \exp[(E_{th} - E_{act})/kT_0]\}^{-\frac{2}{\alpha-1}} \quad (7)$$

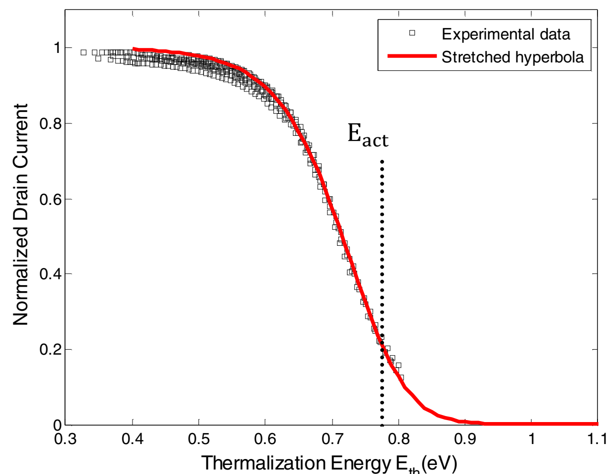

Figure 4. Normalized drain current unified in terms of the thermalization energy $E_{th} = kT\ln(\nu t)$, where $\nu = 4\times10^5$ Hz. Stretched-hyperbola fit (solid line) with $\alpha = 1.9$.

Equation (7) provides an excellent stretched-hyperbola fit with $\alpha = 1.9$, shown as the solid curve in Fig. 4. We find $E_{act} = 0.78$eV and $T_0 = 680$K; both are typical values for a-Si and are independent of temperature. The relation of $E_{th} = kT\ln(\nu t)$ between thermalization energy and time enables the stretched hyperbola fit in a direct function of time to the data in Fig. 3 (dotted lines in Fig. 3), using the parameters α, ν, E_{act} and T_0 (Table I). The fits agree well with the experimental data over the entire temperature range.

TABLE I. FITTING PARAMETERS

α	ν (Hz)	E_{act} (eV)	T_0 (K)
1.9	4×10^5	0.78	680

In previous current degradation work [10], the exponent of t/τ (our t/t_0) was referred to as β. Physically, β should equal to T/T_0, where T_0 is the characteristic temperature reflecting the disorder broadening of the a-Si structure and should not change under low temperature stress. In [10], β was used as an independent fitting parameter at each temperature, and the T_0 caculated from T/β was temperature dependent, which is physically implausible. Although the data could be fitted at each temperature, there was no physical basis for using high temperature results to predict drain current degradation at room temperature.

In our work, we used a single fitting parameter T_0 for all stress temperatures, which makes a physically plausible accelerated lifetime test possible.

C. Acceleration Factors

We define the acceleration factor (AF) for drain current reduction as the ratio of the DC saturation current half-life [1] at room temperature (20°C) $t_{RT,50\%}$ to that at the stress temperatures $t_{ST,50\%}$. From (6), AF can be written as

$$AF = \frac{t_{RT,50\%}}{t_{ST,50\%}} = \frac{(50\%^{-\frac{\alpha-1}{2}}-1)^{\frac{T_0}{T_{RT}}}\nu^{-1}\exp(E_{act}/kT_{RT})}{(50\%^{-\frac{\alpha-1}{2}}-1)^{\frac{T_0}{T_{ST}}}\nu^{-1}\exp(E_{act}/kT_{ST})} \quad (8)$$

With the fitting parameters α, ν, E_{act} and T_0, AFs at elevated temperatures are calculated from (8) and listed in Table II. A 160°C AF is 9.5×10^3, which means that accelerated lifetime tests with our method can be used to drastically reduce the duration of a-Si TFT stability tests.

TABLE II. HALF-LIVES AND ACCELERATION FACTORS AT STRESS TEMPERATURES FROM 20°C to 160°C RELATIVE TO ROOM TEMPERATURE (20°C)

T (°C)	20	40	80	120	160
Half-life (s)	5.0×10^6	8.1×10^5	4.0×10^4	3.7×10^3	5.2×10^2
AF	1.0	6.1	1.2×10^2	1.4×10^3	9.5×10^3

D. Accelerated Threshold Voltage Shifts

With the current-voltage relation for a-Si TFTs in the saturation regime expressed as (5), the drain current degradation can be converted to the threshold voltage shift. The converted threshold voltage shifts as a function time at temperatures from 20°C to 160°C are shown with the open squares in Fig. 5. The threshold voltage shifts are faster at elevated temperatures. Stretched hyperbola fits with (4) and the fitting parameters listed in Table I are shown with the dotted lines in Fig. 5. Our results for the threshold voltage shift of TFTs biased in saturation regime at different temperatures agree well with the stretched hyperbola model and are similar to the threshold voltage shift analysis in [5-8].

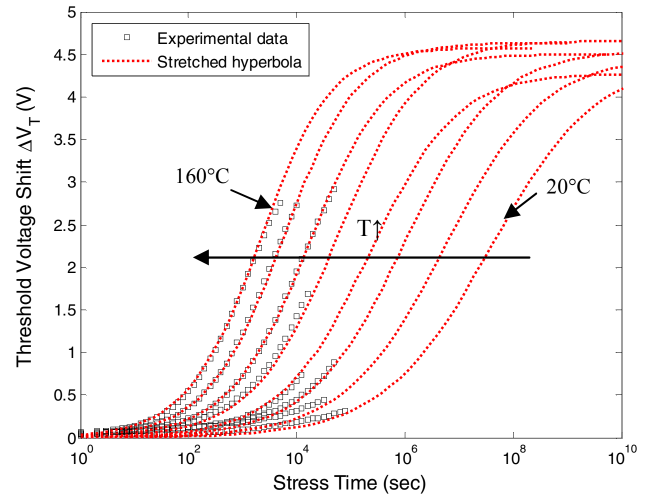

Figure 5. Threshold voltage shift data (open squares) and stretched hyperbola fits (dotted lines) of the a-Si TFTs at temperature stepped by 20°C from 20°C to 160°C.

Note that to convert the threshold voltage shift from drain current data and plot the stretched hyperbola fits require the knowledge of V_{T0} at each temperature. The difference of $(V_G - V_{T0})$ at each temperature leads to the different asymptotic values of ΔV_T at long time.

The analysis of the normalized drain current degradation with (6) and that of the threshold voltage shift with (4) are fundamentally similar. However, the normalized drain current degradation analysis we present here does not require the measurement of transfer characteristics to calculate V_{T0} of each transistor.

E. Discussion

For our benchmark of DC saturation current half-life, the 50% drain current degradation for an initial threshold voltage V_{T0} =0.44V is equivalent to a threshold voltage shift of ΔV_T=1.3V, which corresponds to a 2D charged defect density of $\Delta N_{DB}=1.7\times10^{11}$cm^{-2} created during the low gate field stress.

We have explained our approach in terms of weak bonds with the exponential barrier distribution model [12] and additional weakening of the occupied conduction-bandtail

states [5]. However, we note that the stretched hyperbola model [5-8], the basis of our method, is a semi-empirical model, which can also be used to model the defect creation by a hydrogen diffusion model [11] with a carrier-dependent hydrogen-diffusion constant [5].

For the 160°C bias stress, subthreshold plots of I_D-V_G are shown in Fig. 6. The subthreshold slopes were ~750mV/dec both before and after the bias stress, with any change difficult to determine within the experimental resolution, which agrees with the observations in [9,10]. It is not straightforward to quantitatively relate the number of created defects as inferred by the threshold voltage shift data to the defects created in the a-Si or at the interface between the a-Si and the silicon nitride from the subthreshold slope data. This is because the threshold voltage shift characterizes the number of defects created deep in the band gap, while the subthreshold slope depends heavily on the localized band tail states as well [13].

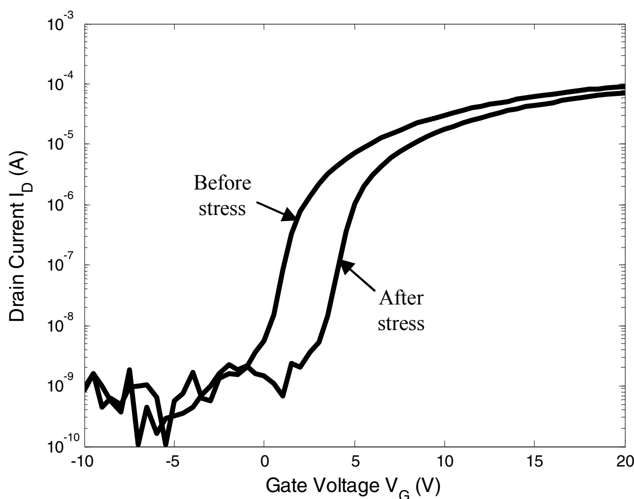

Figure 6. Subthreshold plots before and after a 1×10^4 sec bias stress at 160°C.

Highly stable a-Si TFTs reported recently have extrapolated DC saturation current half-lives that range from 100 to 1000 years, based on only months of testing at room temperature [1,2]. With our method for accelerated lifetime testing by monitoring the DC saturation current degradation at elevated temperatures, an acceleration factor of $\sim 10^4$ at 160°C is achieved, which enables us to establish the half-life of such devices with much higher confidence than tests conducted at room temperature alone.

V. SUMMARY

a-Si TFTs can be fabricated to have extremely long operating lifetimes under DC gate bias. The time at room temperature for the drain current to drop to 50% of its initial value can reach 100 to 1,000 years. To date, these lifetimes have been calculated by extrapolating tests conducted for several months at room temperature. Now we have shown that the rate of current drop can be accelerated by a factor of nearly 10,000 when the test temperature is raised to 160°C. Thus, a month-long degradation test conducted at 160°C would yield the same information as a 10,000-month (~800 years) long test conducted at 20°C. This ability is particularly significant for predicting the stability and lifetime of a-Si TFTs in AMOLED displays.

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