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MOBILITY ENHANCEMENT AND QUANTUM MECHANICAL MODELING IN Ge_xSi_{1-x} CHANNEL MOSFETs FROM 90 TO 300 K

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ABSTRACT

A peak hole inversion layer mobility of 290 $cm^2/V{\cdot}s$ has been achieved at room temperature in Ge_xSi_{1-x} buried channel pMOSFETs. The peak mobility rises to 970 $cm^2/V{\cdot}s$ at 90 K. This corresponds to a 50% enhancement in the effective mobility over Si control devices at room temperature and enhancements of over 100% at 90K. The mobility of MOS-gated Ge_xSi_{1-x} buried channel transistors can be effectively modeled at room temperature by considering the dependence of the surface scattering on the average separation of carriers from the Si/SiO_2 interface. The mobility for devices with a 75 Å and a 105 Å Si spacer layer were tested and accurately modeled at room temperature using parameters extracted from a Si control device. At low temperatures (~90 K) an additional scattering term must be included to better fit the data. It is suggested that this additional term could result from alloy scattering in the Ge_xSi_{1-x} channel.

INTRODUCTION

Recently Ge_xSi_{1-x} / Si heterojunctions have been considered for use in improved hole mobility MOS devices (1),(2),(3). The idea is to place a Ge_xSi_{1-x} layer, separated from the gate oxide by a thin (≈100 Å) Si spacer layer, underneath the gate of a PMOS device (see Figure 1). The discontinuity in the valence band at the Ge_xSi_{1-x}/Si interface allows for an inversion layer to form in the Ge_xSi_{1-x} layer increasing the separation of the holes from the Si/SiO_2 interface. It is thought that the surface scattering, from the surface roughness and the oxide's fixed charge, is the reason for the inversion layer's inherently poor mobility (4) (≈1/3 that of bulk Si). The increased separation of the holes from the Si/SiO_2 interface should (and does (1)(5)(6)(7)) result in a substantially enhanced inversion layer mobility.

Quasi-static C-V measurements and Hall measurements have shown that carriers can be exclusively confined to the Ge_xSi_{1-x} well up to a certain gate voltage beyond which the Si/SiO_2 interface is also inverted. Results from a 1-D Poisson simulation of the hole density versus gate bias for a structure with a 105 Å Si spacer layer and a Ge fraction of 0.33 in the well are shown in Figure 2. One sees that an inversion layer initially forms in the Ge_xSi_{1-x} well with no corresponding inversion layer at the surface, however at some critical gate voltage, determined by the structure, the Si/SiO_2 interface also inverts. Once this occurs almost all the subsequent holes are added to the Si/SiO_2 interface causing a "kink" in the total hole density curve due to the transition from the lower capacitance of the well:

$$(C_{gate})^{-1}=(C_{ox})^{-1}+(C_{Si\ spacer})^{-1}$$

to the higher capacitance of the Si/SiO_2 interface (C_{ox}).

The hole density in the Ge_xSi_{1-x} well, where we expect to have a higher mobility, is a function of the spacer layer width and the Ge fraction in the well. The optimization of the hole density in the Ge_xSi_{1-x} well has been explored using a 1-D Poisson solver (3) but this question remains - "How does the spacer layer thickness affect the inversion layer mobility ?" . If we are able to accurately model the dependence of the mobility on the spacer layer thickness then all the necessary information will be available for modeling the transconductance of the Ge_xSi_{1-x} /Si MOSFETs.

In this paper we examine the performance enhancement of two Ge_xSi_{1-x} structures relative to Si control devices and the utility of a simple surface scattering model in predicting the device performance.

EXPERIMENT

The Ge_xSi_{1-x} /Si transistor structures were epitaxially grown on Si (100) substrates by Rapid Thermal Chemical Vapor Deposition using dichlorosilane and germane at 625°C (8). The epitaxial films are doped n-type with concentrations of $\approx 1\times10^{16}$ cm^{-3}. Sources and drains were implanted with boron at 25keV and 50keV with a total dose of 5×10^{14} cm^{-2}. A low temperature plasma deposited gate oxide of 125 Å thickness was used. This deposition was followed by a 700°C/30 min N_2 furnace anneal. This anneal served as both an implant anneal and to reduce the fixed charge of the PE-CVD oxide. Contact holes for the source and drain were opened and aluminum was evaporated to form the gate and source/drain contacts. For this work two variations of the buried Ge_xSi_{1-x}/Si structure were grown and analyzed along with Si control devices grown on a prime Si wafer (see Table I). The two Ge_xSi_{1-x}/Si structures have been shown by simulation to have approximately the same upper limit to the hole density in the Ge_xSi_{1-x} well of $\approx 1.2\times10^{12}$ cm^{-2}, thus differences between the two structures will be due to the actual mobility differences in the Ge_xSi_{1-x} channel rather than the number of carriers.

Values of the low field mobility were extracted from drain conductance measurements on FETs with gate lengths ranging from 7 to 200 µm. Typical drain conductance measurements for the three samples using 97 µm gate length FETs and an applied drain bias of -0.1 volts are shown in Figure 3 (measured at 300K). The drain conductance curves are plotted vs. V_g-V_t to compare the curves at approximately the same carrier density. The drain current of sample 646 is uniformly 20-30 % better than the Si control across the whole range of V_g-V_t and sample 649 is 50% improved. This suggests that the mobility enhancement is due to the increasing separation of holes from the Si/SiO_2 interface.

A curve of the *effective* mobility vs. effective field can be extracted from this data by approximating the inversion carrier

density by: $Q_{inv} = C_{ox} \times (V_g - V_t)$

and the effective (normal) field by:

$$E_{eff} = (Q_{dep} + \frac{1}{\eta} Q_{inv}) / \varepsilon_{Si}$$

The *effective* mobility is useful for circuit design and makes for meaningful performance comparisons with all-Si devices. (The actual hole mobility differs from this number because of the lower gate capacitance of the Ge_xSi_{1-x} layer.)

Results for the *effective* mobility measured at 300K are shown in Figure 4. At low temperature not only do all the mobilities increase (as expected), but the relative increase in the Ge_xSi_{1-x} devices is faster than that of the silicon control. The performance enhancement of sample 649 at 90 K is now over 100% across the whole range of effective fields, with a peak effective mobility of 780 $cm^2/V{\cdot}s$ (Figure 5). The performance enhancement trend is also clearly seen when one looks at the peak effective mobility vs. temperature as plotted in Figure 6.

MODEL

The disproportionately large increase of the Ge_xSi_{1-x} device mobility relative to the silicon control at low temperature is evidence that the enhancement mechanism is indeed surface scattering. At low temperatures the reduced phonon scattering makes the surface scattering more significant, so that a larger improvement in the Ge_xSi_{1-x} device's mobility is seen. This trend of increasing mobility enhancement for the Ge_xSi_{1-x} devices at low temperature is not consistent with a reduced effective mass in the Ge_xSi_{1-x} well. Any increase in mobility due to a lowering of the effective mass should be independent of temperature.

In order to model the mobility enhancement achieved by moving the carriers away from the interface in the Ge_xSi_{1-x} FETs we must develop a relation between the surface scattering mobility (μ_s) and the average separation of the carriers from the surface (Z_{avg}). In this model we link these two quantities via their relation to the effective field (i.e. the transverse field of the gate potential).

We use the experimentally obtained inversion layer mobilities of the Si control devices to extract the surface scattering term by assuming that only the bulk and surface mobilities are significant. Using Matthiessen's rule we see that $(\mu_s)^{-1} = (\mu_{inversion})^{-1} - (\mu_{bulk})^{-1}$. Thus from measurements of our Si control devices (measuring $\mu_{inversion}$) we can extract a relation between μ_s and the effective field (also knowing the bulk mobility).

We now need to find the dependence of the average separation of the carriers from the Si/SiO_2 surface in a Si device on the effective field ($Z_{avg} = Z_{avg}(E_{eff})$). We do this as follows:

1. We start with the subband energy levels in a PMOS inversion layer as calculated for several inversion layer hole densities by Ohkawa and Uemura (9).
2. Next we express this as a relation between the effective field and the subband energy levels.
3. Now we fit variational wavefunctions such as those described in (10) to the energy levels in order to estimate the average spacing of the holes in the subband from the surface.
4. Finally we equate the average carrier separation distance from the Si/SiO_2 surface (Z_{avg}) to a weighted average of the subband separation distances (based on the subband occupation levels).

Now that we have related both the surface scattering mobility term and the average separation of the holes from the Si/SiO_2 interface to the effective field we can fit a relation directly between the two. We assume that the surface scattering is inversely proportional to the square of the separation distance. In terms of mobility: $\mu_{sr} \propto (Z_{avg})^2$

Once this relation is fit using measurements from a silicon control device we can use it to predict the surface scattering mobility in our Ge_xSi_{1-x} devices (which due to the band offsets follow a different relation of Z_{avg} to the effective field).

We must take into account the presence of carriers in both the Ge_xSi_{1-x} well and the Si/SiO_2 channel since their separation from the Si/SiO_2 interface is very different. Thus we propose:

$$Z_{avg}(Ge_xSi_{1-x}) = t_{Si\ spacer} + Z(E_{eff,Ge_xSi_{1-x}})$$

and

$$Z_{avg}(Si) = Z(E_{eff,Si/SiO_2})$$

where:

$$E_{eff,Si/SiO_2} = (Q_{dep} + Q_{Ge_xSi_{1-x}} + \frac{1}{3} \times Q_{Si/SiO_2}) / \varepsilon_{Si}$$

and

$$E_{eff,Ge_xSi_{1-x}} = (Q_{dep} + \frac{1}{3} \times Q_{Ge_xSi_{1-x}}) / \varepsilon_{Si}$$

These definitions are visually portrayed in Figure 8.

Hole densities in the Ge_xSi_{1-x} well and at the Si/SiO_2 interface obtained from simulations using a 1-D Poisson solver are used to take a weighted average of the Ge_xSi_{1-x} surface mobility term and the Si/SiO_2 surface mobility term. The calculated surface mobility is then combined with the bulk mobility using Matthiessen's rule to obtain our estimate of the inversion layer mobility for a given Ge_xSi_{1-x} FET at a given effective field. The familiar data of Jacoboni et al. (11) is used for the bulk mobility.

It is important to distinguish the *effective* mobility from the actual inversion layer mobility in Ge_xSi_{1-x} / Si transistors. The *effective* mobility assumes that the hole density under the gate is simply: $Q_{inv} = C_{ox} \times (V_g - V_t)$. In the case of the GexSi1-x / Si transistors the gate capacitance is lower than C_{ox} because of the additional series capacitance of the Si spacer layer. Thus the number of carriers is overestimated using C_{ox}. The effective mobility is useful for circuit modeling but obscures the physics of these devices. Henceforth we will consider the actual inversion layer mobility as calculated and modeled using the simulated hole densities.

The result of applying this model to sample 649, which has a 105Å Si spacer, at room temperature is shown in Figure 9. The model fit is very good across the whole range of effective fields. Also plotted for comparative purposes is the effective mobility.

At low temperatures this model greatly overestimates the mobility. In order to fit the data at 90 K an additional, constant mobility term must be incorporated into the estimates of the hole mobility in the Ge_xSi_{1-x} well (Figure 10). This additional term could be attributed to either alloy scattering or "roughness" of the Ge_xSi_{1-x}/Si interface. The additional term has a magnitude of 1470 $cm^2/V{\cdot}s$. Similar results are seen while modeling sample 646, which has a 75 Å Si spacer.

SUMMARY

Good quantitative results are achieved in modeling the inversion layer mobility of Ge_xSi_{1-x} buried channel pMOSFETs at room temperature by assuming that the surface scattering is inversely proportional to the square of the average separation of the holes from the Si/SiO_2 interface. These devices have shown large increases in the *effective* mobility at both 300K (50%) all the way down to 90K (120%) and may prove to be a viable approach for improving pMOS device performance.

ACKNOWLEGEMENTS

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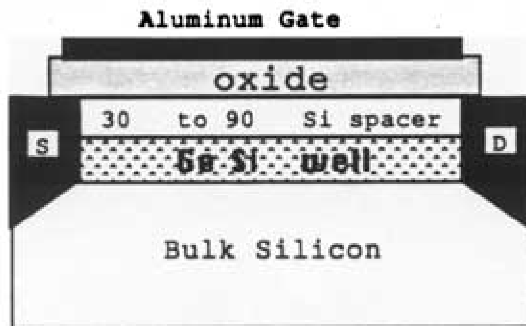

Figure 1: Schematic of GeSi/Si MOSFET. The inversion layer is formed both at the oxide interface and at the GeSi/Si heterojunction.

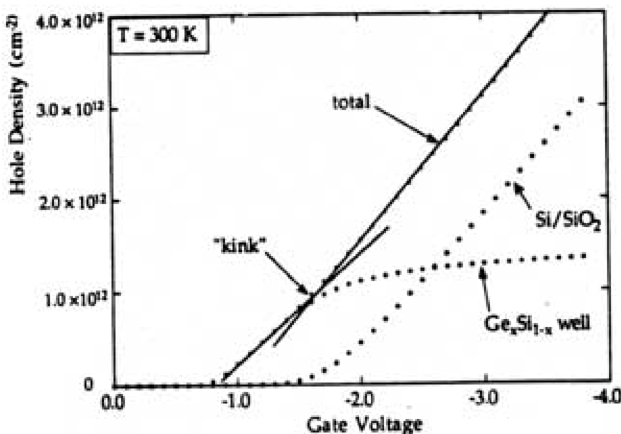

Figure 2: Hole density versus gate voltage from a simulation of sample 649 which has a 105 Å Si spacer layer and a 0.33 Ge fraction in the well.

Sample	Spacer Width (Å)	Ge fraction
control	-	-
646	75	0.33
649	105	0.21

Table I: Description of the samples examined experimentally and numerically in this paper. Both Ge_xSi_{1-x} samples had upper (calculated) hole densities of $\approx 1.2 \times 10^{12}$ cm^{-2}.

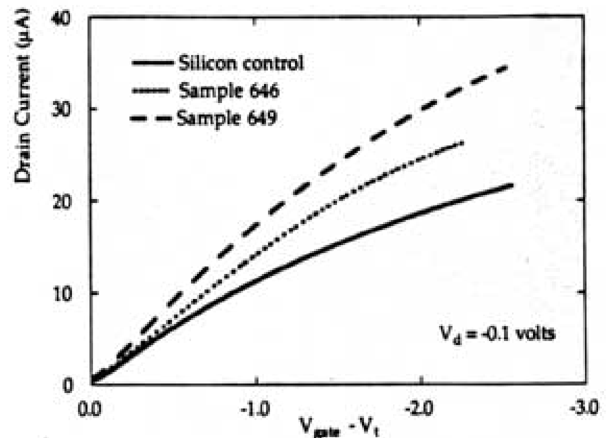

Figure 3: Drain current versus V_{gate}-V_t. Measured on 97μm gate length FETs.

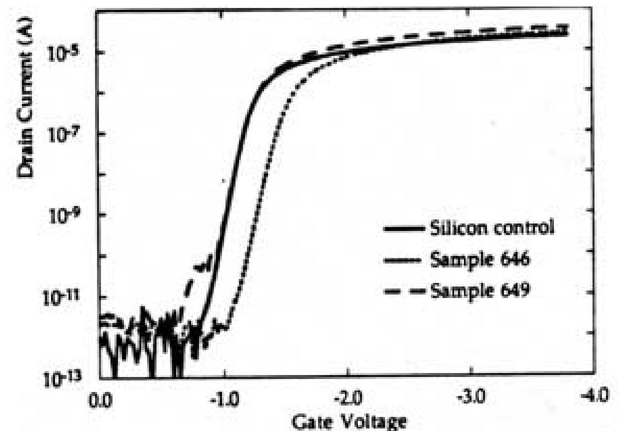

Figure 4: Subthreshold plot of drain current versus gate voltage. All three devices display a suthreshold slope of ≈75mV/decade. Measured using 97μm gate length FETs.

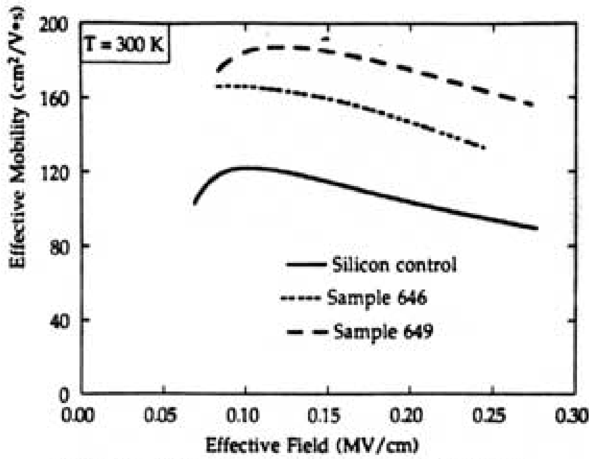

Figure 5: Effective mobility vs. effective field at 300 K. Q_{inv} is $C_{ox} \times (V_g - V_t)$ and $\eta = 1/3$.

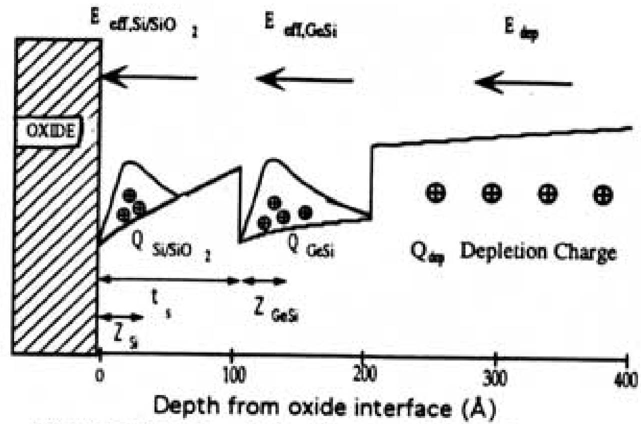

Figure 8: Relation of the effective fields and average spacings to the hole potential in the devices.

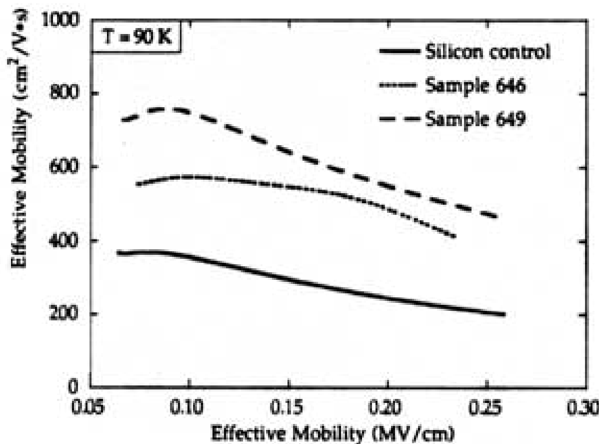

Figure 6: Effective mobility vs. effective field at 90 K. Q_{inv} is $C_{OX} \times (V_g - V_t)$ and $\eta = 1/3$.

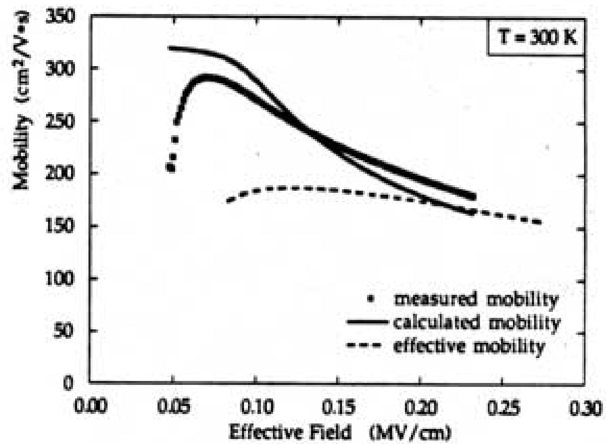

Figure 9: Inversion layer mobility versus effective field at 300K. Experimental and model results for sample 649.

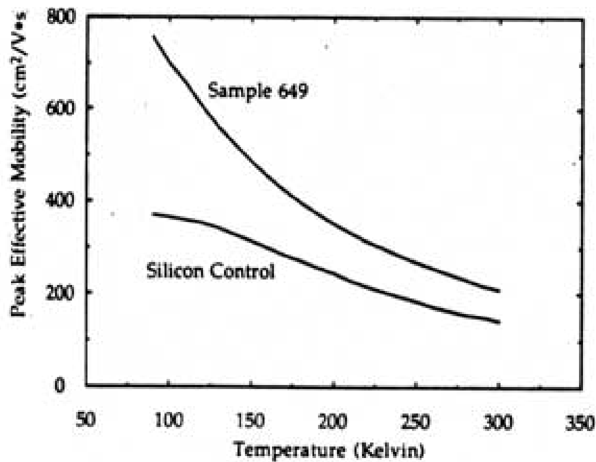

Figure 7: Peak Effective mobility versus temperature.

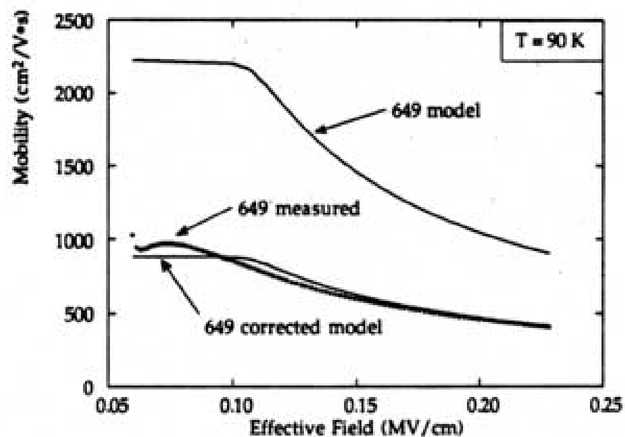

Figure 10: Comparison of the inversion mobility at 90K to model calculations for sample 649. An additional mobility term of 1478 cm²/V•s is added in the "corrected" model curve.