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A Novel Double Base Heterojunction Bipolar Transistor for Low Temperature Bipolar Logic

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Future low temperature applications of electronic devices demand low power consumption which could be achieved by increased functionality of each transistor. Here we report a novel Double-Base Heterojunction Bipolar Transistor (DB–HBT) in the Si/SiGe material system which can operate with high gain in a single-transistor NAND gate at 77K. The device structure is similar to that of a Si/SiGe/Si HBT, except for an intrinsic Si layer inserted into the p-SiGe base. The intrinsic Si layer is used to electrically isolate the two SiGe base layers of an n-Si/p-SiGe/i-Si/p-SiGe/n-Si DB–HBT, because the valence band discontinuity at the SiGe/Si heterojunction acts as a barrier for holes. A key point is that the Si layer introduces only a very small barrier in the conduction band because most of the bandgap difference between unstrained Si and strained SiGe occurs as a valence band offset, ΔE_V.

If a bias is applied between the two p-SiGe base layers, holes are injected by thermionic emission over the valence band discontinuity at the Si/SiGe heterojunction. The magnitude of this current precludes independent base operation of the device at room temperature. At 77 K, however, thermionic emission is sufficiently suppressed to provide isolation between the two base layers. The voltages applied between each of the base layers and the emitter shape the *conduction* band barrier seen by the electrons. Only if *both* bases are forward biased can electrons travel over the base potential barrier from emitter to collector. ("ON" state). If the voltage of either base contact is below the turn-on voltage of the n-Si/p-SiGe junction, no electron current flows ("OFF" state). Operated with a load resistor this device therefore performs the logic NAND function.

The device structure was grown using Rapid Thermal Chemical Vapor Deposition. After the n-Si collector growth at 1000°C, the temperature was kept below 700°C to minimize boron diffusion into the Si barrier while growing the 200Å-thin p-$Si_{0.70}Ge_{0.30}$ bases, the 200Å-thin intrinsic Si barrier, and the n-Si emitter. Four-terminal devices (emitter, base 1, base 2, and collector) were fabricated in a triple-mesa process. The two p-SiGe base layers were contacted by selective chemical etching [1, 2] and the collector by plasma-etching.

At room temperature the intrinsic Si-barrier has no isolating effect and the device works as a single base HBT with an ideality factor of 1.3 for the base current and 1.0 for the collector current and a common-emitter current gain of about 200. At 77 K the device has a maximum current gain of about 100 when operating with both base contacts externally shorted together. Unlike at room temperature, however, the thermionic emission across the p-SiGe/i-Si/p-SiGe barrier is suppressed and the two bases are independent with leakage currents below 5 μA for relative base voltages of less than 0.5 V in a device with a base mesa area of 184 × 184 μm^2. Since the voltages applied at *both* base layers shape the *conduction* band, the collector current injected from the emitter can be controlled independently with either base contact. Only if the voltage on both bases exceeds about 0.8 V does the collector current turn on. It increases with a slope of less than 17 mV/decade which is close to the ideal value of 15.3 mV/decade at 77 K. Using a load resistor of 1 kΩ, switching is demonstrated in a NAND-gate using a single DB–HBT where the two inputs are the base terminals and the output is at the collector terminal.

In summary, a novel DB-HBT device has been demonstrated at 77 K, with high gain and nearly ideal switching behavior in a single-transistor NAND-gate. We acknowledge support of the Office of Naval Research and the National Science Foundation.

[1] P. Narozny *et al.*, IEEE Trans. on Electron Dev., Vol. 36, p. 2363, 1989.
[2] A.H. Krist *et al.*, Appl. Phys. Lett., Vol. 58, p. 1899, 1991.

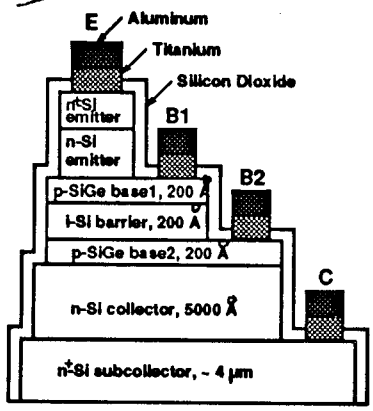

Fig. 1: Device structure of Double-Base Heterojunction Bipolar Transistor (DB–HBT).

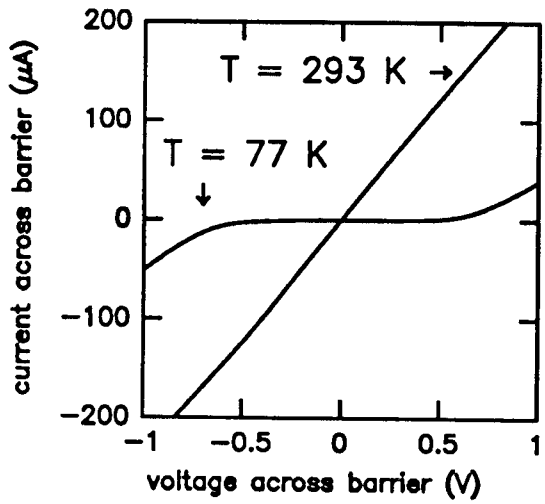

Fig. 3: Measured current-voltage characteristics of p-SiGe/i-Si/p-SiGe barrier at room temperature and at 77 K. Note the low leakage current for voltages below 0.5 V at 77 K where thermionic emission is effectively suppressed.

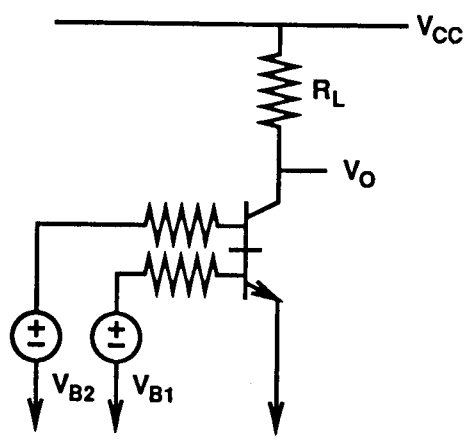

Fig. 5: Circuit diagram for single-transistor NAND-gate. If both inputs are high (see Fig. 2) the current across the load resistor R_L lowers the output voltage V_O.

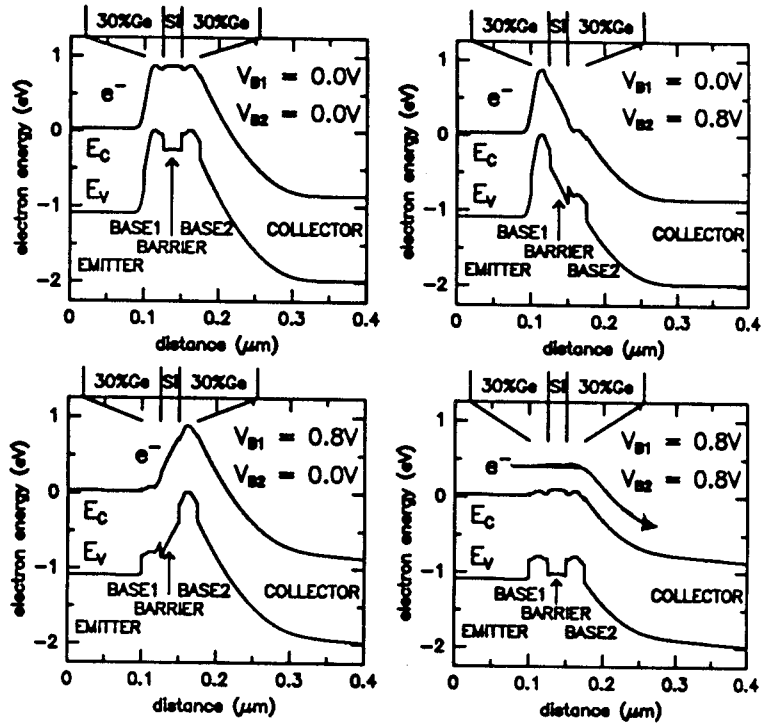

Fig. 2: Calculated band diagrams of DB–HBT for various base voltage inputs.

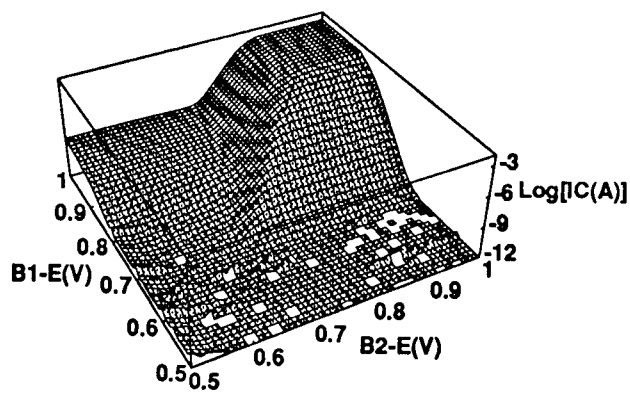

Fig. 4: Measured collector current plotted logarithmically vs. voltage applied at base 1 and base 2. Note the sharp turn-on when *both* inputs are above about 0.8 V.

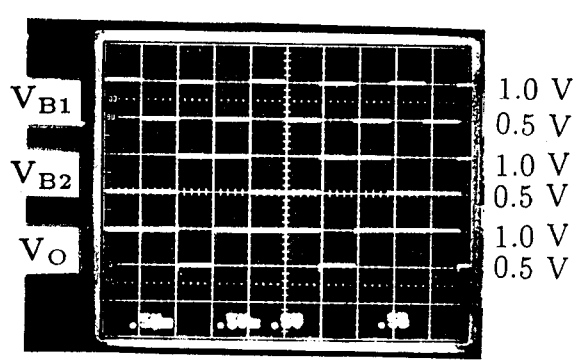

Fig. 6: Measured switching behavior of the circuit of Fig. 5. Both the input and output voltage levels are between 0.5 V (transistor ON) and 1.0 V (transistor OFF).