High mobility electron gases and modulation-doped field effect transistors fabricated in $Si/Si_{1-x}Ge_x$ by rapid thermal chemical vapor deposition

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High mobility *n*-type $Si_{0.62}Ge_{0.38}$/strained Si modulation-doped structures have been fabricated on relaxed graded $Si_{1-x}Ge_x$ buffers by rapid thermal chemical vapor deposition. The mobility and density of the two-dimensional electron gas was studied as a function of spacer thickness of the modulation-doped structure. Mobilities exceeding 40 000 $cm^2/V\,s$ at a density of 1.7×10^{12} cm^{-2} (10 K) and 15 000 $cm^2/V\,s$ at a density of 2.9×10^{12} cm^{-2} (77 K) were observed, giving a record low sheet resistivity of 140 Ω/□ at 77 K. Self-aligned depletion and enhancement mode modulation-doped field effect transistors were fabricated in similar structures using a novel two-step lithography process. Good saturation characteristics with low gate leakage currents were achieved, but the maximum room-temperature transconductance was limited by parasitic source and drain resistances.

I. INTRODUCTION

The $Si_{1-x}Ge_x$/Si material system has been widely investigated for its potential application in heterojunction-based electronic and optoelectronic devices with superior performance over current state-of-the-art silicon devices. Initial devices relied on the valence band offset in strained $Si_{1-x}Ge_x$ layers with respect to silicon substrates. Recently, high mobility two-dimensional (2D) electron gases have been observed in tensilely strained Si layers on relaxed $Si_{1-x}Ge_x$ buffer layers grown by molecular-beam epitaxy (MBE) and ultrahigh vacuum chemical vapor deposition (UHVCVD).[1-3] The strained Si/SiGe buffer provides a conduction band offset and confines the electrons provided by modulation doping to the Si. In this article, we present the first results of high mobility electrons in modulation-doped structures and field effect transistors (MODFETs) prepared by rapid thermal chemical vapor deposition (RTCVD), a non-UHV technique. High carrier densities have been achieved without excessive degradation of the mobility. The lowest reported sheet resistivities at 77 K (140 Ω/□) were obtained.

II. MATERIAL GROWTH AND CHARACTERIZATION

All samples used in this study were grown by RTCVD. The growth system consists of a cold wall quartz tube with a loadlock. The wafer is supported on a quartz stand and heated by tungsten halogen lamps. The silicon active layers are typically grown at 700 °C using dichlorosilane while the $Si_{1-x}Ge_x$ alloy layers are grown at 625 °C using germane, and wafer temperature is accurately determined by monitoring infrared transmission through the wafer. Further details of the growth system and the temperature measurement setup can be found in Ref. 4. Modulation-doped heterojunctions in this work had a structure shown in Fig. 1. The substrates used were 4 in. lightly doped *p*-type wafers and the growth sequence is as follows. After an initial high temperature silicon layer, the relaxed buffer is grown by grading the germanium concentration from 0% to 38% over a thickness of 0.5 μm followed by a 1.0 μm thick uniform $Si_{0.62}Ge_{0.38}$ layer. The sample is then annealed *in situ* at 800 °C for 1 h. Finally, the 75 Å active silicon channel is grown at 700 °C followed by an undoped spacer and a heavy $\sim10^{19}$ cm^{-3} phosphorous-doped 300 Å $Si_{0.62}Ge_{0.38}$ cap. Cross-sectional transmission electron microscopy (TEM) revealed a dense network of misfit dislocations in the relaxed buffer and the substrate, with fewer dislocations in the top uniform layer, similar to observations reported by other workers.[2,5] X-ray analysis showed the buffer to be fully relaxed and the threading dislocation density at the surface was determined from electron beam induced current (EBIC) and TEM imaging to be 10^7 cm^{-2}.

III. ELECTRICAL MEASUREMENTS

For electrical characterization, cleaved samples in the Van der Pauw geometry and lithographically defined Hall patterns were used. A gold–antimony (0.6% Sb) alloy was evaporated and lifted-off in the contact regions and annealed at ~350 °C for 15 min. This resulted in low resistance ohmic contacts at liquid helium temperatures. The results of Hall measurements are displayed in Fig. 2 for three samples with the same structure shown in Fig. 1, but different spacer widths. The mobility increases monotonically for all the samples with decreasing temperature, reaching 42 000 $cm^2/V\,s$ at 10 K for a spacer width of 80 Å. At the same time, the carrier density decreases and saturates at low temperatures with no evidence of freeze-out. This indicates the presence of a degenerate 2D electron gas (2DEG) confined in the strained silicon channel. At 77 K for a 40 Å spacer, a 2DEG of density 2.9×10^{12} cm^{-2} and mobility 15 000 $cm^2/V\,s$ was obtained, which yields a sheet resistivity of 140 Ω/□, the lowest yet reported in these type of structures. The clear trends of increasing low temperature mobility and decreasing carrier density with spacer thickness are expected and will be discussed later.

To further study the quality of the 2D electron system, we did magnetotransport experiments at liquid helium

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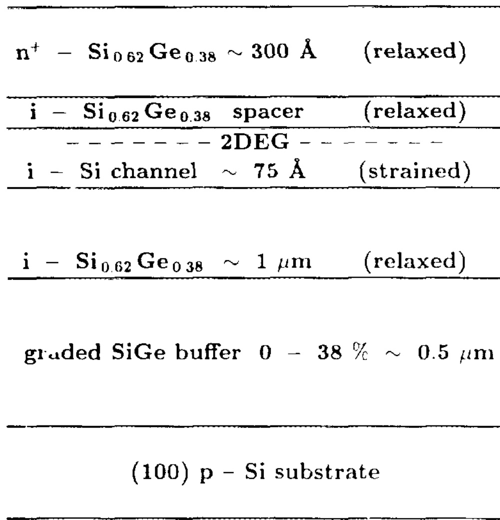

FIG. 1. Sample structure for the modulation-doping experiments. The doping level was $\sim 10^{19}$ cm^{-3} and the spacer was varied from 0 to 80 Å.

temperatures using a high field superconducting magnet. As shown in Fig. 3, well-defined Shubnikov–de Haas oscillations in the longitudinal resistance and quantized Hall plateaux in the transverse resistance are observed as a function of the magnetic field. The cap layer was slightly etched for these experiments to prevent parallel conduction. The oscillations are periodic in 1/B as clearly seen from Fig. 4. A single oscillation frequency indicates that only the lowest quantized level is occupied, even at these carrier densities. At higher fields, the oscillation frequency doubles due to spin splitting of the Landau levels (Fig. 4). Only even integer plateaus are observed in the Hall data at high fields, indicating a valley degeneracy of two. These results can be understood, if we consider the conduction band of the strained silicon channel. The biaxial tensile strain splits the six-fold degeneracy and lowers the two valleys along the growth direction in energy. The electrons in the ground state have therefore a heavy longitudinal mass ($\sim 0.98\ m_0$) and a lighter transverse mass ($\sim 0.19\ m_0$). The carrier

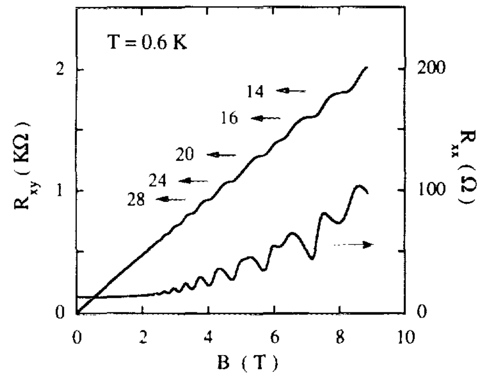

FIG. 3. Longitudinal resistance (R_{xx}) and Hall resistance (R_{xy}) for the sample with spacer 40 Å as a function of the magnetic field. The plateau filling factors ν are given by $R_{xy}=h/e^2\nu$, where e is the electron charge and h is the Planck constant.

density derived from the oscillation frequency, 2.7×10^{12} cm^{-2}, agrees very well with the temperature dependent measurements.

For the same spacer thickness, the carrier densities in our samples are consistently higher than those obtained in Refs. 1 and 2. This is mainly due to the higher germanium content, and therefore, a larger conduction band offset. Using a simple electrostatic equilibrium model, we estimate a band offset of 240 meV, in agreement with theoretical calculations.[6] However, we see only lowest subband occupation in our 75 Å single quantum well (QW) with 2.7×10^{12} cm^{-2} carriers in contrast to previously reported experimental observations and calculations.[7] Since the samples in Ref. 7 had a multiple QW structure, each with its own 2DEG, nonuniform densities in the QWs rather than occupation of the second quantized level, could have given rise to multiple periods in the Shubnikov–deHaas oscillations. Furthermore, the large effective masses coupled with a 10–20 meV ambiguity in the band offsets can lead to sizable errors in estimates of the energy levels and the Fermi-level position, which make calculations of the exact number of occupied levels difficult. Although the mobilities we obtained are comparable to the UHVCVD

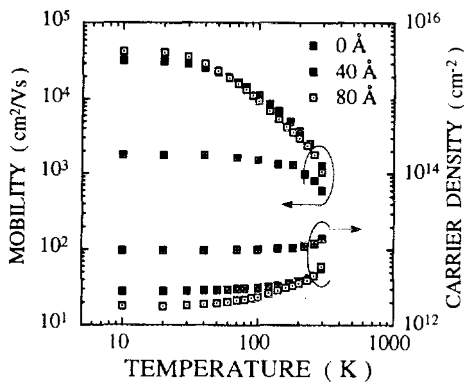

FIG. 2. Mobility and carrier density as a function of temperature for three samples with spacer thicknesses 0, 40, and 80 Å. All samples had the structure shown in Fig. 1.

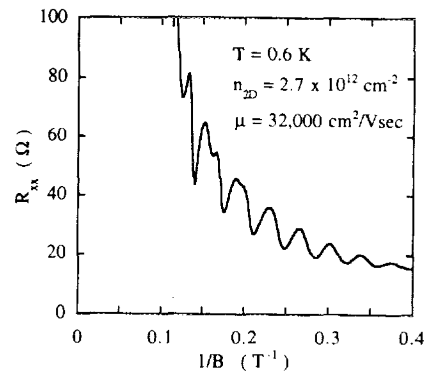

FIG. 4. Longitudinal resistance shown in Fig. 3 plotted as a function of inverse magnetic field. The oscillations are periodic in $1/B$ with a single frequency showing only lowest level occupation at this carrier density.

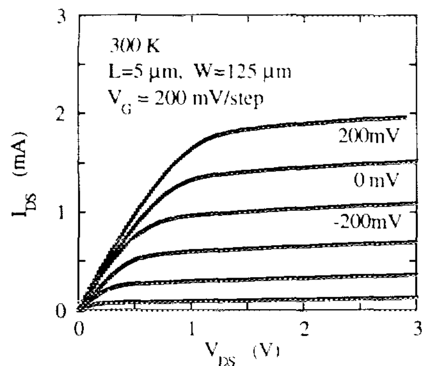

FIG. 5. Drain current (I_D) as a function of the source-drain bias (V_{DS}) for gate voltages from −800 to +200 mV. The threshold voltage is ~1 V and the gate current was less than 10 μA throughout this bias range.

results,[3] they are lower than the best MBE results[2] by a factor of 4. Calculations show that this is consistent with a higher background doping (~10^{16} cm^{-3}) in our system. The quality of the relaxed buffer in terms of a higher grading rate (80%/μm) and threading dislocation density could also play a role.

IV. DEVICE PROCESSING AND RESULTS

To control the density of the 2DEG for MODFET devices, it is necessary to form a good Schottky barrier and deplete the doped layer completely. Therefore, we grew modulation-doped structures similar to those described above, but with lower doping (~3–5$\times 10^{18}$ cm^{-3}) and an undoped cap layer (200–400 Å). We fabricated MODFETs using a novel two-step optical lithography process which yielded a self-aligned structure. First, a 1000 Å thick aluminum gate was deposited and followed by lithography to define the source and drain regions. We used a chlorobenzene soak step in this lithography to leave a photoresist "overhang" after developing. The gate metal was etched from the source and drain regions and marginally overetched. Gold–antimony was then evaporated and lifted-off, leaving source and drain contacts. The gate is automatically aligned to these regions and separated by the photoresist overhang and the aluminum overetch which can be controlled and reproduced. Source-to-gate separations under 1 μm can be achieved in this way without sophisticated alignment tools. A second lithography step defined the gate region. Using the resist and Au:Sb contacts as masks, a self-aligned mesa was finally etched to isolate the devices.

The devices were electrically characterized at room temperature and low temperatures. Good saturation characteristics were observed and gate leakage currents at 300 K were less than 10 μA at $V_G = -1$ V for 100$\times$100 μm^2 gate areas. This is indicative of the excellent control of the n^+-doping turnoff available by RTCVD. Shown in Fig. 5 are measured room-temperature characteristics for a 5 μm $\times$125 μm depletion device with a 300 Å gate-to-channel separation and a 2 μm gate-to-source separation. The threshold voltage is −1 V and enhancement mode operation up to +400 mV is possible without gate leakage in excess of 10 μA. The maximum transconductance, however, is 20 mS/mm at room temperature, and 30 mS/mm at 77 K, considerably less than that expected from the structural design. By studying devices with different gate lengths, it was found that the transconductance is severely limited by source and drain access resistances, even with the self-alignment technique. Further work is in progress to improve contact resistivities and reduce parasitics.

V. SUMMARY

In conclusion, high mobility strained $Si/Si_{1-x}Ge_x$ modulation-doped 2D electron systems have been fabricated on relaxed buffers by RTCVD. To achieve high carrier densities for MODFETs, we used higher doping densities and germanium concentrations without significant degradation of low temperature mobilities. In this way, we were able to obtain record low sheet resistivities (140 Ω/□ at 77 K). To reduce parallel conduction, it is necessary to use thin, heavily doped layers. Future work in this direction should concentrate on delta-doping studies in $Si_{1-x}Ge_x$. We have also fabricated MODFETs using a novel completely self-aligned two-step lithography process. Submicron devices can be fabricated using an advanced version of this process without sophisticated lithography and alignment tools.

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