# Limited Reaction Processing: *In-situ* Epitaxial Silicon-Thin Oxide-Polysilicon Layers for MOS Transistors

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Limited reaction processing is a new technique for the *in-situ* growth and deposition of multiple thin high-quality semiconductor and insulator layers. We report here on the *in-situ* growth of epitaxial silicon-thin oxide-doped polysilicon structures and describe the performance of n- and p-channel MOSFET's made using these layers ($t_{ox}$ = 140 Å, $L_{eff}$ = 0.8 $\mu$m).

The limited reaction processing system basically consists of a quartz tube connected to a low-pressure pumping apparatus [1]. A gas control system can supply several conventional processing gases such as silane, argon, oxygen, diborane, etc. The tube is surrounded by microprocessor-controlled lamp banks which can bring a wafer inside the tube from room temperature to typical processing temperatures (e.g. 1000 °C) in less than three seconds. With such rapid temperature control, the gas flows are first stabilized with the wafer at room temperature, and the surface reaction is then switched on and off by controlling the wafer temperature. By changing the process gases between high-temperature cycles, multiple individual rapid thermal processing steps, such as silicon epitaxy [1] or oxidation [2], can now be performed sequentially *in situ*, i.e. without disturbing the wafer or breaking the vacuum seal of the system.

To avoid the inevitable interface contamination that occurs when wafers are transported from one reactor to another, an *in-situ* process for MOSFET's was developed. Starting with heavily doped substrates, active area holes were first opened up in a field oxide in a conventional manner. The wafers were then loaded into the LRP apparatus and, following an *in-situ* pre-cleaning step, were subjected to three sequential growth or deposition cycles: (1) silicon epitaxy ($t_{si}$ = 1.5 $\mu$m), (2) oxidation ($t_{ox}$ = 140 Å), and (3) doped polysilicon deposition. For device isolation, the epitaxial growth process was adjusted to be selective, i.e. the growth occured only in the oxide holes. Following the high-temperature step for epitaxy, the process gases were changed and a thin gate oxide was grown at 1100 °C. During a third high-temperature step, a layer of heavily doped polysilicon was deposited. The wafers were then removed from the processing chamber, and conventional processing was used to convert the multi-layer MOS structures into both p- and n-channel MOSFET's (minimum $L_{eff}$ = 0.8 $\mu$m). The MOSFET's were well-behaved and exhibited excellent threshold uniformity. In general, the advantages of interface cleanliness offered by multi-layer *in-situ* processing could be important for the uniformity and yield requirements demanded by ULSI.

1. C.M. Gronet, K.E. Williams, and J.F. Gibbons, Appl. Phys. Lett. **47**, 721 (1985).
2. J. Nulman, J.P. Krusias, and A. Gat, IEEE Electron Dev. Lett. **EDL-6**, 205 (1985).