Modeling of Leakage Current Distributions in Series Connected Polysilicon Thin Film Transistors

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Leakage current is an important parameter in thin film transistors (TFTs) for achieving gray scales in Active Matrix Liquid Crystal Displays (AMLCDs)[1]. Leakage regulation is especially important in polysilicon (Poly-Si) TFTs, where the leakage is significantly greater than in their amorphous silicon counterparts. To reduce the leakage current, it is a common practice to place two poly-Si TFTs in series[2], as shown in Figure 1, which may reduce the leakage current by over an order of magnitude.

In this work, we show how leakage current in a series connected pair can be analytically predicted from the I-V characteristics of a single FET for the first time, and how the leakage current distribution of single transistors may affect the distribution of the series connected devices. These implications are important for estimating the pixel yield in AMLCDs from single device characteristics.

For $V_{GS} < 0$ and $V_{DS} > 2$ V, n-channel poly-Si TFT characteristics (Fig. 2) can be typically modelled as:

$$I_D = ce^{aV_{DS} - bV_{GS}} \qquad (1)$$

When N transistors are placed in series with the same gate voltage, this model can be applied to each one with an appropriately defined V_{GS} and V_{DS}. Since the drain currents in all transistors must be equal, one can use the model to solve a recursive relation to find the drain voltage on the bottom transistor ($V_{D,1}$) compared to the total drain voltage (V_{DD}).[3] In the case of two transistors in series, this ratio reduces to:

$$\eta = \frac{V_{D,1}}{V_{DD}} = \frac{a}{2a - b} \qquad (2)$$

Note that within the limits of the model, the drain voltage reduction in the negative gate voltage range on the lower transistor is independent of the gate voltage. If we then use this reduced drain voltage and Eq'n (1) to calculate the leakage current of a series connected pair of identical transistors ($I_{L,2}$) compared to that in a single transistor ($I_{L,1}$), one finds:

$$\frac{I_{L,2}}{I_{L,1}} = e^{-a(a-b)V_{DD}/(2a-b)} \qquad (3)$$

Note that for a given V_{DD}, this implies a reduction in leakage current independent of V_G, which is indeed observed in practice (Fig. 3). Note also in Fig. 3 that the predicted

leakage current reduction is a factor of 19 (using a ~ 1.1 and b ~0.7), in good agreement with the experimentally observed value of ~16 at Vg = -8 V.

Because statistical variations from one TFT to the next are inevitable in fabrication, we extend the leakage current modeling to dissimilar TFT pairs. Applying (1) and setting the two drain currents equal, we derive an expression for leakage in the series pair.

$$I_{D,SERIES} = c' e^{a'V_{DD} - b'V_G} \qquad a' = \frac{a_1 a_2}{a_1 + a_2 - b_2} \qquad b' = \frac{a_1(b_2 - b_1)}{a_1 + a_2 - b_2} + b_1 \qquad c' = c_1 e^{\frac{a_1 \ln\left(\frac{c_1}{c_2}\right)}{a_1 + a_2 - b_2}} \quad (4)$$

Parameters a_1, b_1, c_1 and a_2, b_2, c_2 refer to the a, b, and c parameters of the lower and upper transistors of the series connected pair respectively. To examine the effect of statistical variations, we have assumed that both a's, b's and ϕ's ($\phi \equiv \log_{10} c$) all vary with Gaussian distributions. We also assume that the standard deviations in the parameters are the same for each of the two transistors and are σ_a, σ_b and σ_ϕ, and then use (4) to predict the variation in $I_{D,SERIES}$.

Looking independently at the effect of variations in a, b, and c of the individual transistors, one finds a surprising result. For simplicity, we have first assumed a variation in only parameters a or c. Note that the predicted distribution of the $\log_{10} I_{D,SERIES}$ is less than or at most approximately equal to that of a single transistor, depending on the degree of correlation assumed between the two different transistors (Fig. 4, 6). A tightening of the distribution for the series-connected pair would be advantageous for yield considerations. However, in the case of only a variation in b, the variation in $\log_{10} I_{D,SERIES}$ is actually greater than in the individual transistor, even if the two transistors are not correlated. (Fig. 5) Note in practice the situation will be more complicated because of cross-correlations between the parameters of a single TFT and variations of all parameters at once.

Shown in Figures 7, 8, 10 and 11 are the measured statistical data for two different high-temperature long-channel (L > 8μm) poly-Si TFT processes from two different laboratories, for both single transistors and series-connected pairs. The leakage current reductions in the two cases are factors of ~2 and ~7, respectively, agreeing well with the predicted values using (3) of 2.2 and 10.0. However, in the first case a narrowing of the leakage current distribution is seen, while in the second case a substantial broadening is observed (Fig's. 9, 12). These two experimental results qualitatively demonstrate the two limits of the effects predicted in Fig's 4-6. Work is currently in progress to quantitatively model experimental distributions of series pairs from known distributions of single TFTs.

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[2] S. Morozumi, *et al.*, Society for Information Display (SID) Digest, p. 278 (1985).
[3] J.C. Sturm, *et al.*, IEEE Transactions on Electron Devices, Vol. 42, No. 8, pp. 1561-1563 (1995).

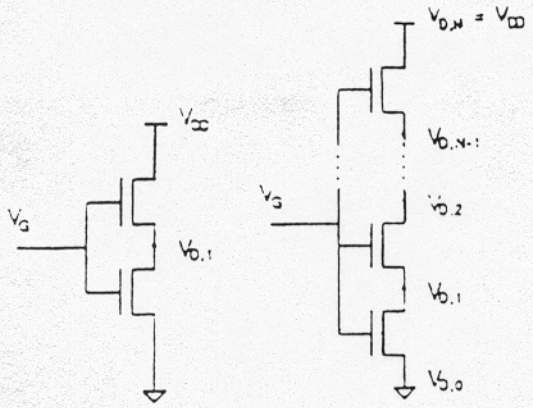

Fig. 1. Circuit diagram of multiple TFT's in series to reduce leakage current.

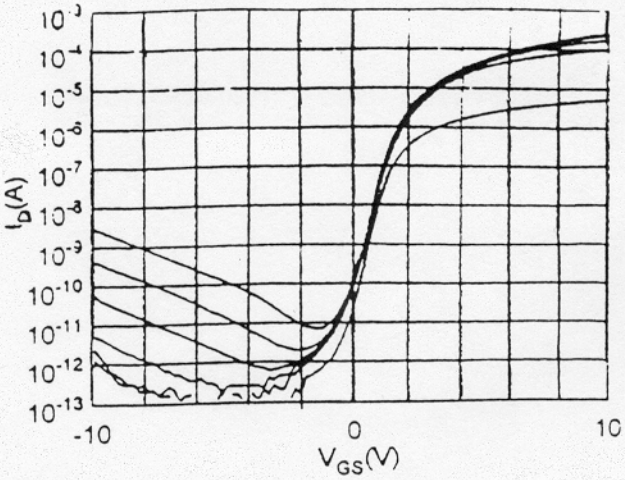

Fig. 2. Measured I-V characteristics of a 40μm/20μm poly-Si TFT demonstrating leakage current for $V_{GS} < 0$. V_{DS} curves are from 0.1 V to 10.1 V in 2 V steps.

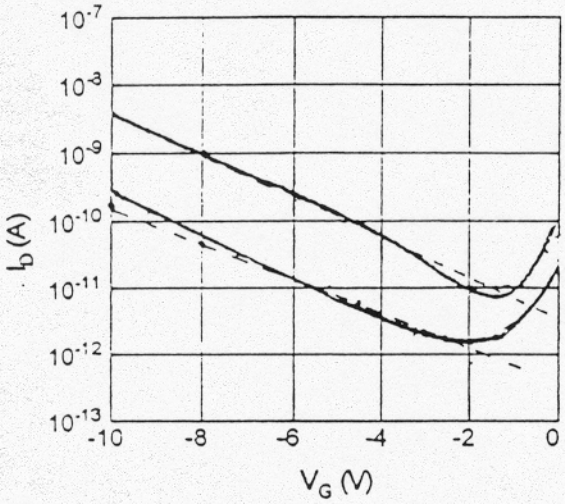

Fig. 3. Experimentally measured (solid lines) and modeled result (dashed lines) for single TFT's (top) and 2 in series (bottom) for V_{DD} = 10.1 V.

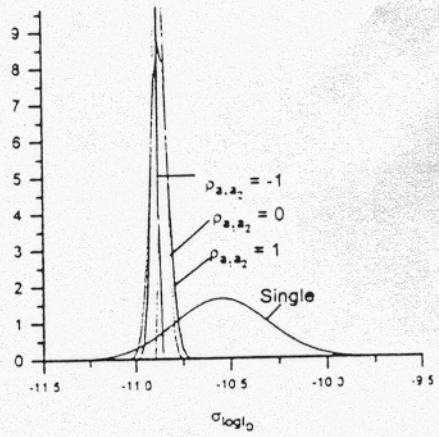

Fig. 4. Predicted leakage current distribution for a single transistor and two transistors in series with varying degrees of correlation. Assumed mean values of a, b, ϕ of .72, .63, -16.44, and σ_a, σ_b, σ_ϕ of .057, 0, 0.

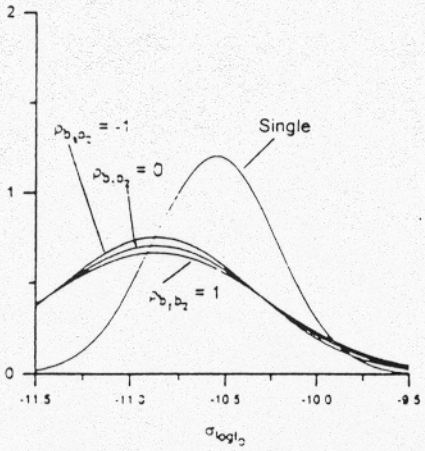

Fig. 5. Predicted leakage current distribution for a single transistor and two transistors in series with varying degrees of correlation. Assumed mean values of a, b, ϕ of .72, .63, -16.44, and σ_a, σ_b, σ_ϕ of 0, .076, 0.

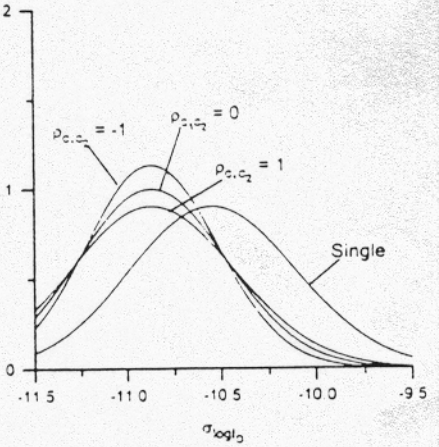

Fig. 6. Predicted leakage current distribution for a single transistor and two transistors in series with varying degrees of correlation. Assumed mean values of a, b, ϕ of .72, .63, -16.44, and σ_a, σ_b, σ_ϕ of 0, 0, .44.

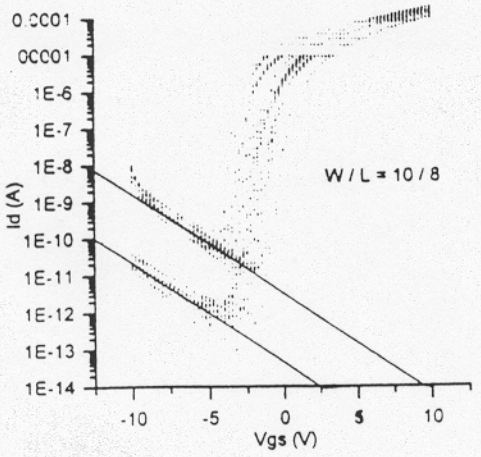

Fig. 7. Measured leakage current curves and fits to the single transistor model for V_{DS} = 9, 15 V for twenty single TFTs from process 1.

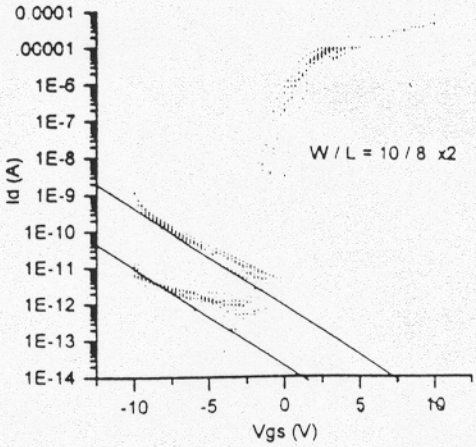

Fig. 8. Measured leakage current curves (and modelled predictions of means) for ten series connected pairs from process 1 on same chip as data of Fig. 7. V_{DS} = 9, 15 V

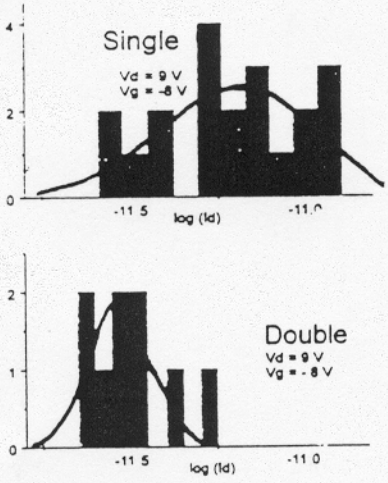

Fig. 9. Histograms and best Gaussian fits of $\log_{10}I_{leak}$ for data in Fig's 7-8.

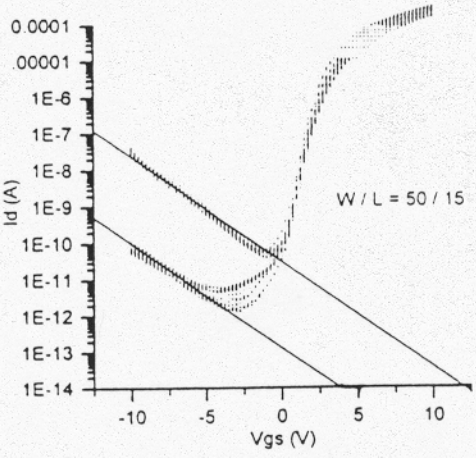

Fig. 10. Measured leakage current curves and fits to the single transistor model for V_{DS} = 6, 12 V for eighteen single TFTs from process 2.

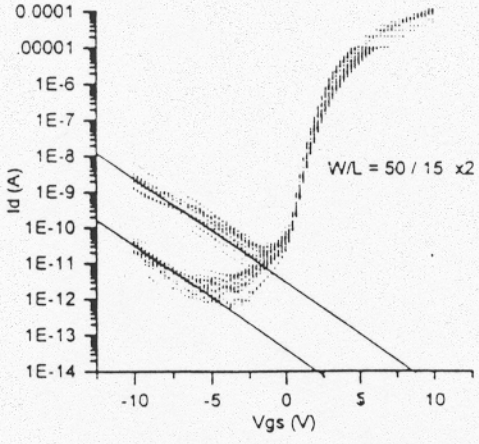

Fig. 11. Measured leakage current curves (and modelled predictions of means) for twenty series connected pairs from process 2 on same chip as data of Fig. 10. V_{DS} = 6, 12 V

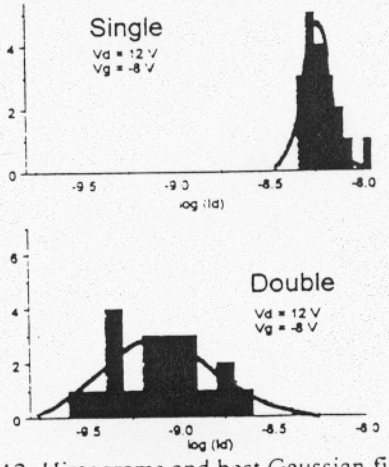

Fig. 12. Histograms and best Gaussian fits of $\log_{10}I_{leak}$ for data in Fig's 10-11.