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Dependence of Transconductance on Substrate Bias in Ultra-thin Silicon on Insulator MOS Transistors

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ABSTRACT

A simple model is presented to explain the dependence of transconductance on substrate bias in ultra-thin silicon-on-insulator MOS transistors. Good agreement with experimental data is found. The model can also be used to predict the dependence of transconductance with underlying oxide thickness.

Recently it has been shown that the transconductance of fully-depleted SOI MOSFET's on thick underlying oxides can exceed that of comparable bulk transistors. In this letter, a simple model is presented to explain the dependence of the transconductance of fully-depleted SOI MOSFET's on substrate voltage. Supporting data is also presented. The model can also be used to predict the dependence of transconductance on underlying oxide thickness.

In a simple picture, a segment of the channel in an SOI MOS structure may be analyzed as shown in Fig. 1. The channel potential is coupled to the top gate via gate oxide capacitance C_{gate}. In the ideal case, as in a fully depleted SOI film on a very thick substrate, there is no other coupling to the channel. However in most FET's, there is a parasitic capacitance coupling to the channel. With a fully depleted SOI film, any new electric field lines from changing the channel voltage will terminate at the substrate underneath the underlying oxide. We may then define an effective substrate capacitance C_{subs} given by the series combination of the capacitance of the depleted SOI body and of the underlying oxide,

$$\frac{1}{C_{subs}} \equiv \frac{t_{box}}{\epsilon_{ox}} + \frac{t_{SOI}}{\epsilon_{Si}} \tag{1}$$

where ϵ_{ox} and ϵ_{Si} are dielectric constants of silicon and oxide, respectively, and t_{box} and t_{SOI} are the underlying oxide and SOI thicknesses, respectively. This C_{subs} is then a parasitic capacitance which couples the channel to the substrate (fig. 1). The analogous capacitance in a bulk transistor is the substrate space-charge layer capacitance.

To develop a model for transistor current, one needs an expression for channel charge Q_{ch} as a function of gate voltage (V_G) and channel voltage (V_{ch}). Defining threshold voltage (V_t) as the gate voltage required for $Q_{ch} = 0$ when $V_{ch} = 0$, it follows from fig. 1(a) that

$$Q_{ch}(V_{ch},V_G) = (V_G - V_t - V_{ch})\, C_{gate} - V_{ch} C_{subs}. \tag{2}$$

(We have assumed that substrate voltage is held fixed.) This expression can then be used

in the usual gradual channel approximation formulation to yield an expression for drain current I_D,

$$I_D = \frac{W}{L} \mu \left[(V_G - V_t) V_D C_{gate} - ½ (C_{gate} + C_{subs}) V_D^2 \right] \quad (3)$$

To determine drain saturation current, one needs to set $Q_{chan} = 0$ to find drain saturation voltage:

$$V_{DSAT} = V_{ch} |_{Q_{ch}=0} = (V_G - V_T) \frac{C_{gate}}{C_{gate} + C_{subs}} = \gamma(V_G - V_T) \quad (4)$$

$$\gamma \equiv \frac{C_{gate}}{C_{gate} + C_{subs}} \quad (5)$$

Note we have defined an efficiency factor γ which is always ≤ 1. Substituting (3) into (2) and combining terms yields drain saturation current and transconductance

$$I_{DSAT} = \gamma \frac{W}{2L} \mu (V_G - V_t)^2 \quad (6)$$

$$g_m = \frac{\partial I_{DSAT}}{\partial V_G} = \gamma \frac{W}{2L} \mu (V_g - V_t) \quad (7)$$

The expression for saturation current and transconductance are surprisingly simple; they are reduced from their ideal maximum value by the factor γ. For a fully depleted SOI FET with a gate oxide of 250 Å , SOI thickness of 1000 Å , and an underlying oxide of 3500 Å , one finds $\gamma = 0.94$.

If one applies a very negative substrate bias to normally fully depleted n-channel SOI FET, the back interface will become accumulated with holes. The potential of this interface will be pinned close to the source voltage, since if it were positively biased holes would be injected into the source [2]. (We assume drain voltages small enough to avoid the "kink" effect.) Because the potential at the back interface is now pinned, the effective substrate capacitance C_{subs} should now be replaced by simply the capacitance of the SOI film body, $C_{SOI} = \frac{\epsilon_{ox}}{t_{SOI}}$ (fig. 1b). The above derivation still holds, except that now

$$\gamma \equiv \frac{C_{gate}}{C_{gate} + C_{SOI}} \tag{8}$$

For the parameters described above, this would reduce γ to 0.57, and significantly degrade transconductance.

As an experiment, n-channel MOSFET's were fabricated in SOI prepared by oxygen implantation. The device parameters were corresponded to those just described, and $W/L = 50\mu m/8\mu m$. Drain saturation current is shown in fig. 2 for several substrate biases. Because threshold voltages change with substrate bias, the data is plotted vs. $V_G - V_t$ for a fair comparison. To analyze this data, it is necessary to have independent information on the charge state of the lower SOI interface. This may be inferred by measurements of threshold voltage vs. substrate bias (fig. 3) [3]. At $V_{subs} = 0$, the threshold voltage depends strongly on substrate bias, indicating full depletion of the SOI film near the source. The SOI film will then also be depleted for higher channel voltages, and thus throughout the entire FET. Equation (5) gives $\gamma = 0.94$, and as seen in figure 2, this case of full depletion yields the highest transconductance.

For $V_s \leq -10V$, the back interface is accumulated at the source, (little dependence of V_t on V_{subs}). As one moves to higher channel voltages, keeping the back interface accumulated will of course require more negative substrate bias since the potential at the back interface can not move by more than a few kT/q. The amount of this extra substrate bias is easily calculated by considering the relative capacitances of the SOI film and the underlying oxide. As the channel voltage is increased by ΔV_{ch} from zero, an increase in substrate bias by ΔV_{SUBS} from -10V will be required to maintain an accumulated backside, where $\Delta V_{SUBS} = -\Delta V_{ch} \frac{t_{box}}{t_{SOI}} \frac{\epsilon_{Si}}{\epsilon_{SiO_2}}$. For the experimental device measured here, this relationship corresponds to $\Delta V_{SUBS} = -10.5 \cdot V_{ch}$. Thus for a -40 V substrate bias, the backside will be accumulated up to channel voltages of about 3 V (which includes all data points in Fig. 2.), and the simple model based on figure 1(b) and the reduced γ of (8) may be used. In Fig. 3, the device with a -40 V substrate bias (fully

accumulated backside) has a transconductance that is 0.64 of that of the fully depleted device (zero substrate bias). According to the simple theory outlined earlier, this ratio should be equal to the ratio of the efficiency factors γ's of the two transistors. Taking the ratio of $\frac{0.57}{0.94} = 0.59$, we find good agreement with the experimentally observed ratio. For -20V on the substrate, the back interface will be accumulated for channel voltages up to ~ 1 V, and the portion of the channel above 1 V will have a depleted backside. Indeed, for a substrate voltage of -20 V, the drain current for $V_G - V_t = 1$ is close to that of -40 V on the substrate (accumulated backside), but as channel voltage increases ($V_G - V_t$ increases), drain current rises faster than the accumulated backside case (more like the fully depleted case).

Through the efficiency factor γ, Equation (4) can also be used to predict the dependence of device performance in the fully depleted case on underlying oxide thickness. For a gate oxide thickness of 250 Å and an SOI thickness of 1000 Å , the dependence of drain current on oxide thickness is shown in figure 4. For the 3500 Å underlying oxide

in this experiment, the drain current is 0.94 of its maximum (which would be acheived with an infinitely thick oxide). However, an oxide thickness of 1000 Å would reduce γ to 0.77. Our analysis has assumed negligible depletion in the SOI substrate, as would be caused by a heavily doped substrate or an accumulated substrate interface. This is the worse case analysis since any substrate depletion would reduce C_{subs}. However in a real SOI CMOS circuit this worst case will probably be realized for one of the two transistor types.

In summary, a simple model utilizing an efficiency parameter γ has been developed to explain the dependence of transconductance in fully depleted SOI FET's on substrate voltage and oxide thickness. Good agreement with data is found. The results directly imply that consideration of the underlying oxide thickness and the charge condition of the lower SOI interface are very important in the design of high performance fully depleted SOI FET's.

Acknowledgement

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References:

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2. J.P. Colinge, "Reduction of kink effect in thin-film SOI MOSFET's," *IEEE Electron Device Lett.,* vol. EDL-9, pp. 97-99, 1988.

3. H.-K. Lim and J.G. Fossum, "Threshold voltage of thin-film silicon-on-insulator (SOI) MOSFET's," *IEEE Trans. Electron Devices,* vol. ED-30, pp. 1244-1251, 1983.

Figure Captions

Figure 1: Capacitor model for fully depleted SOI FET with a depleted SOI film and depleted backside (a), and with a depleted SOI film but accumulated backside (b).

Figure 2: Square-root of drain current vs. $V_G - V_t$ for a single SOI FET as a function of substrate voltage. Gate oxide thickness is 250 Å, underlying oxide is 3500 Å, SOI thickness is 3500 Å, film doping is 10^{17}cm^{-3}, and $W/L = 50\mu m/8\mu m$.

Figure 3: Threshold voltage vs. substrate voltage for the SOI transistors.

Figure 4: Drain current vs. underlying oxide thickness for a fully depleted SOI transistor.

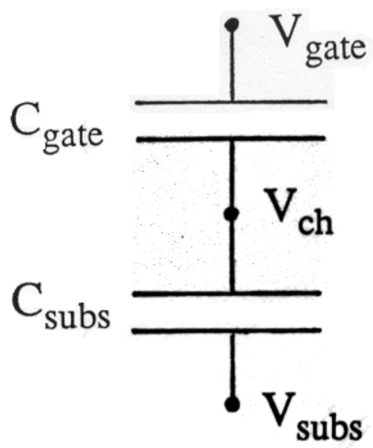


Fig 1(a)

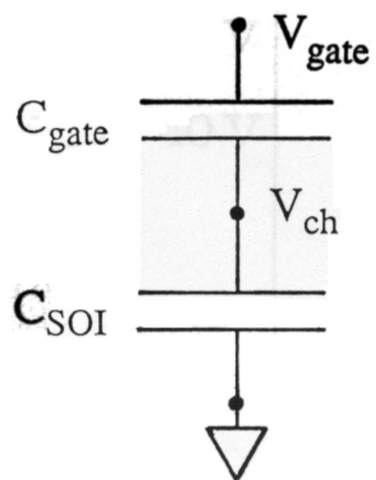


Fig 1(b)

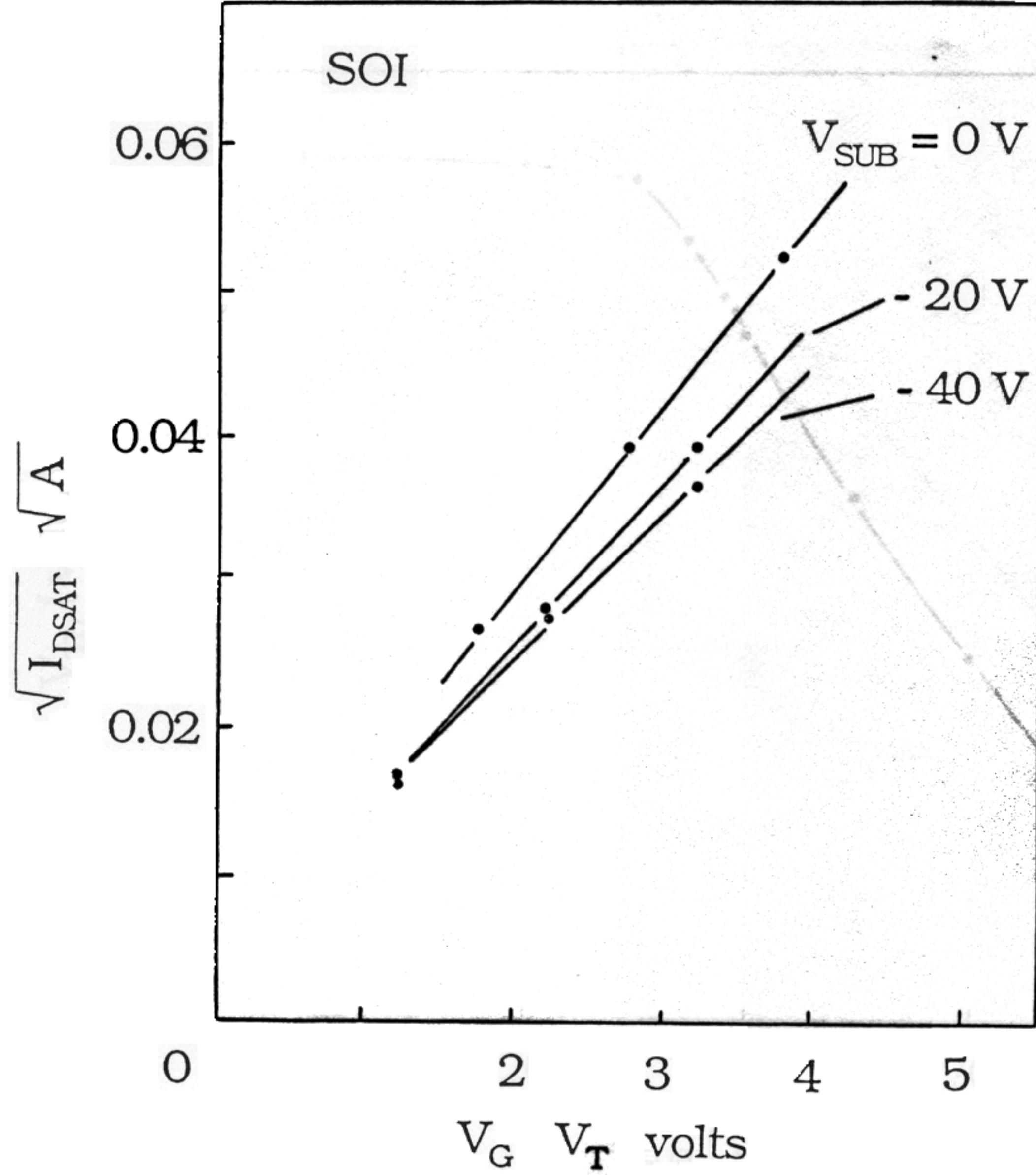


Fig 2

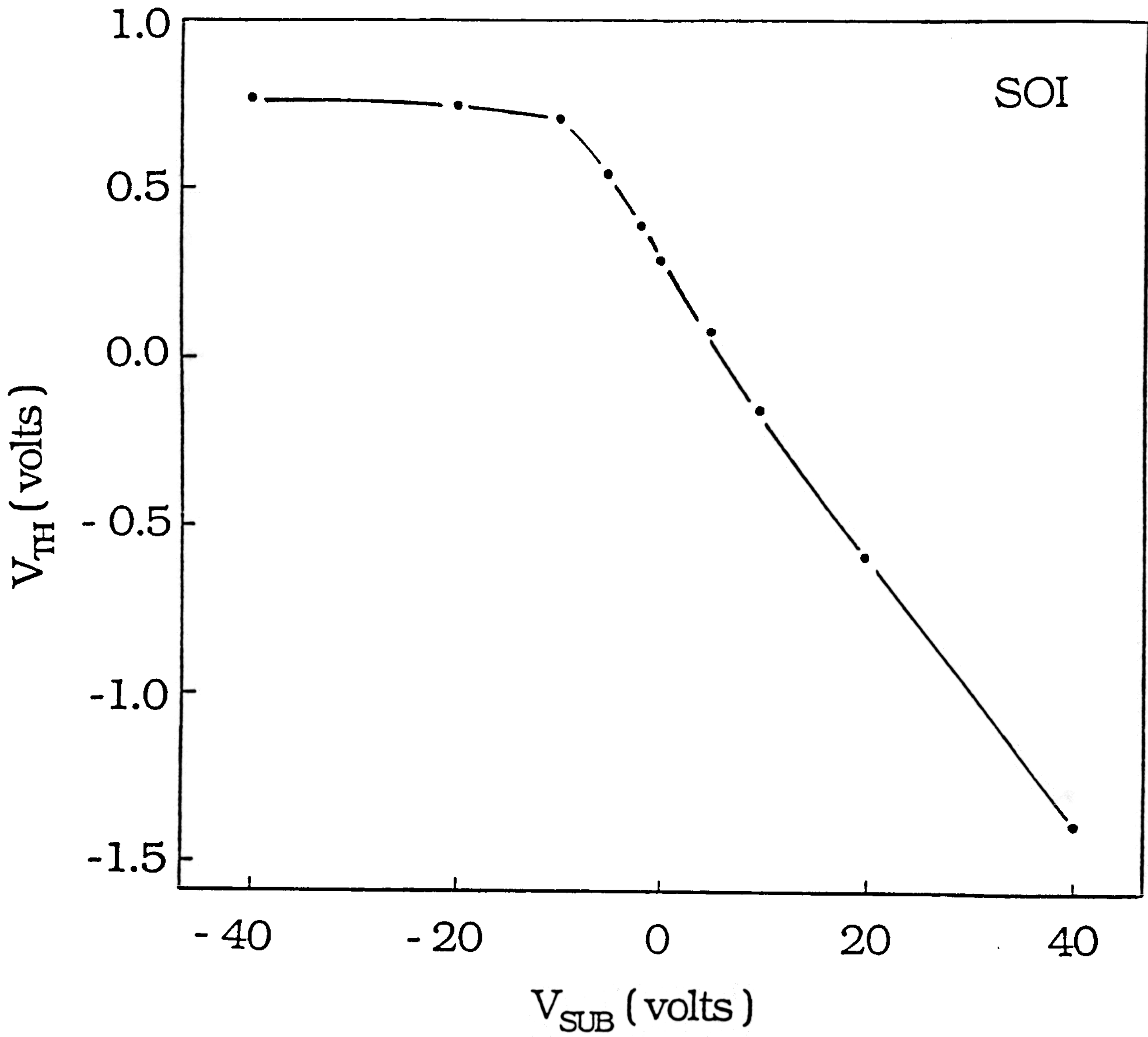
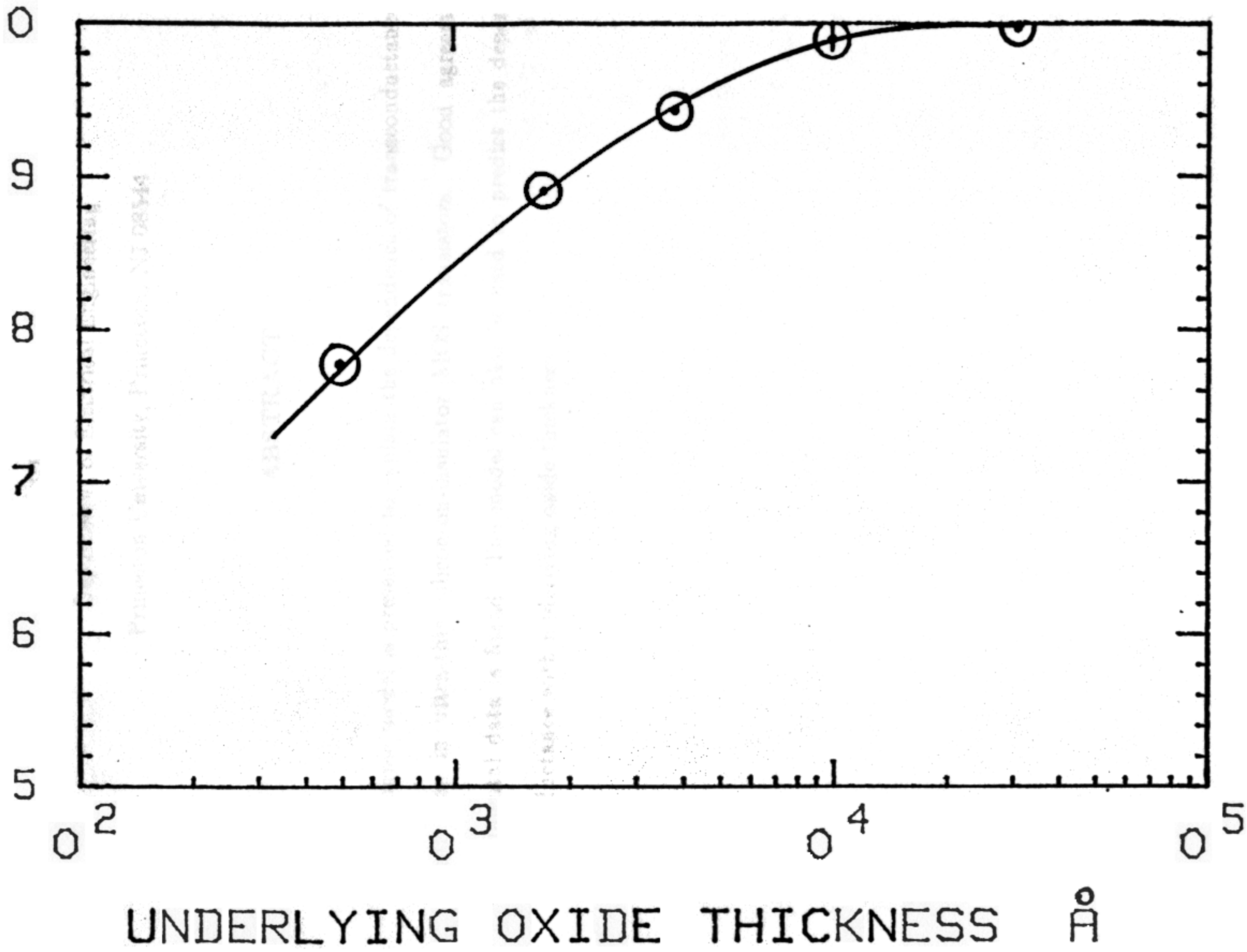


FIGURE 3



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