NANO LETTERS

2004
Vol. 4, No. 12
2489−2492

Self-Aligned, Insulating-Layer Structure for Integrated Fabrication of Organic Self-Assembled Multilayer Electronic Devices

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Received August 30, 2004; Revised Manuscript Received October 17, 2004

ABSTRACT

We demonstrate an approach for fabricating nanometer-scale devices with minimal device areas while still retaining compatibility with integrated metal wiring. A self-aligned layer of silicon oxide evaporated on top of a thin (25 nm) gold film deposited on a substrate with an etched step ensures that only a fraction of the gold, along the step edge, is exposed. Self-assembled multilayers of 11-mercaptoundecanoic acid (MUA) were grown on the exposed gold to define an arbitrarily long device length. A second, evaporated gold layer served as second electrode. Devices with between 3 and 7 MUA layers were insulating, with currents that decreased exponentially with the number of MUA layers.

The prospect of employing single organic molecules or organic self-assembled monolayers as the active elements in electronic devices has generated much recent interest. A variety of two-terminal monolayer devices and even integrated memory circuits (based on bistable devices) have been demonstrated.[1−5] One of the critical issues in the design of monolayer devices is the minimization of the overlap area between the metal electrodes that contact the monolayer. The minimization of device area is necessary to reduce the power consumption and to reduce the likelihood of metal penetration through the thin organic layer, which can lead to electrical defects and shorting. A further constraint in the development of monolayer devices for circuit application is that the fabrication procedure must allow integrated metal wiring. This requirement is particularly challenging because of the limited compatibility between most self-assembled monolayers and conventional metal-patterning techniques. Many common approaches for fabricating self-assembled monolayer and single molecule devices, such as scanning tunneling microscopy/conducting-probe atomic-force microscopy, mercury-drop junctions, and crossed-wire junctions, are not compatible with such integration.[2] A structure that minimizes device areas but still allows the use of (relatively) large patterned metal for connection to other devices or measurement probes is therefore desirable.

In this work, we demonstrate such an approach to fabricating molecular-scale devices that allows very small dimensions and integrated metal wiring. We also present the use of self-assembled multilayers of 11-mercaptoundecanoic acid (MUA) ($HS(CH_2)_{11}COOH$)) to define an arbitrarily long distance between electrodes and report the first current−voltage characteristics of these multilayers. The ability to define arbitrarily long distances between the electrodes is of interest not only for further study of transport in thin organic layers but also because it provides the potential for three-terminal measurements. In a three-terminal, field-effect transistor (FET) geometry, a large distance between source and drain contacts helps to allow penetration of the gate field into the organic layer for current modulation.

A self-aligned procedure was used to fabricate electrical test devices with minimal overlap areas while still allowing integrated metal wiring. This approach utilizes the thickness of a deposited metal (which can be controlled to a resolution of ∼1 nm) to define the width of the device area. The device dimension defined by the deposited metal is therefore much smaller than can be achieved by standard lithography techniques. Our work differs from other work that utilizes the thickness of a deposited layer as a critical dimension in that we do not cleave the sample or polish a cross section.[6−9]

In our work, silicon wafers were patterned by standard photolithography followed by plasma etching to define mesas

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10.1021/nl048593p CCC: $27.50 © 2004 American Chemical Society
Published on Web 11/02/2004

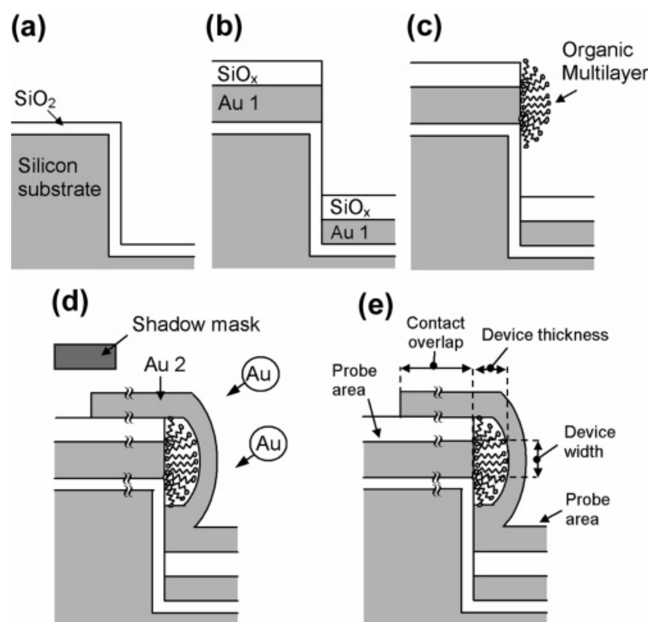

Figure 1. Schematic of device fabrication. (a) A silicon wafer is patterned by photolithography, plasma-etched to define 2−3 μm tall mesas, and thermally oxidized (30 nm). (b). A thin gold layer (25 nm) and SiO_x layer (30 nm) are deposited sequentially by e-beam evaporation, with 5-nm Ti layers used for adhesion purposes (not shown). (c). Organic multilayer is grown on exposed gold edge. (d) Second gold layer (50 nm) is deposited at angle to define top contact. (e) Probe areas are much larger than effective device width, which is defined by the thickness of the first gold layer.

that were 2−3 μm high (Figure 1a). A ~30-nm thermal oxide was then grown on the silicon wafer, including the step edges. Next, an electron-beam evaporator was used to deposit a layer of Au (25 nm) followed by an insulating layer of silicon oxide (SiO_x) (30−50 nm) (Figure 1b). Thin adhesion layers of Ti (~5 nm) were evaporated prior to both Au and SiO_x deposition. The evaporation direction was normal to the surface. The evaporation geometry was kept constant for every layer by rotating the source materials between evaporations while maintaining the same focal point for the electron beam so that each film was evaporated from the same location. The sequential deposition of the Au layer followed by the insulating SiO_x in identical evaporation geometries ensures that, although the top of the Au is covered by SiO_x, a small fraction of the Au layer along the side of the mesa remains exposed. Multilayers of MUA were then grown on this exposed Au (as described later in further detail) (Figure 1c). Finally, a second Au layer (50 nm) was deposited onto the sample at an angle (~60° from the normal) to form a top contact to the organic (Figure 1d). The azimuthal angle was chosen to be incident toward the site of the etched step. This layer was patterned by shadow mask to limit the area of the second gold layer on top of the mesa, so that the first gold layer could be electrically contacted later with a probe (Figure 1e). During the second Au evaporation, the sample stage was cooled to temperatures of 100 K, and the Au evaporation rate was kept below 0.05 nm/s to minimize damage to the MUA.[10] For comparison, some devices were fabricated without any SiO_x deposition so that the Au electrodes were separated by only the MUA layer over the entire electrode overlap area. (In these devices, the first Au/Ti layer was defined by a shadow mask instead of silicon etching.)

The critical feature of this process is the use of an insulating layer to limit the device area to the gold edge. As indicated in Figure 1e, this self-aligned layer allows the use of large electrode contact pads (typically 25 × 50 μm) and large electrode overlap areas (25 × 50 μm) while still retaining minimal device areas. The accuracy of the shadow-mask alignment to the mesa edge was not critical, typically being 5−50 μm. In the area where the two metals overlap, the deposited oxide insulator prevents any conduction between electrodes and the device area is limited to the sidewall of the mesa. This device area is defined as the product of the thickness of the gold layer and the width of the second shadow-masked Au layers to obtain 25 nm × ~25 μm ≅ 6 × 10^{-9} cm^2. (Note that in the active device the distance between the metal electrodes is defined by the thickness of the self-assembled organic layer and is typically 3 to 10 nm.) For comparison, when the devices were fabricated without the insulating layer, the device area includes the much larger top overlap area, typically ~25 × 50 μm, corresponding to an increase in area of ~10^6. We also note that these minimal device areas are attainable without the need for careful alignment and could be readily decreased by over an order of magnitude or more by using photolithography to define the width of the device instead of a shadow mask.

The organic layer examined in this study consisted of self-assembled multilayers of 11-mercaptoundecanoic acid (MUA). Using MUA, ordered layers of arbitrary thickness were possible, whereas conventional rigid monolayers do not assemble well for molecules with lengths > 5 nm.[11] MUA has been shown to form well-ordered multilayers via a simple deposition process.[12] Briefly, a gold-coated substrate is immersed in a 1 mM solution of MUA in ethanol for 2−12 h to form a monolayer of MUA. The exposed COOH functional groups of the MUA monolayer are then bonded to Cu ions by immersing the sample in a solution containing $Cu(ClO_4)_2$ for 5 min. A second layer of MUA (with the same orientation as the first) is grown by returning the sample to the MUA solution. Multiple layers can be grown by alternating MUA and Cu depositions. A conceptual diagram of the structure of an assembled mercaptoalkanoic acid multilayer is shown in Figure 2a. Previous work suggests that the oxidation state of the Cu is +2; however, the exact stoichiometry of the binding between the copper ions and molecules is less clear and may not correspond to the simple 1:1 ratio depicted in Figure 2a.[13] A linear increase in thickness of 1.6 nm/layer for MUA was measured in our work by ellipsometry (with $n = 1.45$) on samples grown on a thin layer of Au (80 nm, with 5 nm Ti adhesion layer) thermally evaporated onto silicon substrates (Figure 2b).

The device fabrication approach was evaluated by recording the electrical characteristics of devices with differing numbers of MUA layers at room temperature. Devices were either insulating, with low current densities (up to a factor of 10^7 smaller than control samples prepared without an

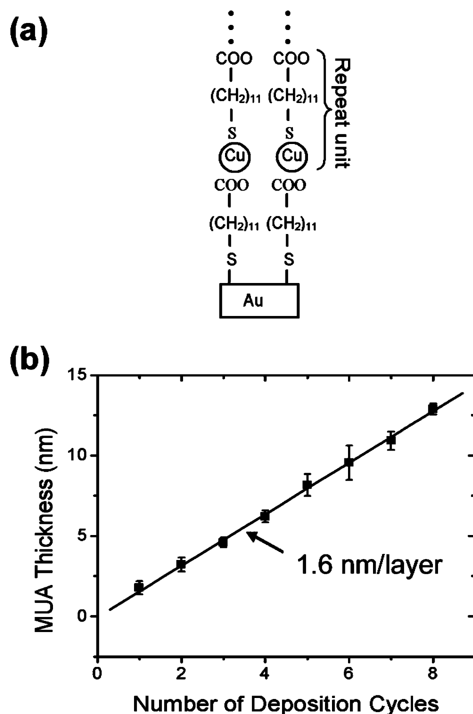

Figure 2. (a) Conceptual structure of MUA multiplayer on Au substrate. The actual stoichiometry of the binding between the copper and molecules may not correspond to the depicted 1:1 ratio. (b) MUA film thickness (determined by ellipsometry) vs number of deposition cycles.

organic layer between the gold electrodes) (Figure 3a) and nonlinear current−voltage characteristics (Figure 3b), or shorted, with high current densities and ohmic current−voltage traces. The resistances of the shorted devices were comparable to those of devices fabricated without an organic layer, indicating the presence of conducting pathways between the gold electrodes. As the number of MUA layers was increased from 3 to 7 layers, the yield of insulating devices increased to as high as ∼90% for 7 layers of MUA (devices made with 1−2 MUA layers were typically shorted) (Figure 4). Yields of unshorted devices were also much higher than in comparison devices fabricated without deposition of the SiO_x layer. For example, in devices with 7 MUA layers, only 16% of devices without the SiO_x layer (with top overlap area averaging from 10 to 600 μm^2) are not shorted, whereas with the self-aligned SiO_x layer ∼90% of the devices are not shorted.

Current densities in insulating devices at a given voltage were similar for devices with the insulating SiO_x layer and without the insulating layer (Figure 5). Device currents decreased exponentially with the number of MUA layers. The best fit to the geometric average of current density (measured at 0.5 V) yields a slope of one decade per 1.8 layers. Previous work on similar alkanethiol monolayers indicates that the transport mechanism for such layers at low bias is coherent tunneling, implying that the current (generally measured near a bias of 0 V) decreases exponentially with the length of the monolayer (or multilayer).[14−20] Reported values of the decay constant β, which varies only slightly with voltage, range from 5/nm to ∼10/nm.[20] Our

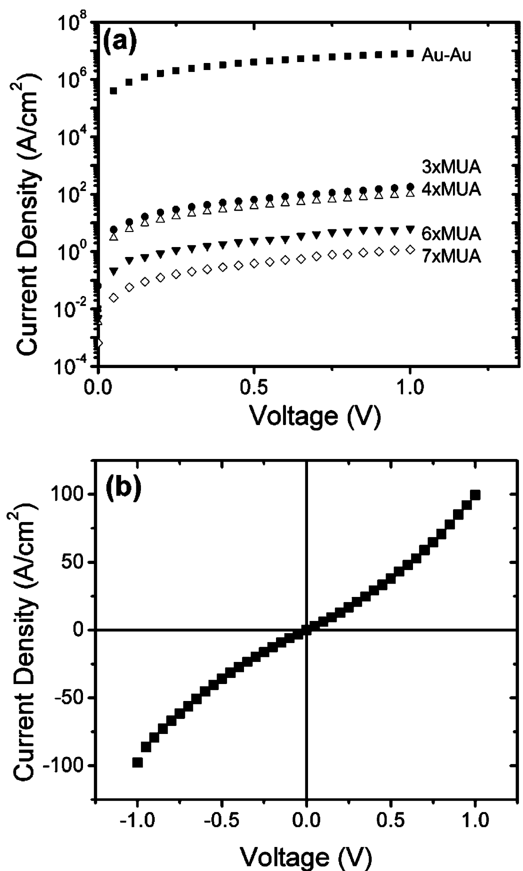

Figure 3. (a) Average current densities vs voltage (top contact with respect to lower contact) of devices with three to seven MUA layers. Also shown for reference is the current density of devices without any MUA layers (Au−Au contact). Each curve represents the geometric average of 6 to 22 devices. (b) Average current density vs voltage for devices with four MUA layers.

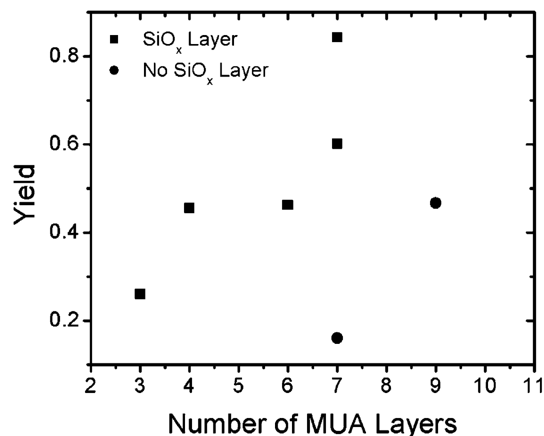

Figure 4. Yield (defined as fraction of unshorted devices) for samples made with SiO_x layer over first gold layer (squares) and without SiO_x layer (circles). Each point corresponds to at least 15 measured devices. Typical overlap areas in devices without SiO_x were 10−600 μm^2.

slope corresponds to a much lower $\beta = 0.7$/nm at 0.5 V, which indicates that transport in these multilayers (with interspersed copper layers) differs substantially from transport in pure alkanethiol monolayers. Furthermore, although device currents remained stable over multiple sweeps in each device,

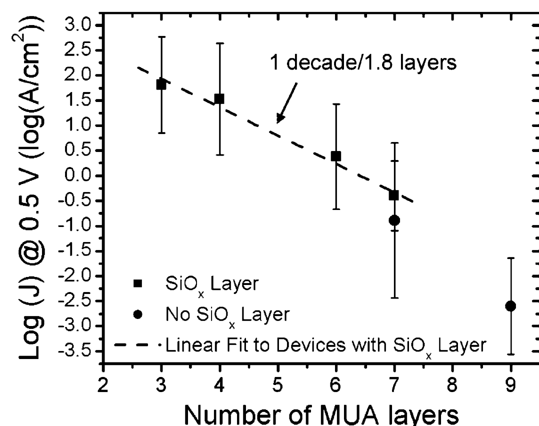

Figure 5. Log_{10} of current density (measured at a voltage of 0.5 V applied to top electrode) vs number of MUA layers. Each point was calculated by averaging the logarithms of 6 to 22 device currents; error bars represent the standard deviation of these logarithms. Data from devices with an SiO_x layer (squares) and without an SiO_x layer (circles) are shown, as well as a linear fit to the data of devices with an SiO_x layer.

the current density varied significantly (by up to a factor of 100) between similar devices. The source of this variation is not clear. A more detailed study of the active layer was inhibited by the geometry of the structure, which prevented us from studying the MUA multilayer formation on the sidewall of the mesa with conventional means such as scanning probe microscopy. However, the similarity between current densities for devices with and without the SiO_x layer suggests that the structure of the layers grown on the gold sidewalls was similar to that on conventional flat surfaces. Furthermore, the possibility that a thin oxide incidentally forms over portions of the gold sidewall in the insulating-layer devices so that the observed electrical characteristics are dominated by leakage through the thin oxide film is unlikely. In this case, the current density would not decrease with the number of MUA layers and would also not be similar to that measured in control devices, in contrast to what is observed in our experiments.

In conclusion, we have demonstrated a promising approach for fabricating molecular-scale electronic devices. This approach employs a self-aligned insulating layer to minimize device area combined with multiple self-assembled organic layers to further minimize electrical defects and obtain arbitrary device lengths. The device structure was used to measure the electrical characteristics of self-assembled multilayers of MUA. These layers were electrically insulating, and yields of unshorted devices as high as 90% were obtained. This approach may provide a robust platform for measuring and integrating small-area molecular-scale organic devices into circuits.

Acknowledgment. This work was supported by ONR contract N00014-02-1-075 and the NDSEG program. The authors thank Jie Zheng for helpful discussions and Nan Yao for help in characterizing the structure.

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NL048593P