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Reliability of Active-Matrix Organic Light-Emitting-Diode Arrays With Amorphous Silicon Thin-Film Transistor Backplanes on Clear Plastic

Bahman Hekmatshoar, *Student Member, IEEE*, Alex Z. Kattamis, Kunigunde H. Cherenack, Ke Long, Jian-Zhang Chen, Sigurd Wagner, *Fellow, IEEE*, James C. Sturm, *Fellow, IEEE*, Kamala Rajan, and Michael Hack

***Abstract*—We have fabricated active-matrix organic light emitting diode (AMOLED) test arrays on an optically clear high-temperature flexible plastic substrate at process temperatures as high as 285 °C using amorphous silicon thin-film transistors (a-Si TFTs). The substrate transparency allows for the operation of AMOLED pixels as bottom-emission devices, and the improved stability of the a-Si TFTs processed at higher temperatures significantly improves the reliability of light emission over time.**

***Index Terms*—Active matrix, active-matrix organic light-emitting-diode (AMOLED) display, amorphous silicon, clear plastic, stability, thin-film transistor.**

I. Introduction

ACTIVE-MATRIX organic light-emitting-diode (AMOLED) displays have all the necessary features to become the dominant technology for the next generation of flat-panel and flexible displays. Compared to liquid crystals displays (LCDs), OLEDs offer superior properties such as high-speed response, wide viewing angle, simple structure and low fabrication cost. In addition, OLEDs are emissive devices and do not need backlight illumination and color filters, resulting in low power consumption [1], [2]. Integrating OLEDs with TFTs in the form of active matrices is required for achieving very low power consumptions in mid-sized and large-sized displays [3], [4]. Since the introduction of AMOLED displays, low-temperature poly-Si has been the material of choice for making the TFT backplanes due to the relatively high mobility and stability of poly-Si TFTs [4], [5]. However, with the improvement of OLED efficiency and especially the introduction of phosphorescent OLEDs with efficiencies superior to conventional fluorescent OLEDs, which allow the use of a-Si TFTs instead of poly-Si devices [3], a-Si TFTs have become very appealing for AMOLED applications [6], [7]. The reason is that a-Si technology is a mature low-cost technology widespread in production and is very suitable for large-area deposition especially on flexible plastic substrates [8]. Flexibility is a requirement for economical mass production by roll-to-roll processing.

A critical technical issue associated with employing a-Si TFT backplanes on clear plastic substrates for AMOLED displays is the stability of a-Si TFTs. The threshold voltage of a-Si TFTs increases with time due to charge trapping in the gate nitride and defect creation in the a-Si [9]. This problem becomes serious when the TFTs are made at the low process temperatures compatible with existing clear plastic substrates ($\ll 300$ °C) [10]–[12]. Unlike AMLCDs, AMOLED pixels operate in dc and the OLED current depends directly and continuously on the TFT threshold voltage. Therefore, as the threshold voltage increases, the OLED current supplied by the TFT and thus the pixel brightness drops. The threshold voltage shift is reduced as a result of improvement in the quality of the gate nitride and a-Si material at higher process temperatures [10]–[13].

In this letter, we report the successful fabrication of AMOLED test arrays on a clear plastic substrate at temperatures as high as 285 °C, which is a significant improvement compared to the previously reported AMOLED devices on clear plastic substrates fabricated at 150 °C [14], [15]. Such a high temperature process has been made possible by a novel clear plastic substrate that exhibits all of the four critical properties of: 1) high glass transition temperature (> 300 °C); 2) low coefficient of thermal expansion (CTE) (< 10 ppm/°C); 3) optical transparency; and 4) process compatibility (vacuum and chemicals), as well as proper stress engineering of the layers as established earlier by our group [16], [17].

II. Fabrication Process

The circuit schematic of the fabricated two-TFT AMOLED pixels is shown in Fig. 1. The pixel is composed of a switching TFT, a driving TFT, a storage capacitor, and an OLED, as well as a data line, a select line, a power line and a common ground line (OLED cathode). The cross section of the AMOLED pixel structure is shown in Fig. 2. The fabrication process starts by coating both sides of the clear plastic substrate

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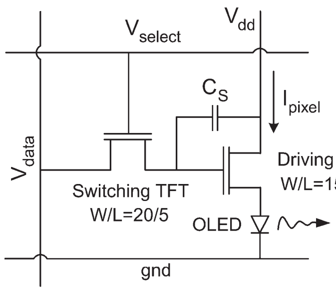
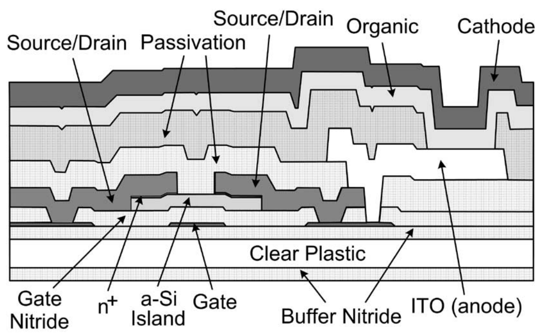


Fig. 1. Circuit schematic of a two-TFT AMOLED pixel.



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with 200-nm-thick silicon nitride (SiN_x) buffer layers grown by plasma-enhanced chemical vapor deposition (PECVD) for protection against chemicals during the fabrication process. The bottom metal (Cr/Al based) is then evaporated thermally and patterned by wet-etching. Next, a 300/200/30-nm TFT stack of SiN_x/a-Si(undoped)/n^+ a-Si (gate dielectric/channel/drain and source contacts) is deposited in a multichamber PECVD machine without exposure to air. For comparison, we fabricated AMOLED arrays at three different gate nitride deposition temperatures of 285 °C, 250 °C, and 200 °C. The gate nitride deposition temperature is the highest temperature used in processing and hereafter we will refer to it as the process temperature. The a-Si deposition has been optimized for best quality at 250 °C for the 250 °C and 285 °C processes, and at 200 °C for the 200 °C process [10]–[12]. Dry etching is used next to pattern the a-Si islands and open contact vias to the bottom metal. The top metal (Cr/Al based) is then thermally evaporated and patterned by wet etching. The n^+ a-Si is then cut at the backside of the a-Si channel by dry etching, and the samples are annealed at 180 °C for 1 h to repair the dry etching damage to the channel. The backplane is then passivated by a 250-nm-thick layer of SiN_x grown by PECVD at 125 °C, and dry-etching is used to open contact holes for ITO (OLED anode). Next, a 200-nm-thick ITO layer is deposited at room temperature by dc-sputtering from an In_2O_3/SnO_2 target (with 90/10 weight ratio) in Ar/O_2 ambient and patterned by wet etching. A passivation layer is then deposited and patterned to cover the edges of ITO to avoid shorts between the ITO and the cathode in the OLED (evaporated subsequently). Dry etching is used next to open vias to the external pads in the passivation (not shown in the cross section). Finally, the AMOLED structure is completed by evaporation of a green phosphorescent OLED (PHOLED) through a pair of shadow masks for organic layers and cathode.

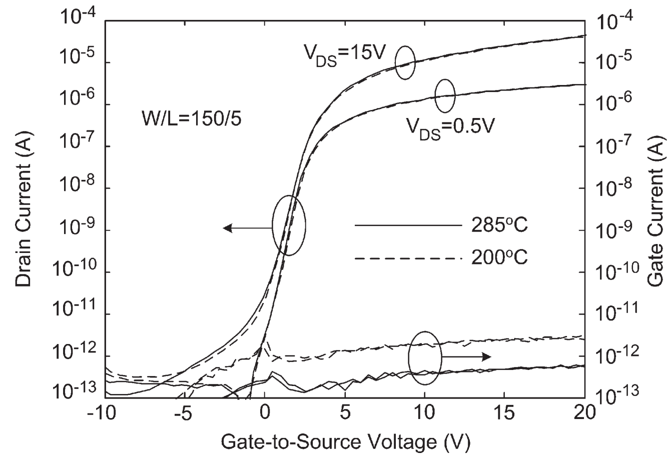

Fig. 3. DC output characteristics of the driver TFTs fabricated on clear plastic at 200 °C and 285 °C process temperatures.

Controlling the mechanical stress in the deposited layers is crucial to obtain a flat surface with crack-free layers, especially at high process temperatures (250 °C and 285 °C) where the dimensional change in the substrate becomes significant (even with the low CTE of the clear plastic substrates). The mechanical stress in the PECVD-grown layers can be adjusted by the plasma power density [16], [17]. The buffer nitride layers on both sides of the clear plastic are grown at a plasma power density of 200 mW/cm^2 resulting in compressive films balancing out the stress levels in each other and laying out the passivated substrate flat. Both bottom and top metal layers are tri-layers of Cr–Al–Cr with thin and thus low-tensile-stress Cr layers (15 nm) for adhesion and low-stress Al layers for sufficient conduction. The gate SiN_x and a-Si are deposited at plasma power densities of 22 and 17 mW/cm^2, respectively, resulting in compressive films. The n^+ a-Si layer grown at 17 mW/cm^2 is tensile, similar to the top and bottom Cr layers, and balances out the stress from the compressive layers. The SiN_x passivation layer on the device side and the sputtered ITO are nearly stress free. The overall result is a crack-free backplane with a flat surface, ready for OLED evaporation.

III. Results and Discussion

The dc output characteristics of typical driving TFTs $(W/L = 150/5\ \mu m)$ fabricated on clear plastic at 200 °C and 285 °C are shown in Fig. 3. It is observed that the ON-state driving current is not essentially affected by changing the process temperature. Both TFTs show an apparent (i.e., not corrected for contact resistance) effective mobility of $0.63\ cm^2/(V \cdot s)$ and an apparent threshold voltage of 2.1 V in the saturation regime. However, the lower gate leakage current for the 285 °C process shows improvement in the quality of gate nitride at higher process temperatures. The dc output characteristics of a fabricated AMOLED pixel are shown in Fig. 4. A luminance intensity of 1000 Cd/m^2 is obtained at a data voltage of 16.8 V and corresponds to an OLED efficiency of 57 Cd/A. The inset is an optical image of an 8 × 8 AMOLED test array made on clear plastic at 250 °C, showing a high process yield of about 96%.

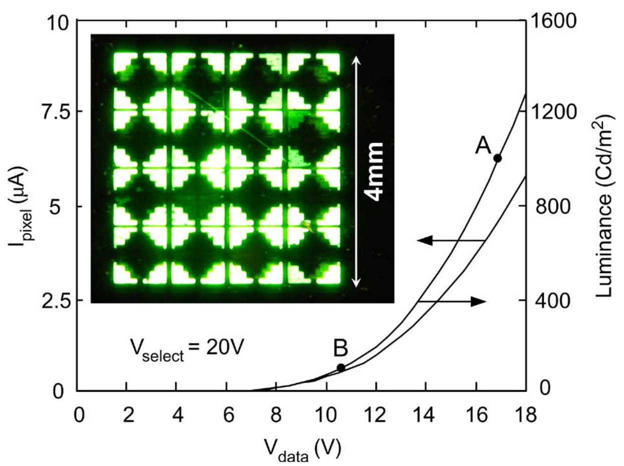

Fig. 4. DC output characteristics of an AMOLED pixel fabricated on clear plastic. The inset shows an image of an 8 × 8 AMOLED test array fabricated on clear plastic at 250 °C. The pattern of emission is defined by the ITO area.

The process temperature drastically affects the stability of AMOLED pixels. We stressed each pixel at two different pixel currents corresponding to pixel luminance intensities of 1000 and 100 Cd/m^2 (points A and B marked on the luminance curve in Fig. 4). For each stress point, the bias voltages on the select line (20 V) and data line (with values corresponding to the initial pixel luminance at points A and B) were kept constant and the pixel luminance was measured versus time. Fig. 5(a) shows the luminance drop under the mentioned stress conditions for pixels processed at three process temperatures, 200 °C, 250 °C, and 285 °C. The luminance intensities are normalized to their initial values (100 Cd/m^2 for stress point B and 1000 Cd/m^2 for stress point A). In all curves, the pixel luminance drops over time. It is observed that for each process temperature, the luminance degradation is faster at stress point A than at stress point B, and more importantly degradation proceeds significantly faster at lower TFT process temperatures. Since the temperature is the only process variable, faster luminance degradation at lower TFT process temperatures may be attributed to a faster threshold voltage increase in the driver TFT, which reduces the pixel current accordingly. Note that on this time scale, the effect of OLED luminance degradation is negligible due to the very long lifetime of the green phosphorescent OLED (PHOLED) [18]. The faster drop at stress point A compared to stress point B may be explained by the increased charge trapping in the gate nitride and defect creation in a-Si at higher gate voltages, resulting in a larger threshold voltage shift in the driving TFT. As shown in Fig. 5(a), the improvement in the pixel reliability at higher process temperatures is significant. After 4 h of continuous stress, the pixel brightness drops to about 40% of its initial value for the 200 °C process, while for the 285 °C process the brightness drops to only about 95%. This result demonstrates the impact of increasing the process temperature on improving the reliability of AMOLED pixels. Such high process temperatures are not conventionally possible because of the thermal constraints of clear plastic substrates, which limit the TFT process to low temperatures. Therefore, new clear plastic substrates with thermal properties that allow processing at such high temperatures are essential to flexible bottom-emitting AMOLED displays based on a-Si.

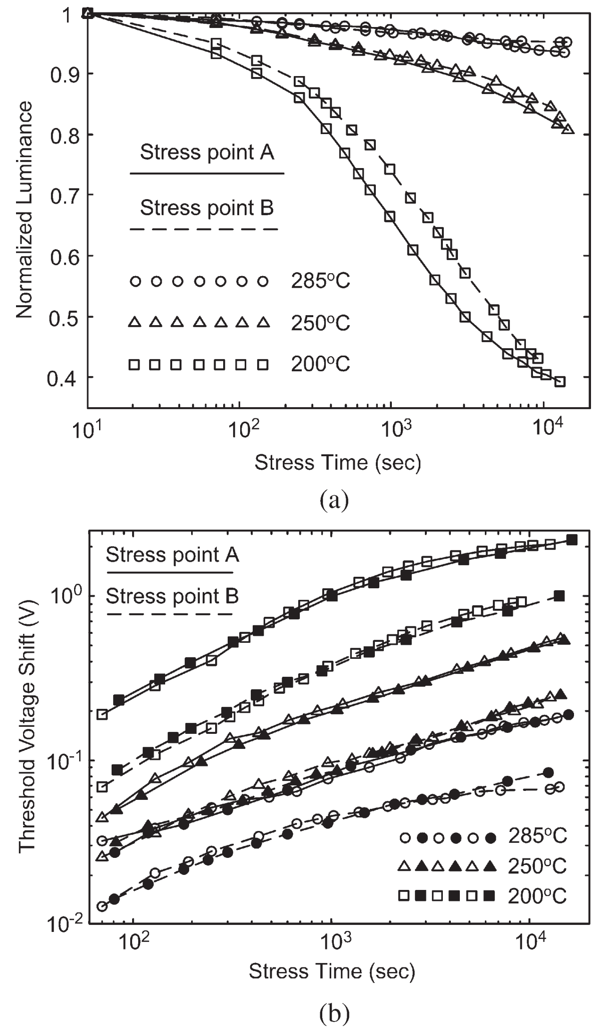

Fig. 5. (a) Luminance as a function of dc stress time for the AMOLED pixels fabricated at three process temperatures on clear plastic. The stress points A and B correspond to the points marked on the luminance curve in Fig. 4 and (b) threshold voltage shift of the driver TFT as a function of dc stress time extracted from the luminance data of part (a) assuming negligible OLED luminance degradation (empty symbols) and measured threshold voltage shift of individual test driver TFTs under the same dc bias stress (full symbols).

To confirm that the luminance degradation of the fabricated AMOLED pixels is mainly due to the a-Si TFT threshold voltage shift, we compare the threshold voltage shift of the driver TFTs calculated from the AMOLED luminance data in Fig. 5(a) assuming no OLED degradation, with the directly measured threshold voltage shift of individual test driver TFTs under the same dc bias stress, in Fig. 5(b). The small differences between these data verify that the pixel luminance degradation is mainly a result of the threshold voltage shift of the driver TFTs.

IV. SUMMARY AND CONCLUSION

We have successfully fabricated AMOLED test arrays on clear plastic substrates at temperatures as high as 285 °C, and demonstrated the impact of high a-Si TFT process temperatures on the reliability of AMOLED pixels. Our results suggest that high temperature processing is crucial for AMOLED displays with a-Si TFT backplanes.

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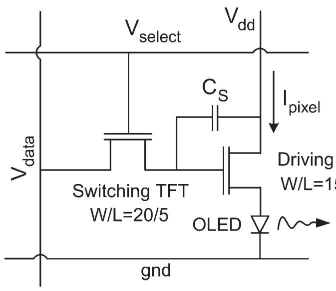

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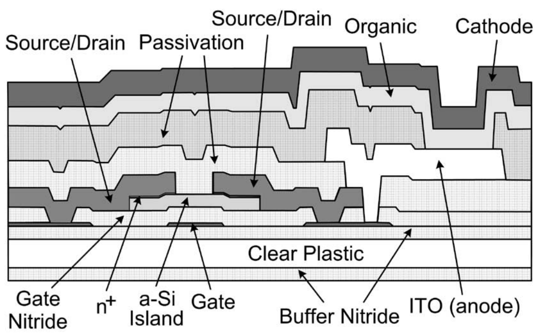

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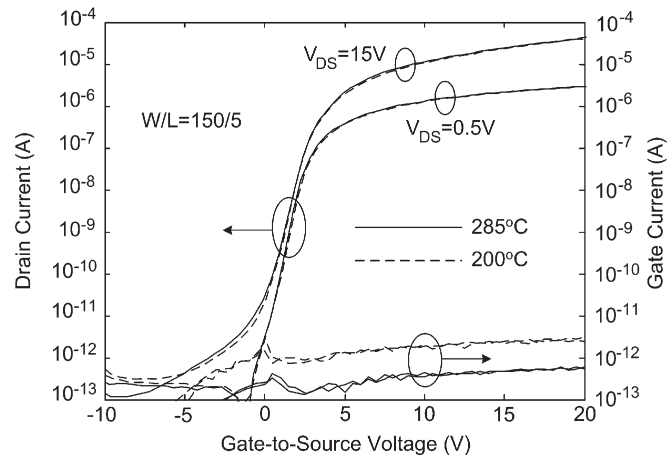

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Controlling the mechanical stress in the deposited layers is crucial to obtain a flat surface with crack-free layers, especially at high process temperatures (250 °C and 285 °C) where the dimensional change in the substrate becomes significant (even with the low CTE of the clear plastic substrates). The mechanical stress in the PECVD-grown layers can be adjusted by the plasma power density [16], [17]. The buffer nitride layers on both sides of the clear plastic are grown at a plasma power density of 200 mW/cm^2 resulting in compressive films balancing out the stress levels in each other and laying out the passivated substrate flat. Both bottom and top metal layers are tri-layers of Cr–Al–Cr with thin and thus low-tensile-stress Cr layers (15 nm) for adhesion and low-stress Al layers for sufficient conduction. The gate SiN_x and a-Si are deposited at plasma power densities of 22 and 17 mW/cm^2, respectively, resulting in compressive films. The n^+ a-Si layer grown at 17 mW/cm^2 is tensile, similar to the top and bottom Cr layers, and balances out the stress from the compressive layers. The SiN_x passivation layer on the device side and the sputtered ITO are nearly stress free. The overall result is a crack-free backplane with a flat surface, ready for OLED evaporation.

III. Results and Discussion

The dc output characteristics of typical driving TFTs $(W/L = 150/5\ \mu\text{m})$ fabricated on clear plastic at 200 °C and 285 °C are shown in Fig. 3. It is observed that the ON-state driving current is not essentially affected by changing the process temperature. Both TFTs show an apparent (i.e., not corrected for contact resistance) effective mobility of $0.63\ \text{cm}^2/(\text{V}\cdot\text{s})$ and an apparent threshold voltage of 2.1 V in the saturation regime. However, the lower gate leakage current for the 285 °C process shows improvement in the quality of gate nitride at higher process temperatures. The dc output characteristics of a fabricated AMOLED pixel are shown in Fig. 4. A luminance intensity of 1000 Cd/m^2 is obtained at a data voltage of 16.8 V and corresponds to an OLED efficiency of 57 Cd/A. The inset is an optical image of an 8 × 8 AMOLED test array made on clear plastic at 250 °C, showing a high process yield of about 96%.

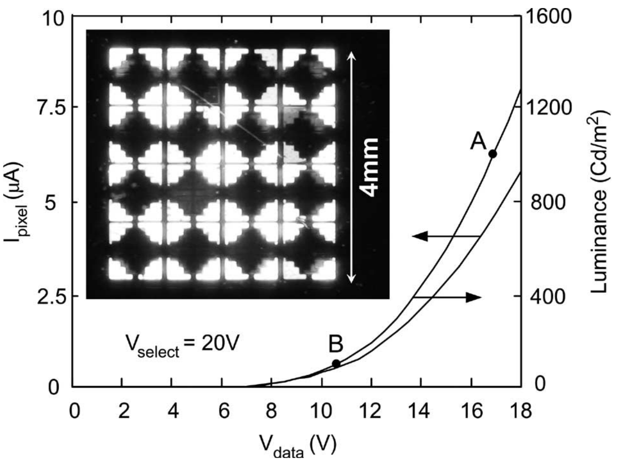

Fig. 4. DC output characteristics of an AMOLED pixel fabricated on clear plastic. The inset shows an image of an 8 × 8 AMOLED test array fabricated on clear plastic at 250 °C. The pattern of emission is defined by the ITO area.

The process temperature drastically affects the stability of AMOLED pixels. We stressed each pixel at two different pixel currents corresponding to pixel luminance intensities of 1000 and 100 Cd/m^2 (points A and B marked on the luminance curve in Fig. 4). For each stress point, the bias voltages on the select line (20 V) and data line (with values corresponding to the initial pixel luminance at points A and B) were kept constant and the pixel luminance was measured versus time. Fig. 5(a) shows the luminance drop under the mentioned stress conditions for pixels processed at three process temperatures, 200 °C, 250 °C, and 285 °C. The luminance intensities are normalized to their initial values (100 Cd/m^2 for stress point B and 1000 Cd/m^2 for stress point A). In all curves, the pixel luminance drops over time. It is observed that for each process temperature, the luminance degradation is faster at stress point A than at stress point B, and more importantly degradation proceeds significantly faster at lower TFT process temperatures. Since the temperature is the only process variable, faster luminance degradation at lower TFT process temperatures may be attributed to a faster threshold voltage increase in the driver TFT, which reduces the pixel current accordingly. Note that on this time scale, the effect of OLED luminance degradation is negligible due to the very long lifetime of the green phosphorescent OLED (PHOLED) [18]. The faster drop at stress point A compared to stress point B may be explained by the increased charge trapping in the gate nitride and defect creation in a-Si at higher gate voltages, resulting in a larger threshold voltage shift in the driving TFT. As shown in Fig. 5(a), the improvement in the pixel reliability at higher process temperatures is significant. After 4 h of continuous stress, the pixel brightness drops to about 40% of its initial value for the 200 °C process, while for the 285 °C process the brightness drops to only about 95%. This result demonstrates the impact of increasing the process temperature on improving the reliability of AMOLED pixels. Such high process temperatures are not conventionally possible because of the thermal constraints of clear plastic substrates, which limit the TFT process to low temperatures. Therefore, new clear plastic substrates with thermal properties that allow processing at such high temperatures are essential to flexible bottom-emitting AMOLED displays based on a-Si.

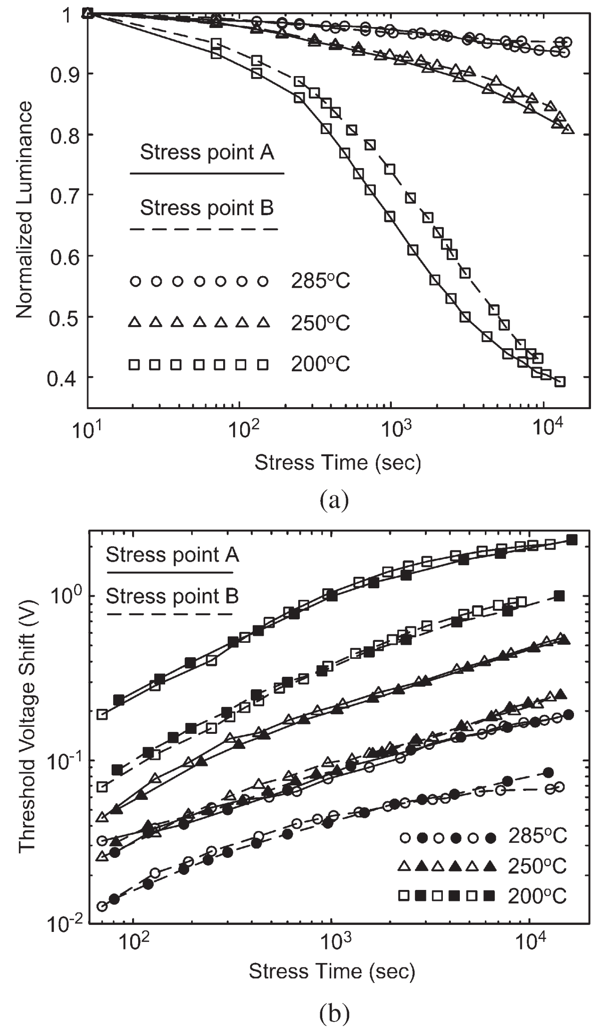

Fig. 5. (a) Luminance as a function of dc stress time for the AMOLED pixels fabricated at three process temperatures on clear plastic. The stress points A and B correspond to the points marked on the luminance curve in Fig. 4 and (b) threshold voltage shift of the driver TFT as a function of dc stress time extracted from the luminance data of part (a) assuming negligible OLED luminance degradation (empty symbols) and measured threshold voltage shift of individual test driver TFTs under the same dc bias stress (full symbols).

To confirm that the luminance degradation of the fabricated AMOLED pixels is mainly due to the a-Si TFT threshold voltage shift, we compare the threshold voltage shift of the driver TFTs calculated from the AMOLED luminance data in Fig. 5(a) assuming no OLED degradation, with the directly measured threshold voltage shift of individual test driver TFTs under the same dc bias stress, in Fig. 5(b). The small differences between these data verify that the pixel luminance degradation is mainly a result of the threshold voltage shift of the driver TFTs.

IV. Summary and Conclusion

We have successfully fabricated AMOLED test arrays on clear plastic substrates at temperatures as high as 285 °C, and demonstrated the impact of high a-Si TFT process temperatures on the reliability of AMOLED pixels. Our results suggest that high temperature processing is crucial for AMOLED displays with a-Si TFT backplanes.

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