Nonvolatile Amorphous-Silicon Thin-Film-Transistor Memory Structure for Drain-Voltage Independent Saturation Current

Yifei Huang, Sigurd Wagner, and James C. Sturm

***Abstract*—Transistors with floating gate, used for nonvolatile memory, have a saturation current that increases with drain voltage. This is the result of undesirable capacitive coupling between the floating gate and the drain electrode, which can occur in devices made on crystalline silicon or amorphous silicon (a-Si) technologies. In this paper, we report on a new a-Si thin-film transistor memory structure that uses a high-defect-density interface in the gate insulator, instead of a floating gate, to trap charges. By reducing the ability of the trapped charge to laterally move in the device, this structure eliminates the drain-voltage dependence of the saturation current and the threshold voltage. The room-temperature data retention time is greater than ten years.**

***Index Terms*—Amorphous silicon (a-Si), nonvolatile memory, thin-film transistor (TFT).**

I. Introduction

NONVOLATILE memory devices based on amorphous Silicon (a-Si) thin-film transistors (TFTs) have the potential to greatly expand the functionality of the a-Si TFT circuitry. If designed to be compatible with the existing TFT fabrication process, they could provide a low-cost and efficient way to integrate memory capabilities into large-area electronics. One potential application is active-matrix organic light emitting diode (OLED) displays, where integrated nonvolatile memory can be used to reduce excess refresh cycles [1]. As a result, there has been a rising interest in the development of a-Si floating gate TFT memory [2], [3]. However, these initial demonstrations suffer from two major drawbacks, i.e., 1) short retention time [2] and 2) strong dependence of drain saturation current $I_{D,\mathrm{SAT}}$ on drain voltage [3]. In this paper, we will focus on the latter issue and demonstrate a new device structure that eliminates the effect.

II. Background

In the a-Si floating gate TFT memory, electrons tunnel into the floating gate from the channel and out from the floating gate into the channel under the applied gate field. No drain field or hot electron effects are involved. The charges stored in the floating gate alter the threshold voltage of the transistor, which serves as the indicator of the memory state [3]. Because a-Si technology, as used for large-scale active matrix liquid crystal display (AMLCD) production, is a bottom-gate structure, in the a-Si floating gate TFT memory, the lower gate is the control gate, and the a-Si layer, which is completely surrounded by SiN_x, is the floating gate [see Fig. 1(a)]. The equivalent capacitive circuit model of the device, where C_{fc}, C_{fs}, C_{fd}, and C_{fg} are the capacitance values between the floating gate and channel, source, drain, and control gate, respectively [see Fig. 1(b)]. Unlike a conventional a-Si TFT [4] or any other MOS transistor, the voltage on the control gate does not directly modulate channel carrier density. Instead, the voltage on the floating gate controls the channel behavior. Furthermore, the voltage on the floating gate V_{FG} node is a combined function of the voltages on the control gate, drain, and source electrodes. Assuming a grounded source electrode [5], i.e.,

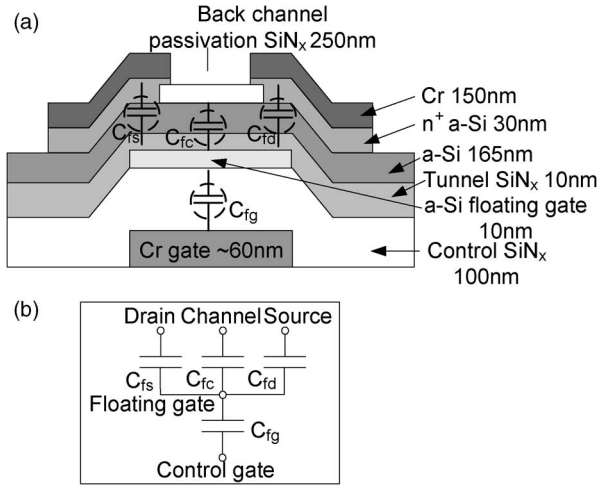

Fig. 1. (a) Structure of the a-Si floating gate TFT memory. (b) Capacitive network model of the a-Si floating gate TFT.

$$V_{\mathrm{FG}} = \frac{C_{\mathrm{fg}}}{C_T}(V_G + fV_D) \tag{1}$$

where

$$C_T = C_{\mathrm{fg}} + C_{\mathrm{fs}} + C_{\mathrm{fc}} + C_{\mathrm{fd}} \tag{2}$$

$$f = \frac{C_{\mathrm{fd}}}{C_{\mathrm{fg}}}. \tag{3}$$

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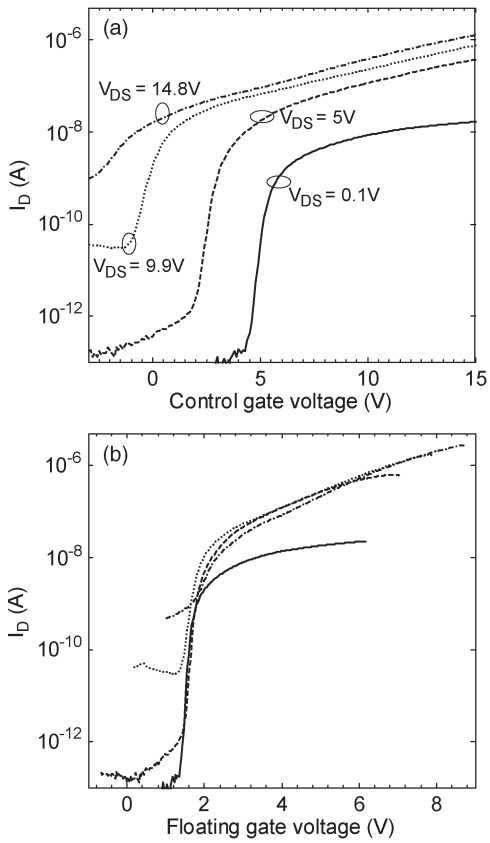

Fig. 2. (a) $I_{\rm DS}$ versus $V_{\rm GS}$ (control gate voltage) characteristics of an a-Si floating gate TFT at four different drain bias conditions. Note the different apparent threshold voltages under each drain bias condition. (b) Same $I_{\rm DS}$ data as (a) plotted versus $V_{\rm FG}$ (floating gate voltage). Floating gate voltages are calculated via equation (1). With respect to the floating gate, V_T values of the different curves are the same.

Substituting (1) into the equation for the conventional MOS transistor saturation current yields [4]

$$I_{\rm DS} = \frac{\mu C_{\rm CG}}{2}\frac{W}{L}\frac{C_{\rm fg}}{C_T}(V_{\rm GS} + fV_{\rm DS} - V_T)^2 \qquad (4)$$

where $C_{\rm CG}$ is the capacitance of the entire gate stack, and V_T is the threshold voltage with respect to the control gate, not the floating gate.

In (4), one can clearly observe that the device saturation current will not be independent of the drain–source bias, as is the case in conventional MOS transistors. This is because the drain voltage capacitively controls the floating gate voltage. In fact, depending on the ratio f, which is defined in (3), the $I_{\rm DS}$ versus $V_{\rm DS}$ curves can have a large positive slope in the saturation regime. Furthermore, the $I_{\rm DS}$ versus $V_{\rm GS}$ (control gate voltage) curves will show different apparent threshold voltages depending on the applied drain bias. This is illustrated in Fig. 2(a), where $I_{\rm DS}$ is shown as a function of the control gate voltage at various different drain biases. Fig. 2(b) shows the same set of current data with the x-axis transformed to a floating gate voltage using (1), where $C_{\rm fc}$, $C_{\rm fs}$, $C_{\rm fd}$, and $C_{\rm fg}$ have been calculated based on device geometry (i.e., the overlap areas and dielectric thicknesses). Since the floating gate voltage directly modulates the channel carrier density, the threshold voltage with respect to the floating gate is the intrinsic channel

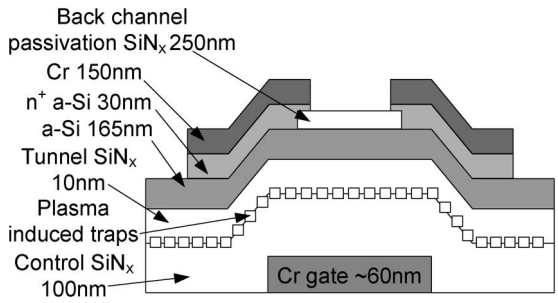

Fig. 3. Structure of the a-Si ST-TFT memory.

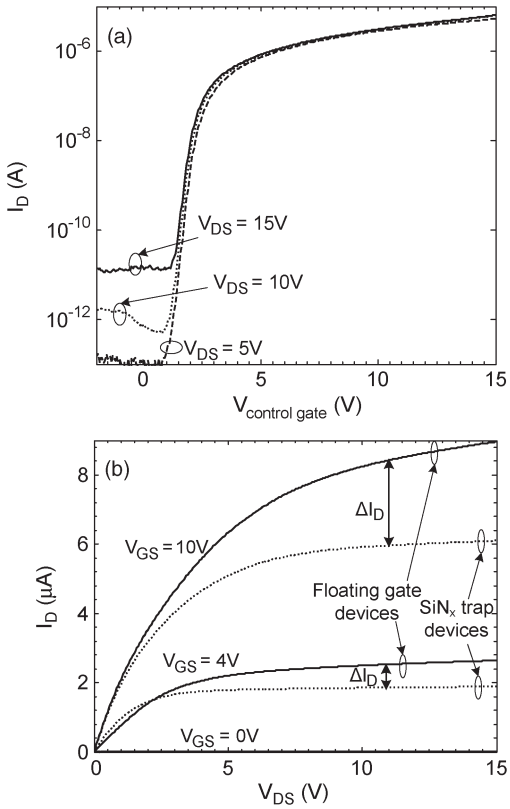

Fig. 4. (a) $I_{\rm DS}$ versus $V_{\rm GS}$ characteristics of an a-Si ST-TFT at three different drain bias conditions. (b) $I_{\rm DS}$ versus $V_{\rm DS}$ characteristics of an a-Si ST-TFT and $I_{\rm DS}$ versus $V_{\rm DS}$ characteristics of an a-Si floating gate TFT at three different gate bias conditions. Note the difference in saturation drain current.

threshold. As a result, there are no differences in the V_T in the various curves of Fig. 2(b). In applications such as the OLED driver in an active-matrix OLED pixel, the TFT converts a control voltage (gate voltage) into a pixel current (drain–source current) to control the OLED brightness [6]. Having the current depend on the drain voltage is an undesirable characteristic, and it is a motivation for this paper.

III. New Device Structure

The dependence of the saturation current of the floating gate TFT on the drain voltage can be eliminated if the overlap capacitance between the drain and the floating gate is eliminated. This can be done with careful lithographic alignment, which is not amenable to low-cost manufacturing over large areas. In this paper, we replace the floating gate with a charge-trapping

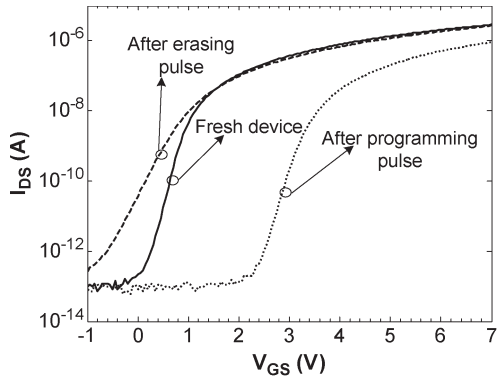

Fig. 5. $I_{\rm DS}$ versus $V_{\rm GS}$ characteristics of the ST-TFT at various stages of the program/erase cycle. Program: apply 35 V to the gate for 10 ms with the source/drain (S/D) grounded. Erase: apply -28.5 V to the gate for 10 ms with the S/D grounded.

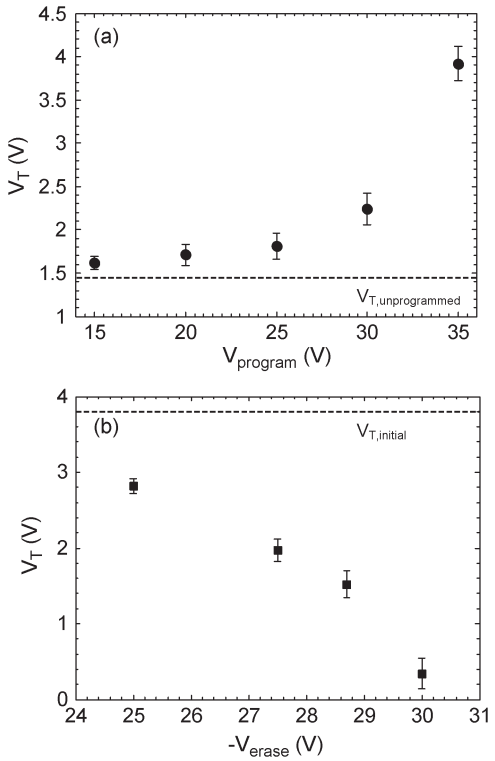

Fig. 6. (a) Programming characteristics of the ST-TFT. The devices are programmed with the S/D grounded, and $V_{\rm program}$ is applied to the gate for 10 ms. (Dotted line) $V_{T,\rm unprogrammed}$ refers the threshold voltage of the device prior to programming. (b) Erasing characteristics of the ST-TFT. The devices are first programmed with the S/D grounded, and 35 V is applied to the gate for 10 ms and then erased by applying $V_{\rm erase}$ to the gate for 10 ms with the S/D grounded. (Dotted line) $V_{T,\rm initial}$ refers the threshold voltage of the devices after programming and prior to erasing.

medium that is not conductive (see Fig. 3). In the new approach, a high-defect-density interface is used as the charge storage medium. Because the discrete traps are spatially separated, charges cannot move around in the charge-trapping medium. As such, any capacitive coupling from the drain to the traps will not produce a change in the potential distribution in the gate stack and will therefore not affect the channel carrier density. The fabrication process is nearly identical to that of the standard a-Si TFT [7], except that the gate nitride deposition is interrupted to deposit a thin layer ($\sim$10 nm) of a-Si. The a-Si is immediately

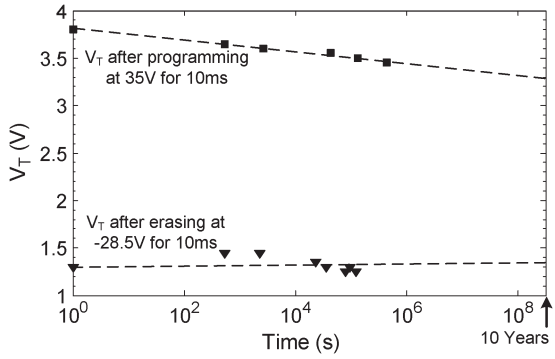

Fig. 7. Room-temperature retention characteristics of the ST-TFT. The devices are programmed/erased and stored at room temperature with all electrodes floating. The shown dotted lines are extrapolations of measured data points (solid squares and triangles).

etched away using reactive ion etch. The overetch damages the top-nitride surface, resulting in the traps. A thin layer of nitride is then deposited over the traps as the tunnel gate dielectric. The fabrication then proceeds in the same way as that of the conventional a-Si TFT process. Our proposed structure, which we will refer to as the $\rm SiN_{\it x}$ trap TFT (ST-TFT), is not unlike the VLSI SONOS type nonvolatile memory transistors [8]–[10], in which electrons tunnel through the tunnel gate oxide layer to be trapped in the defects at the $\rm SiO_2/Si_3N_4$ interface.

IV. Electrical Characterization of the $\rm SiN_{\it x}$ Trap Devices

The $I_{\rm DS}$ versus $V_{\rm GS}$ characteristics of an ST-TFT memory device at three different drain bias conditions are shown in Fig. 4(a). Unlike the floating gate memory device, V_T is not dependent on the applied drain bias. This is because any capacitive coupling from the drain to the traps does not affect the number of carriers in the channel. Fig. 4(b) shows the $I_{\rm DS}$ versus $V_{\rm DS}$ characteristics of an ST-TFT memory device that are shown along with that of a floating gate memory device with the same aspect ratio, dielectric thickness, and process conditions (The two device are on the same wafer, sharing all the process steps, except the floating gate device did not have the floating gate etched away). The $\rm SiN_{\it x}$ trap device has a clear saturation regime, where the drain current is nearly independent of the drain voltage. The floating gate device, on the hand, has a drain current that increases with increasing drain bias, which results from capacitive coupling between the drain and the floating gate.

Similar to the floating gate memory device, the nonvolatile effect in the $\rm SiN_{\it x}$ trap memory devices is based on electrons tunneling into the $\rm SiN_{\it x}$ traps from the channel for programming and out from the $\rm SiN_{\it x}$ traps into the channel for erasing, under the applied gate field. No drain field or hot electron effects are involved. This mechanism of charge transport in the gate dielectric is well understood in the context of threshold voltage instabilities of TFTs [11]. Fig. 5 shows the $I_{\rm DS}$ versus $V_{\rm GS}$ characteristics of an ST-TFT before programming, after programming, and after erase. Reversible V_T shifts can be clearly observed. The programming and erasing characteristics of the $\rm SiN_{\it x}$ trap device depend on the magnitude of the positive and

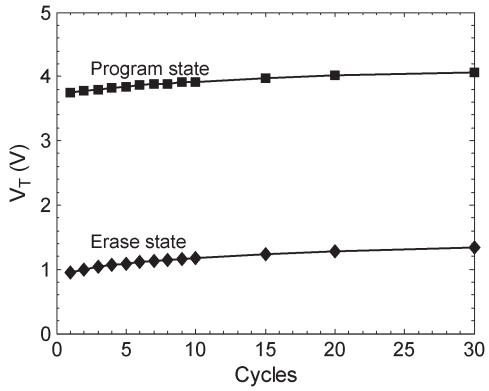

Fig. 8. Room-temperature endurance characteristics of the ST-TFT. The device is programmed with a 35-V 10-ms gate pulse and erased with a −28.5-V 10-ms gate pulse. The shown lines connect the measured data points (solid squares and diamonds).

negative voltage pulses, respectively (see Fig. 6). The room-temperature retention characteristic of the SiN_x trap device is shown in Fig. 7. The programmed state decays over time as the trapped electrons leak out of the traps. The erased state remains unchanged over time because there are no trapped charges to leak out. The memory window of the device is extrapolated to be $\sim$80% of its initial value after ten years of storage at room temperature. Extrapolation is based on the assumption that the charge loss is exponential with time, which is reasonable at room temperature [12]. The room-temperature endurance characteristic is shown in Fig. 8. The device can be reliably toggled between the program and erase states by applying positive and negative gate voltage pulses. The memory window appears to drift up toward higher threshold voltages. This may be due to residual trapped charges that are not completely removed by the erasing pulse.

V. Conclusion

We demonstrated a novel a-Si-based TFT memory device, which, unlike previous a-Si floating gate memory TFTs, does not have a floating gate. The new devices use a high-defect-density interface as the trap storage medium. As such, in these devices the drain voltage does not affect the threshold voltage or the saturation current. The SiN_x trap memory TFT exhibits excellent program, erase, and retention characteristics. Furthermore, the fabrication process is fully compatible with conventional a-Si technology. Therefore, the ST-TFT may be an excellent candidate for integrated memory in large-area electronics based on a-Si.

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