

A Three-Dimensional Folded Dynamic RAM in Beam-Recrystallized Polysilicon

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Abstract—A three-dimensional folded one-transistor dynamic RAM circuit consisting of an access transistor in a beam-recrystallized polysilicon layer above a storage capacitor has been fabricated. Large cell capacitance and low transistor leakage are obtained by use of multiple polysilicon layers and by folding the storage capacitor beneath the access transistor. The resulting storage times are longer than 1 min, several orders of magnitude greater than storage times in a previously published nonfolded dynamic RAM in recrystallized polysilicon [1].

I. INTRODUCTION

CONVENTIONAL one-transistor dynamic RAM's are limited in their retention time by carrier generation in and around the depletion region that forms beneath the stored charge. To circumvent this problem, Jolly *et al.* [1] proposed a circuit with the access transistor fabricated in silicon-on-insulator (SOI). The stored charge is then completely isolated by oxide as shown in Fig. 1. Charge retention in this circuit is limited only by access transistor source-drain leakage, assuming fields low enough to avoid tunneling through the oxide. However, subthreshold conduction in SOI MOSFET's is a strong function of the bias on the substrate due to weak inversion at the back interface [2], [3], and thus Jolly *et al.* needed a large negative voltage on the substrate to achieve maximum storage times.

The circuit of Jolly *et al.* can be improved by applying the folding principle [4] to take full advantage of the three dimensional possibilities of SOI. To demonstrate this process, we have folded the storage capacitor of the planar SOI dynamic RAM under the access transistor and arrived at the cell structure shown schematically in Fig. 2. Active portions of the third polysilicon level (P3) are beam recrystallized to achieve device-worthy material. No special processing is needed for the first two polysilicon layers. The primary storage capacitance is between the first polysilicon level (P1) and the substrate. The second polysilicon level (P2), known as the plate, serves to increase cell capacitance and more importantly to provide the bias needed to ensure minimal leakage on the back surface of the overlying access transistor. Thus the substrate can be kept at any potential desired for possible conventional peripheral circuitry in the substrate. Since a relatively thick oxide (6000 Å) between polysilicon layers P2 and P3 shields the underlying structure from excessively high temperatures

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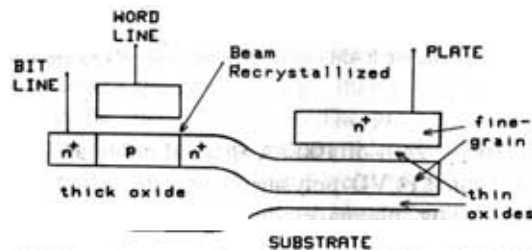


Fig. 1. Schematic cross section of a dynamic RAM cell of Jolly *et al.*

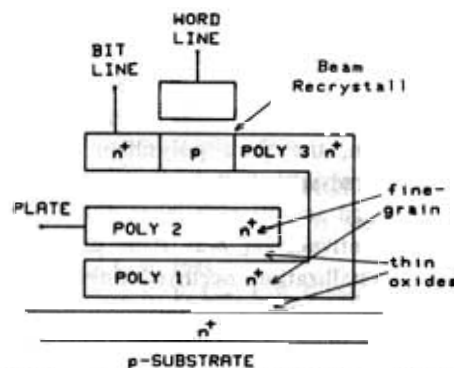


Fig. 2. Schematic cross section of a folded dynamic RAM cell.

during laser processing, the lower two oxides can be made as thin as possible to increase cell capacitance. In our experiments a conservative thickness of 1000 Å for these oxides was used. The advantages of an SOI structure noted by Jolly *et al.*, such as reduced bit-line capacitance (no substrate diffusions) and high immunity from alpha particles and other minority-carrier sources in the substrate, are retained in the structure.

The cell layout is shown in Fig. 3. Note that the polysilicon area P1 is as large as the cell itself. With the extra P1-P2 capacitance, the effective storage capacitor area can actually be larger than the cell area. Cells of various sizes were fabricated, the smallest measuring 30 μm \times 40 μm . In order to measure cell operation, a test structure similar to that of Jolly *et al.* was integrated into the test chip. This circuit monitors on-chip bit-line voltage by using a source-follower transistor and provides the ability to precharge the bit line before reading from the cell.

II. FABRICATION

The starting materials were p-type (100) 5-10 $\Omega\cdot\text{cm}$ silicon wafers, which were doped n⁺ on the front side by a 30-min POCl₃ diffusion at 975°C and a 30-min drive-in at

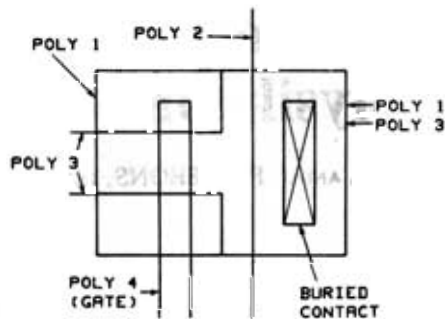


Fig. 3. Folded dynamic RAM cell layout (smallest cell $30\ \mu\text{m} \times 40\ \mu\text{m}$).

1100°C . After growth of 1000-\AA thermal oxide at 1100°C in dry O_2 , $0.5\text{-}\mu\text{m}$ LPCVD polysilicon was deposited at 620°C and patterned by plasma etching. This layer was similarly doped n^+ and oxidized at 1100°C to a thickness of $1000\ \text{\AA}$. The second polysilicon layer (plate) was then deposited by LPCVD, doped n^+ , patterned by plasma etching, and oxidized to $1000\ \text{\AA}$. $5000\ \text{\AA}$ of silox was then deposited at 450°C at atmospheric pressure to act as a heat shield during the later recrystallization process. After a buried contact masking and etch step which formed the contact between the first and third levels of polysilicon, the third polysilicon layer was then deposited and covered with $800\ \text{\AA}$ of silox to act as an anti-reflective coating and stabilization layer during recrystallization. This antireflective layer was then patterned so that melting and recrystallization occurred only in areas which were to become active transistor regions.

The laser recrystallization itself was performed with a scanning Ar^+ ion laser focused to a round spot of roughly $50\ \mu\text{m}$ in diameter. Laser powers used ranged from 6.0 to $8.0\ \text{W}$. The laser scan rate was $20\ \text{cm/s}$ and adjacent scan lines were overlapped by $20\ \mu\text{m}$. The substrate was preheated to 300°C . No seeding technique was used, and the resulting grains, as revealed by a Secco etch, measured roughly $4\ \mu\text{m} \times 20\ \mu\text{m}$ in random directions.

After cap removal, the third poly layer (recrystallized in some areas) was implanted with B^+ at several energies to obtain a reasonably uniform B doping of $10^{16}\ \text{cm}^{-3}$ throughout the film. This layer was then patterned using plasma etching to remove about $2000\ \text{\AA}$ of material and local oxidation to convert the remaining material to silicon dioxide. After nitride and pad oxide removal, $1000\ \text{\AA}$ of gate oxide was grown in dry O_2 at 1100°C . A fourth layer of polysilicon was then deposited as gate material and defined by plasma etching. Source-drain areas were doped by a 30 min 975°C POCl_3 predeposition and 1-h 1000°C drive-in. No effort was made to minimize grain-boundary diffusion of the source-drain dopant in this process run. Processing was completed by $6000\ \text{\AA}$ of P-glass deposition and densification, contact hole etch, P-glass reflow (1000°C , 30'), $1.5\text{-}\mu\text{m}$ e-beam Al deposition, a 20-min 450°C forming gas anneal, and finally metal lithography and etching.

III. MEASUREMENTS

Transistor threshold voltage in the recrystallized layer was approximately $1.0\ \text{V}$ and effective surface mobility varied

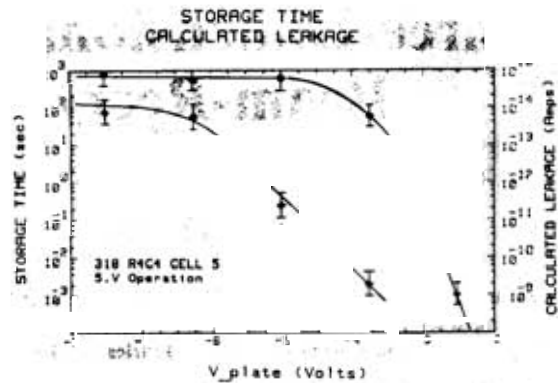


Fig. 4. Measured storage time and estimated leakage as a function of plate voltage.

from 50 to over $200\ \text{cm}^2/\text{V}\cdot\text{s}$, not surprising considering the simple recrystallization technique and resulting grain-boundary dopant diffusion. Dynamic RAM measurements were made on a storage cell which measured $30\ \mu\text{m} \times 40\ \mu\text{m}$. Calculated cell capacitance with 1000-\AA "thin" oxides is $0.6\ \text{pf}$ and calculated bit-line capacitance is $4.1\ \text{pf}$, giving a bit-line-to-cell capacitance ratio of 7 . The access transistor mask dimensions were $W = L = 10\ \mu\text{m}$, but grain-boundary diffusion reduced the effective L to an estimated $5\ \mu\text{m}$.

As expected, storage time was strongly dependent on the plate voltage, varying from less than $1\ \text{ms}$ to greater than $1\ \text{min}$ as the plate voltage was varied from -2 to $-8\ \text{V}$ (Fig. 4). storage time was defined as the time required between the WRITE and READ cycles, for the output signal to be reduced to $1/3$ of its maximum value. Measurements were made with logic levels of 0 and 5-V , and a 2.5-V bit-line precharge between the WRITE and READ cycles. Note that storage times for a logic "0" ($0\ \text{V}$) were consistently lower than those for a logic "1". This is because the gate-source voltage of the access transistor during storage is about $-2.5\ \text{V}$ for a stored "1", but $0\ \text{V}$ for a stored "0". As shown in Fig. 5, subthreshold source-drain leakage is a strong function of the top-gate voltage (V_{gs}), in addition to the plate voltage (bottom gate). In the case of a stored "0", initial leakage during storage would be large, but as the voltage on the storage node increased, leakage would decrease sharply due to a more negative gate-source voltage. In the case of a stored "1", gate-source voltage is fixed since the source is the bit line at $2.5\ \text{V}$, giving $V_{gs} = -2.5\ \text{V}$. Our maximum storage time for a "0" ("0" being a worse case) is over $1\ \text{min}$. Allowing a factor of 10 for our larger cell capacitance, this is an improvement of over 100 (1000 for a "1") from the maximum storage of $20\ \text{ms}$ reported by Jolly *et al.*

IV. DISCUSSION

From cell capacitance and storage times, leakage currents through the access transistors are estimated in Fig. 5. (Note these currents are not exact since, as just explained, leakage currents are expected to change with stored charge.) The minimum calculated current for a "1" is $10^{-15}\ \text{A}$ (corresponding to $10^{-16}\ \text{A}/\mu\text{m}$ of gate width), which is more than two orders of magnitude less than the lowest reported leakage currents in SOI MOSFET's known to the authors. We have

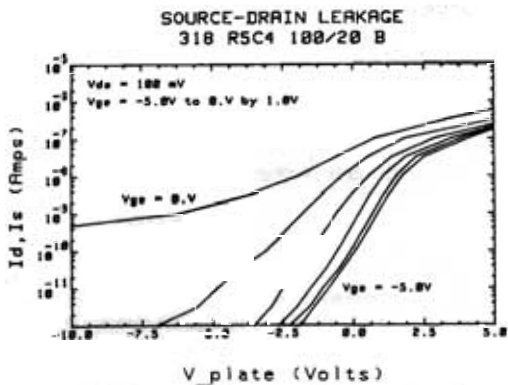


Fig. 5. Measured leakage as a function of plate voltage for various gate voltages.

no explanation for the unusually low leakage currents. Possibilities include the recrystallized layer being on silox rather than on thermal oxide, a very flat horizontal thermal profile during recrystallization due to the intermediate poly layers, and the fact that the boron doping of the layer was done after rather than before recrystallization. The interface state densities at the bottom of the recrystallized polysilicon film were calculated from the bottom parasitic transistor threshold voltage and subthreshold slope. The resulting fixed-charge density of $1.3 \times 10^{11} \text{ cm}^{-2}$ and fast state density of $2 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ are not unusually low for SOI structures.

The ultimate leakage limit once the subthreshold currents are reduced by negative gate voltages is the junction leakage from the reverse-biased drain junction. This current is a strong function of temperature, and one expects decreased storage times at high temperature. Indeed maximum storage times at 100°C were 200 ms and 1 s for a "0" and "1", respectively. Further experiments are currently underway to identify the reasons for the low transistor leakage.

For processing simplicity, the fabrication process used was not optimized for VLSI compatibility. The minimum linewidth was $5 \mu\text{m}$ and threshold voltages varied $\pm 0.3 \text{ V}$ across a wafer. However, other SOI research has shown that threshold voltages can indeed be uniformly controlled [5]. By using rapid thermal annealing to control source-drain dopant diffusion, SOI MOSFET's with $2.0\text{-}\mu\text{m}$ channel lengths have recently been successfully fabricated despite the presence of grain boundaries [6]. Scaling the folded SOI cell using average process parameters of real 256K DRAM cells ($2\text{-}\mu\text{m}$ design

rule, $250\text{-}\text{\AA}$ thin oxide) [7], one finds that the SOI and real cells have comparable area ($70 \mu\text{m}^2$) but that the SOI cells has ~ 50 -percent greater storage capacitance ($75 \text{ V}\cdot\text{s}$, 50 fF). 75 fF is an order of magnitude less than the capacitance of the demonstrated cell, but storage time would be expected to decrease only by a factor of two due to decreased leakage from a narrower access transistor.

V. CONCLUSIONS

A folded "high-rise" dynamic RAM structure in beam-recrystallized polysilicon has been presented. Storage times are orders of magnitude longer than those previously reported in a similar planar structure. The process is capable of being scaled and can be made compatible with VLSI. With refresh time specifications of commercial dynamic RAM's in the millisecond range [8], our high-temperature storage times of over 100 ms demonstrate that SOI technology is a viable competitor to conventional processing.

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