Hole Mobility Enhancement in MOS-Gated Ge_xSi_{1-x}/Si Heterostructure Inversion Layers

P. M. Garone, V. Venkataraman, and James C. Sturm, *Member, IEEE*

Abstract—**Effective hole mobility enhancements of 50% at room temperature and over 100% at 90 K, compared to all-Si controlled devices, are demonstrated by placing a buried epitaxial Ge_xSi_{1-x} layer 7.5 to 10.0 nm beneath the gate oxide of a PMOS transistor. Also mobility degradation caused by misfit dislocations in the inversion region is seen in structures with Ge_xSi_{1-x} layers that exceed the equilibrium critical thickness.**

I. Introduction

The mobility of carriers in the inversion layer of a MOSFET is significantly less than that of carriers in the bulk semiconductor. The mobility reduction is caused by surface scattering of the carriers, which are closely confined to the Si/SiO_2 interface by the strong transverse electric field of the gate. This fact is particularly troublesome for Si PMOS devices since CMOS device performance has been limited by the lower intrinsic mobility of holes. It has been proposed by several groups that moving the holes away from the Si/SiO_2 interface by confining them in a Ge_xSi_{1-x} quantum well would improve their mobility [2]–[4], and it has been shown by capacitance–voltage [3], [4] and Hall effect measurements [4] that p-channel inversion layers can indeed be formed in the Ge_xSi_{1-x} layers before an inversion layer forms at the Si/SiO_2 interface.

In this letter we report clear experimental evidence that such structures do result in enhanced hole mobility. *Effective* mobility improvements of 50% at 300 K and over 100% at 90 K compared to all-Si control devices are reported over a wide range of gate voltages.

II. Fabrication

The device structures were grown epitaxially on n-type Si (100) substrates by rapid thermal chemical vapor deposition [5] at a pressure of 6.0 torr. The Ge_xSi_{1-x} layers were grown at 600 to 625°C with a film thickness of 10 nm and the Si spacer layers were grown at 700°C. The epitaxial films are doped n-type with concentrations of $\approx 1 \times 10^{16}$ cm^{-3}. The vertical device structures are similar to those reported in [4]. MOSFET's were fabricated in the Ge_xSi_{1-x} structures as well as in a Si (100) wafer ($N_D \approx 10^{15}$ cm^{-3}) which was included as a control. Long-channel (7 to 200 μm) PMOS devices were fabricated using a non-self-aligned aluminum gate process in order to measure the low-field effective mobility. Low-temperature processing was utilized throughout in an effort to avoid diffusing or relaxing the strained Ge_xSi_{1-x} layers. Sources and drains were implanted with boron at 25 and 50 kV with a total dose of 5×10^{14} cm^{-2}. The gate oxide was deposited at 350° C by plasma-enhanced CVD to a thickness of 12.5 nm. This deposition was followed by a 700°C/30-min N_2 furnace anneal, which served as both an implant anneal and to improve the quality of the gate oxide. Contact holes for the source and drain were opened and aluminum was evaporated to form the gate and source/drain contacts.

Three variations of the MOS-gated Ge_xSi_{1-x}/Si heterostructure were grown. Sample 646 had a $Ge_{0.2}Si_{0.8}$ well with a 7.5-nm Si spacer layer, sample 649 had a $Ge_{0.3}Si_{0.7}$ well with a 10.5-nm Si spacer, and sample 650 had a $Ge_{0.4}Si_{0.6}$ well with a 7.5-nm Si spacer. The Ge fractions in samples 646 and 649 were confirmed by photoluminescence. Simulations using a 1-D Poisson solver [4] predict that the structures of both sample 646 and sample 649 will have a maximum hole concentration of $\approx 1 \times 10^{12}$ cm^{-2} in the Ge_xSi_{1-x} well. The holes added to the inversion layer at the Si/SiO_2 interface should have an effective mobility similar to that of a typical PMOS device, so any performance enhancement should be derived only from the holes in the Ge_xSi_{1-x} inversion layer.

III. Results and Discussion

At room temperature the drain conductance of MOSFET's with a 97-μm gate length and 315-μm width was measured with zero source-substrate bias and a small drain bias of −0.2 V. The MOSFET's from sample 646, which have a 7.5-nm Si spacer, had a 25% larger drain current than the Si control devices, and the MOSFET's from sample 649, which have a 10.5-nm Si spacer, had a 50% larger drain current over a wide range of gate voltage (Fig. 1). Note that the curves were normalized for small ($\approx$ 0.2 V) differences in the threshold voltage in order to compare the currents at approximately equal carrier concentrations.

At this time we are not able to determine what portion of the enhanced performance is due to the increased separation of the carriers in the Ge_xSi_{1-x} well from the surface scatter-

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The authors are with the Department of Electrical Engineering, Princeton University, Princeton, NJ 08544.

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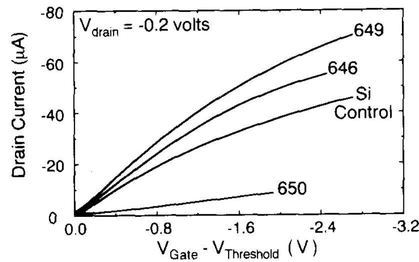

Fig. 1. Comparison of drain conductance, measured on 97-μm gate length MOSFET's, between Ge_xSi_{1-x}/Si structures and a Si control device. Sample 646 has a $Ge_{0.2}Si_{0.8}$ well with a 7.5-nm Si spacer, sample 649 has a $Ge_{0.3}Si_{0.7}$ well with 10.5-nm Si spacer, and sample 650 has a $Ge_{0.4}Si_{0.6}$ well with a 7.5-nm Si spacer. The $Ge_{0.2}Si_{0.8}$ and $Ge_{0.3}Si_{0.7}$ devices perform better than the Si control device, 25% and 50%, respectively, while the $Ge_{0.4}Si_{0.6}$ sample performs far worse.

ing sites and that which is due to the strain-induced lowering of the hole effective mass [6].

Subthreshold curves (see Fig. 2) are well behaved for samples 646, 649, and the all-Si control. These Ge_xSi_{1-x} MOSFET's, which have Ge_xSi_{1-x} layers below or near the critical thickness, have the same subthreshold slope (75 mV/decade) as those of the Si devices, which indicates that the presence of the buried Ge_xSi_{1-x} layer did not induce excessive interface states.

The effective mobility was extracted from similar measurements with a drain bias of -0.1 V in the manner of Sabnis and Clemens [7] using $\eta = 1/3$ for the effective vertical field [8] (i.e., $E_{\rm eff} = (1/\epsilon_{\rm Si}) \times (Q_{\rm dep} + \eta \times Q_{\rm inv})$). In these calculations a fixed gate capacitance equal to that of the oxide capacitance was assumed in estimating the carrier concentrations ($Q_{\rm inv} = C_{ox} \times (V_g - V_t)$). Because of the increased separation of carriers in the Ge_xSi_{1-x} well from the gate, the actual gate capacitance in these devices is lower than that of C_{ox}. This method of estimating the inversion layer charge therefore results in an overestimate of the number of carriers in the Ge_xSi_{1-x} devices and a corresponding underestimate of the actual hole mobility. The extracted effective mobilities, however, are useful for a relevant technological comparison of the device structures. The inversion charge was also estimated using simulations of the given structures [4] (corrected mobility). Estimates of the inversion charge from quasi-static *CV* measurements were not possible due to excessive leakage current though the gate oxide (≈ 18 pA).

At room temperature sample 649 had a peak mobility of over 290 $cm^2/V \cdot s$ and a 50% enhancement of the effective mobility across the whole range of effective fields (i.e., gate voltages) as shown in Fig. 3. We assume that the peak mobility of our devices was limited by the high fixed charge in the plasma-deposited oxide [9] ($6–8 \times 10^{11}$ cm^{-2} as measured by high-frequency *CV* characteristics). This was suggested by the relatively low values of effective mobility seen in our Si control devices compared to previously published data using thermal oxides [10]. Despite this processing limitation, the performance of sample 649 is seen to be 25% better than that of the results [10] using thermal oxides and is better than that seen with similar SiGe-MODFET structures

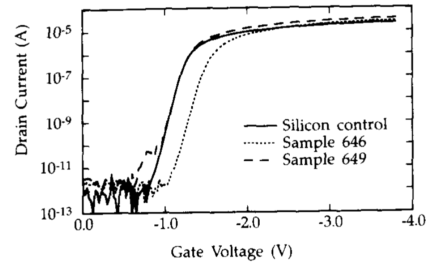

Fig. 2. Comparison of subthreshold current, measured on 97-μm gate length MOSFET's, between Ge_xSi_{1-x}/Si structures and a Si control device. Sample 646 has a $Ge_{0.2}Si_{0.8}$ well with a 7.5-nm Si spacer, and sample 649 has a $Ge_{0.3}Si_{0.7}$ well with 10.5-nm Si spacer. All devices have a subthreshold slope of ≈ 75 mV/decade.

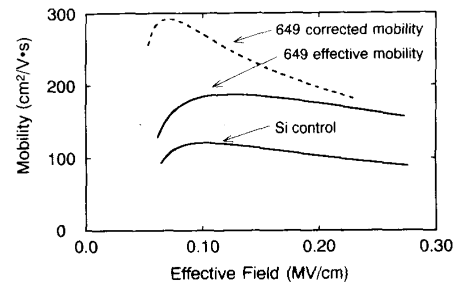

Fig. 3. Mobility versus effective (transverse) field at a temperature of 300 K. Comparison is between a Si control device and sample 649 which has a $Ge_{0.3}Si_{0.7}$ well with a 10.5-nm Si spacer. Both the effective mobility and the inversion layer mobility (calculated using simulated $Q_{\rm inv}$) are shown for the Ge_xSi_{1-x} device. The effective mobility of the Ge_xSi_{1-x} device is 50% better at 300 K.

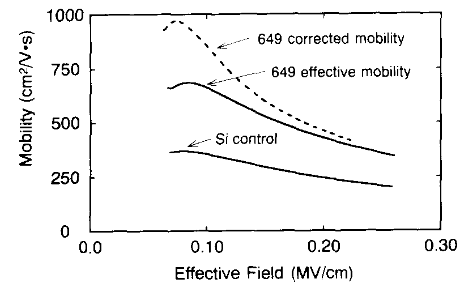

Fig. 4. Mobility versus effective (transverse) field at a temperature of 90 K. Comparison is between a Si control device and sample 649 which has a $Ge_{0.3}Si_{0.7}$ well with a 10.5-nm Si spacer. Both the effective mobility and the inversion layer mobility (calculated using simulated $Q_{\rm inv}$) are shown for the Ge_xSi_{1-x} device. The effective mobility of the Ge_xSi_{1-x} device is over 100% better at 90 K.

[11]. As the temperature is reduced the effective mobility enhancement of the Ge_xSi_{1-x} devices becomes progressively larger (Fig. 4). At 90 K sample 649 ($Ge_{0.3}Si_{0.7}$ well with a 10.5-nm Si spacer) exhibits an effective mobility enhancement of over 100% and a peak mobility of over 970 $cm^2/V \cdot s$ (Fig. 5). This increase in the enhancement at low temperatures is consistent with the reduced role of phonon scattering at low temperatures, which means that surface scattering processes, which should be lower in the Ge_xSi_{1-x} devices, will tend to dominate.

In contrast to the significant improvement in effective

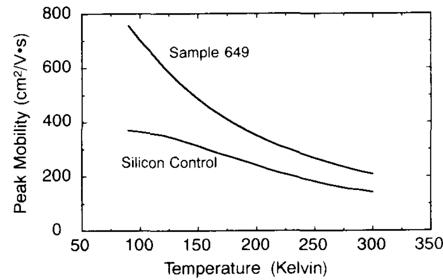

Fig. 5. Peak effective mobility versus temperature between 300 and 90 K. Comparison is between a Si control device and sample 649 which has a $Ge_{0.3}Si_{0.7}$ well with a 10.5-nm Si spacer. The mobility enhancement of the Ge_xSi_{1-x} device grows larger as the temperature is reduced. The peak effective mobility of sample 649 rises from 220 $cm^2/V \cdot s$ at 290 K to 780 $cm^2/V \cdot s$ at 90 K.

mobility seen in samples 646 and 649, the performance of PMOS devices made from sample 650, which has a $Ge_{0.4}Si_{0.6}$ well with a 7.5-nm Si spacer, was markedly worse (lowest curve in Fig. 2) than that of the Si control. In addition, electrical measurements showing poor lifetimes (capacitors would not deep deplete) and poor subthreshold slopes (twice those of the other devices) lead us to strongly suspect that this sample has misfit dislocations at the Si/Ge_xSi_{1-x} interface. This is consistent with the fact that this device has a $Ge_{0.4}Si_{0.6}$ well that is almost twice the equilibrium critical thickness [1] for this Ge fraction. The resulting misfit dislocations at the heterojunction interface would act as scattering sites to severely reduce mobility. It is not known whether the dislocations were process-induced or whether the as-grown layer was relaxed.

IV. Summary

Incorporation of a buried Ge_xSi_{1-x} epitaxial layer underneath the gate of a PMOS device can lead to a significant improvement in the effective mobility compared to a similar all-silicon device. Effective mobility enhancements of 50% at room temperature and over 100% at 90 K have been shown. For improved device performance it is essential to avoid the formation of misfit dislocations in the inversion layer.

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