Anomalous Subthreshold Slopes in Thin-Film Accumulation-Mode SOI p-Channel MOSFET's

Kenji Tokunaga
J. C. Sturm

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tion (V_{DS} = 5 V). In this brief we report that accumulation-mode p-channel devices may also exhibit anomalous subthreshold characteristics depending on the substrate bias condition.

Silicon-on-insulator films were formed by the SIMOX process, with an implant of 1.7×10^{18} cm^{-2} at 150 keV followed by annealing in 1% O_2/N_2 at 1250°C for 6 h. The underlying oxide thickness was 350 nm and the SOI thickness after annealing was 120 nm. Conventional FET fabrication (without LDD) was then performed using LOCOS isolation. The body of the device is doped with boron, typically $\sim 1.3 \times 10^{16}$ cm^{-3} and n^+ polysilcon was used as the gate material.

The film is fully depleted when the device of OFF [8] (at $V_G = V_{sub} = 0$ V). All voltages in this work were measured with respect to the source node which was grounded. In thin-film (100 nm) SOI p-channel MOSFET's, accumulation-type devices give appropriate threshold voltages [8], [9]. Fig. 1 shows the measured threshold voltage for top channel conduction in p-channel devices with L_g = 1.0 μm (V_{DS} = 100 mV). There are three distinct regions which can be related to the charge condition of the lower SOI–oxide interface [10]. Substrate voltages greater than 15 V lead to inversion (electron surface layer) at the lower SOI–oxide interface. Inversion pins the potential at the lower SOI–oxide interface, leading to no dependence of the threshold voltage on further substrate bias. For a substrate bias less than 10 V, the lower interface is depleted. In this case, electric field lines from the top channel are terminated in the substrate, and a dependence of the threshold voltage on substrate bias is observed. For a substrate bias less than -10 V, the back interface is accumulated. We will refer to these three regions later to interpret the subthreshold slope data.

Subthreshold characteristics were measured as a function of substrate voltage for various drain voltages (Fig. 2). Here we use the normalized inverse subthreshold slope n, defined by

$$S = \frac{nkT}{q} \ln 10 \qquad (1)$$

where S is the usual inverse subthreshold slope. The relationship between "n" and the capacitive divider were shown in [3]. At small drain biases ($|V_d| < 2$ V), a U-shaped curve is observed, whereas large drain biases lead to monotonic dependence of subthreshold slope on substrate bias.

II. Small Negative Drain Voltage

These results are explained by the model similar to the NMOS [3].

When the lower interface is accumulated, the initial conduction in the device will be at the lower SOI–oxide interface. There is a lower effective gate capacitance and a higher parasitic capacitance in this case compared to those for the depleted lower interface, a larger n is expected as is seen in Fig. 2.

When the lower interface is depleted, the initial conduction in the device will be at the upper SOI–oxide interface. The effective substrate capacitance becomes minimum, showing almost ideal subthreshold slope (n = 1.2–1.3).

When the lower interface is inverted (electron surface layer, very positive substrate bias), the lower interface potential is pinned. This introduces a large effective substrate capacitance coupled to the top SOI surface, which again degrades subthreshold slope. In this case the initial conduction in the device will be at the upper SOI–oxide interface.

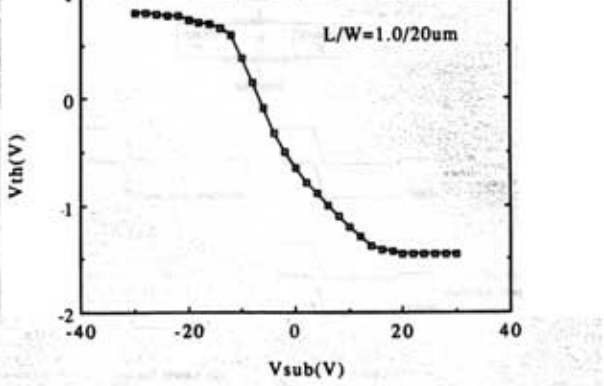

Fig. 1. PMOS top-channel threshold voltage as a function of substrate-source bias. L_g = 1.0 μm, W = 20 μm, and the drain voltage was 100 mV.

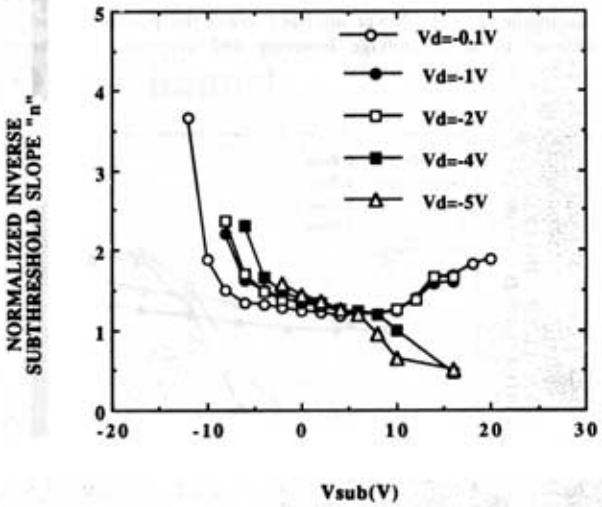

Fig. 2. PMOS normalized inverse subthreshold slope "n" as a function of substrate bias and drain voltage at room temperature. L_g = 1.0 μm, W = 20 μm.

III. Large Negative Drain Voltage

For a depleted lower interface, the subthreshold slopes are similar to those of the small drain voltage case.

For very positive substrate biases (inverted lower interface), however, the results differ substantially from the low drain bias case. The subthreshold slopes become anomalously "sharp" with $n < 1$. The effects are attributed to a small electron current caused by avalanche at the drain junction. The electrons get trapped in the SOI film body, lowering its potential, thus raising the threshold voltage which causes more hole current, and thus causing more electrons in a positive feedback process (Fig. 3). These results are similar to the inversion-mode n-channel SOI MOSFET though the trapped carrier is different [3], [4].

Fig. 4 shows the drain voltage dependence of normalized subthreshold slopes for various gate lengths for the case of a very positive substrate bias (electron layer at back interface). For gate lengths greater than 2 μm, no anomalous sharp slopes were observed. For shorter gate lengths, the sharp subthreshold slopes are observed for large drain voltages as in Fig. 2. One possible explanation is that there will be more recombination of the trapped charge in long-channel devices, so that the charge density does not exceed the critical number, at which the positive feedback process starts.

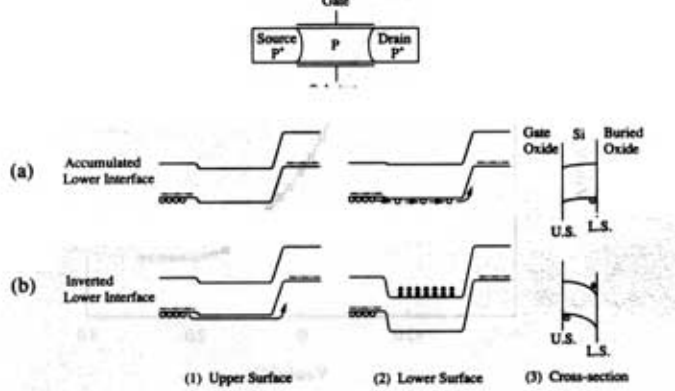

Fig. 3. Potential energy diagram of the (1) upper and the (2) lower surfaces of a depleted SOI transistor with (a) an accumulated (holes) lower interface, and (b) an inverted (electrons) lower interface. (3) Cross-sectional band diagram at the middle of the channel. U.S. and L.S. are abbreviations for the Upper and Lower Surfaces of the SOI, respectively. Electrons accumulated at the lower interface lower the potential, leading to front-channel threshold voltage lowering and anomalous subthreshold slopes.

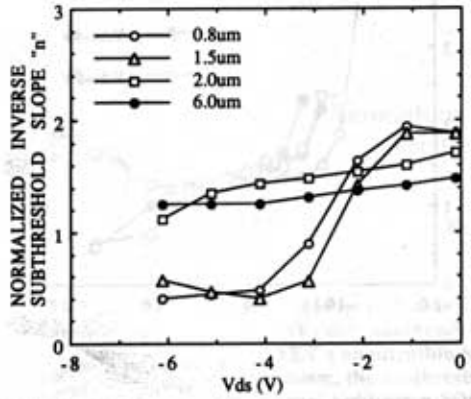

Fig. 4. PMOS normalized inverse subthreshold slope "n" as a function of drain voltage and gate length. The anomalously sharp subthreshold slope depends on the gate length. The numbers in the figure are gate lengths. (V_{sub} = 20 V, W = 20 μm).

IV. Conclusion

Anomalously sharp subthreshold characteristics in thin-film accumulation-mode SOI p-channel MOSFET's have been described. The slope depends on the charge state of the lower SOI–oxide interface. Impact ionization near the drain region and electron trapping at the backside interface with large substrate bias are the main factors for the largely varying subthreshold slope. Abnormally sharp subthreshold slopes can be avoided by an appropriate source–substrate bias.

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