Leakage Current Modeling of Series-Connected Thin Film Transistors

J. C. Sturm, I.-W. Wu, and M. Hack

***Abstract*— The leakage current of an arbitrary number of series-connected polysilicon Thin Film Transistors (TFT's) with a common gate is shown to be easily computed from the I-V characteristics of a single FET for the first time, both by an analytical model and by graphical techniques. Good agreement with experimental data is obtained for drain biases greater than ~1 V. The work is also applicable to single crystal Silicon-On-Insulator (SOI) TFT's.**

I. INTRODUCTION

In many TFT applications, the leakage current of the TFT in the off state is a critical parameter for proper circuit operation. This may be driven by power concerns, as in SRAM technology [1], [2], or in Active Matrix Liquid Crystal Display (AMLCD's) technology, to improve the grey scale by stabilizing the voltage on the liquid crystal [3]–[5]. In AMLCD technology using polysilicon transistors, to reduce the leakage current it is common practice to replace a single transistor with multiple transistors in series connected to a common gate [4]. Because of the highly nonlinear device behavior of this regime, with two transistors in series leakage current reductions of over an order of magnitude are common.

The purpose of this letter is to show that the leakage current characteristics of such multiple TFT's in series can be quickly computed from the characteristics of a single FET, which has not been previously recognized. An analytical model is given which, based on two parameters of a single FET, predicts the leakage current reduction obtained by placing an arbitrary number of TFT's in series.

II. OVERVIEW AND GRAPHICAL ANALYSIS

When two transistors are connected in series (Fig. 1(a.)) their drain currents must be equal, assuming no gate leakage. Therefore the voltage on the intermediate terminal, labeled $V_{D,1}$, must adjust itself to this condition. When the gate voltage of a typical polysilicon NMOS TFT is below some nominal value, e.g., -2 V in Fig. 2, the leakage current rises as the gate-source voltage becomes more negative. This is due to high-electric field tunneling at specific trap sites near the high-field drain region [6]–[8], resulting in a channel current dominated by holes. Also, the leakage current in this regime increases strongly as the drain voltage is increased. The top transistor will have its source at a higher voltage than the lower one, and hence have a more negative V_{GS} than the lower transistor. Therefore the applied V_{DD} will divide itself so that most of the applied voltage falls across the lower transistor, giving it a larger V_{DS} so that the two transistors have equal drain currents. When the gate voltage is such that the devices are in the classical subthreshold region and dominated by electron current in the channel ($V_{GS} > -2$ V in Fig. 1), I_D increases exponentially with increasing V_{GS} and is almost independent of V_{DS}, except decreasing with decreasing V_{DS} for V_{DS} much below 1 V. Because the lower transistor will have a more positive V_{GS} , causing a tendency toward much higher I_D, the drain voltage in this case will mostly fall on the upper transistor. Because of the the relatively weak V_{DS} dependence in this case (versus the V_{GS} dependence), a very small voltage is expected on $V_{D,1}$ (< 1 V) to accommodate for the difference in V_{GS}). These trends of voltage division were first qualitatively observed experimentally by Proano *et al.* [9] and then first analyzed (by performing a full 2-D two-carrier device simulation of the two transistor structure) in [10].

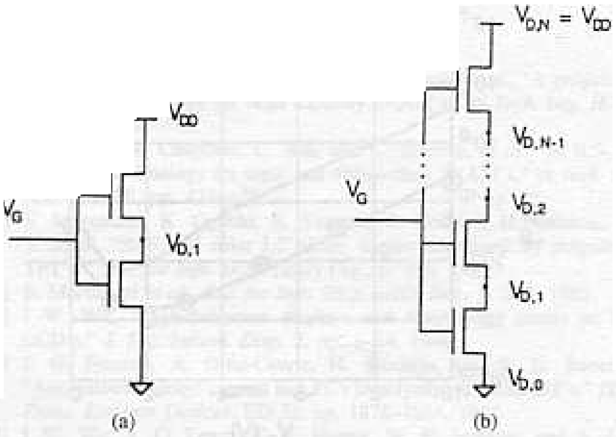


Fig. 1. Schematic diagram of (a) two and (b) N TFT's in series to reduce leakage current.

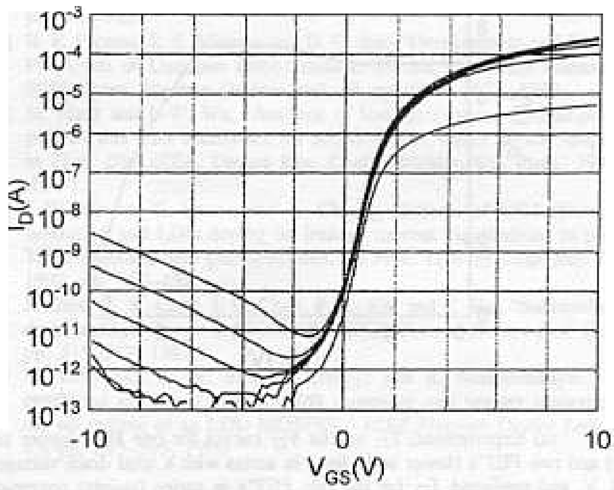


Fig. 2. Measured I-V curves for a single polysilicon TFT ($W = 40$ μm, $L = 20$ μm). V_{DS} varies from 0.1 to 10.1 V in 2.0 V steps. The gate oxide and channel polysilicon thicknesses were both 0.1 μm. No channel doping implant was performed. All process steps were at or below 600°C except a gate LTO oxygen densification step at 950°C (as in [7]).

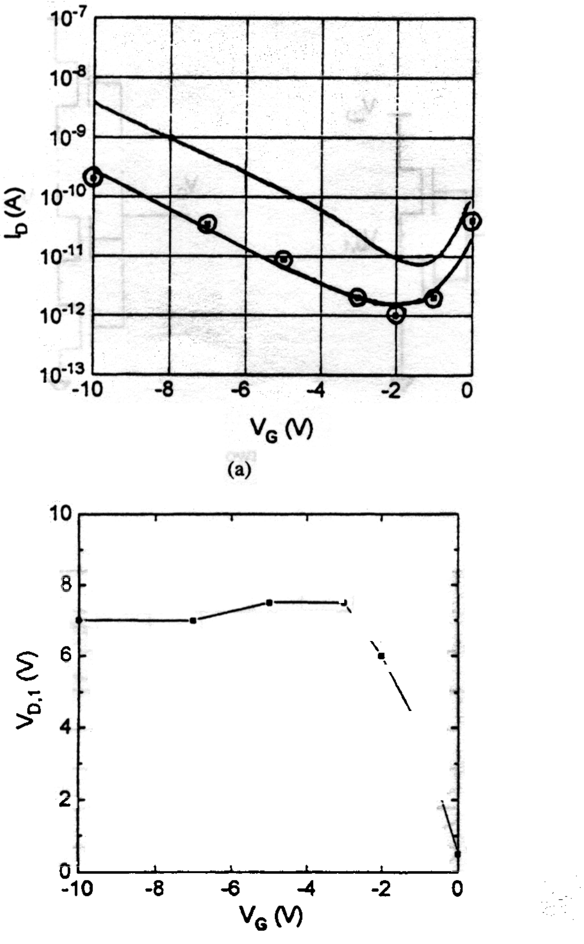
Because TFT's have no body effect, the I-V curves of Fig. 2 may be applied to either of the two FET's in series (with appropriate V_{GS} and V_{DS} definitions). Assuming the two FET's are independent

Manuscript received November 30, 1994; revised March 17, 1995. The review of this brief was arranged by Associate Editor W. F. Kosonocky. The work at Princeton was supported by DARPA through Grant USAF-TPSU-CCT-1464-966 and by Hitachi.

J. C. Sturm is with the Department of Electrical Engineering and the Photonic and Opto-Electronic Materials Center (POEM), Princeton University, Princeton, NJ 08544 USA.

I.-W. Wu and M. Hack are with the Xerox Palo Alto Research Center, Palo Alto, CA 94304 USA.

IEEE Log Number 9412376.



(a)

(b)

Fig. 3. (a) Experimental I_D versus V_G curves for one FET (upper solid line) and two FET's (lower solid line) in series with a total drain voltage of 10.1 V, and predicted I_D for the two FET's in series (points) constructed from the I-V curves of Fig. 2. All FET's have $W = 40\ \mu$ m and $L = 20\ \mu$m. (b) Predicted drain voltage on the lower FET as a function of V_G for the two FET's in series, constructed from the I-V curves of Fig. 2.

and not coupled in any way (e.g., by minority carrier holes passing through the common n^+ region from one channel to the other), Fig. 2 may be applied individually to each of the FET's in series. The I-V curves of the series connected pair (with a common gate voltage) can be graphically constructed from the data of Fig. 2. For each V_{GS} and V_{DD}, only one $V_{D,1}$ can be found such that the drain currents match in the two transistors. Fig. 3(a) shows the comparison of the experimental I-V curve for a single FET with $V_{DD} = 10$ V (from Fig. 2), the experimental data for two FET's in series (with total V_{DD} of 10 V), and the solution for the two transistors constructed as just described. (The upper TFT has a V_{gs} much more negative than that of the lower transistor due to its higher source voltage. Therefore for the graphical solution it was necessary to extrapolate the data of Fig. 2 to $V_{gs} < -10$ V.)

The graphical solution is in excellent agreement with the data, which indicates that the two transistors are indeed operating independently without any subtle coupling of minority carriers, etc. Second, note that the shapes of the two curves are similar for $V_{GS} < -2$ V, and that there is a leakage current reduction by a factor of ~ 17 over this range. The current for the series-connected pair is indeed not expected to be "flatter" than that for a single transistor, as was previously intuitively expected. Fig. 3(b) shows $V_{D,1}$ from the constructed solutions versus V_{GS}. Note that for $V_{GS} < -2$ V, more than half of V_{DD} falls on the lower transistor, as expected. Why the fraction is a constant (~ 0.7) will be analytically shown in the next section. For $V_{GS} > -2.0$ V, $V_{D,1}$ drops rapidly, with only ~ 0.5 V dropped on the lower FET for $V_G = 0$, consistent with the earlier discussion.

III. ANALYTICAL MODEL

In this section, based on an approximation to the I-V characteristics of a single TFT for negative gate voltages, an analytical expression is derived for the leakage current reduction when N ($N > 1$) FET's are connected in series compared to a single FET. Note that for sufficiently negative gate voltages, the drain current is exponentially dependent on both V_{GS} and V_{DS}. For example, in Fig. 2 I_{DS} approximately triples when drain voltage is increased by 1 V (for $V_{DS} > 1$ V), and doubles when the gate voltage is decreased by 1 V. We may therefore approximate I_D as

$$I_D = Ce^{aV_{DS} - bV_{GS}} \tag{1}$$

where C is an arbitrary constant, and a and b are constants found from an individual TFT. ($a \approx \ln 3\ \text{V}^{-1}$ and $b \approx \ln 2\ \text{V}^{-1}$ for the data in Fig. 2). Although many groups have studied the physical mechanisms governing leakage current in TFT's, (1) is not based on a physical model *per se*, but rather is based on an empirical fit to the data of Fig. 2. (Note (1) and the rest of the subsequent analysis is not valid for the low V_{DS} region ($V_{DS} < 1$ V) where the leakage current is dominated by electrons and is sublinearly dependent on V_{DS}, and only applies for the high-field case ($V_{DS} > 1$ V)). Using the notation of Fig. 1(b), expressing the V_{DS} and V_{GS} on each transistor in terms of $V_{D,i}$ and V_G, applying (1), and equating the currents in transistors i and i-1, one finds the recursive relationship

$$aV_{D,i} + (b - 2a)V_{D,i-1} + (a - b)V_{D,i-2} = 0, \quad \text{for } i = 2 \text{ through } N. \tag{2}$$

Applying boundary conditions $V_{D,N} = V_{DD}$ and $V_{D,0} = 0$, one can solve the above series of equations to yield

$$\frac{V_{D,i}}{V_{D,1}} = \frac{a^i - (a - b)^i}{a^{i-1}b}. \tag{3}$$

The fraction of the total drain voltage dropped over the lowest transistor (defined as η) is then

$$\eta \equiv \frac{V_{D,1}}{V_{DD}} = \frac{a^{N-1}b}{a^N - (a - b)^N}. \tag{4}$$

Since one now knows the drain voltage on the lowest transistor, one can easily calculate the leakage current for a given V_G. Note that a fixed fraction of total drain voltage is dropped on the lowest transistor, independent of V_{GS}. Because the leakage in the lowest transistor depends exponentially on the drain-source voltage, this implies a constant reduction in the drain current by a fixed factor independent of V_{GS}. Therefore on a logarithmic scale, the I-V curves for negative V_{GS} of the multiply connected set have the same "shape" or slope as those of a single transistor. As mentioned earlier, this previously has been experimentally observed

[11] but its origin was not understood. The only previous analysis of this problem involved a first-principles, two-dimensional, two-carrier device simulation of a two-transistor structure which reproduced the experimental trend [10].

The leakage current of the N transistors ($I_{L,N}$) versus that of a single transistor ($I_{L,1}$) across V_{DD} is then

$$\frac{I_{L,N}}{I_{L,1}} = \frac{e^{aV_{D,1}}}{e^{aV_{DD}}} = e^{-aV_{DD}(1-\eta)} \tag{5}$$

This is significant because it shows that the reduction in leakage current for multiple transistors in series can quickly be computed from the I-V curves of an isolated FET (without the need to derive a complicated device model that predicts the full range of I-V curves). Note that in using (4) and (5), however, one must make sure that $V_{GS} < -2$ V (for the device of Fig. 2) and that $V_{DS} > 1$ V for all transistors because of the region of applicability of (1). In practice, this limits N to 3 for $V_{DD} = 10$ V and N to 4 for $V_{DD} = 20$ V. Note that because FET's in single crystal silicon have behavior for negative gate voltages qualitatively similar to that described by (1) [12], [13], this result should also be applicable to SOI TFT's (where the body effect is not significant).

In the common application case of $N = 2$, (4) and (5) reduce to

$$\eta \equiv \frac{V_{D,1}}{V_{DD}} = \frac{a}{2a-b} \tag{6}$$

and

$$\frac{I_{L,2}}{I_{L,1}} = e^{-a(a-b)V_{DD}/(2a-b)}. \tag{7}$$

For the FET's of Fig. 2, from (5) one finds that ~0.7 of the applied V_{DD} will be dropped on the lower transistor. This is in good agreement with the graphical solution in Fig. 3 (~7 V for $V_{DD} = 10$ V). For a V_{DD} of 10 V, (7) predicts a 19-fold decrease in leakage current. This is also in good agreement with the graphically constructed and experimental results, showing the usefulness of the analytical approach. (Note that our approach does ignore statistical variations from one FET to the next, however. This can be handled analytically, at least in the case of $N = 2$, by letting the three constants in (1) vary in each device. Such analysis will be addressed in future work.)

IV. SUMMARY

We have shown that the leakage current characteristics of multiple TFT's connected in series can quickly be computed from the characteristics of a single FET using an exponential model of the FET for for negative V_{GS}. For negative gate voltages below the subthreshold region, the leakage current is reduced by a constant factor independent of V_G, and the largest fraction of the total drain voltage is dropped over the lowest FET. Once the subthreshold region is reached, however, most of the drain bias is dropped over the upper FET's.

ACKNOWLEDGMENT

The authors acknowledge the analytical expertise of P. Ramadge on recursive relations.

REFERENCES

[1] S. Ikeda, S. Hashiba, I. Kuramoto, and H. Katoh, *et al.*, "A polysilicon transistor technology for large capacity SRAM's," in *Tech. Dig. IEDM*, 1990, pp. 469–472.

[2] R. Eklund, R. Chapman, C. Wei, and C. Blanton, *et al.*, "A 0.5- μm BiCMOS technology for logic and 4Mbit-class SRAM's," in *Tech. Dig. IEDM*, 1989, pp. 425–428.

[3] S. Morozumi, K. Oguchi, S. Yazama, T. Kodaira, H. Oshima, and T. Mani, "B/W and color LC video display addressed by polysilicon TFT's," *Soc. for Info. Disp. (SID) Dig.*, p. 156, 1983.

[4] S. Morozumi *et al.*, *Soc. for Info. Disp. (SID) Dig.*, p. 278, 1985.

[5] I.-W. Wu, "High-definition displays and technology trends in TFT LCD's," *J. Soc. Inform. Disp.* 2, pp. 1–14, 1994.

[6] J. G. Fossum, A. Ortiz-Conde, H. Shichijo, and S. K. Banerjee, "Anomalous leakage current in LPCVD polysilicon MOSFET's," *IEEE Trans. Electron Devices*, ED-32, pp. 1878–1884, 1985.

[7] I.-W. Wu, A. G. Lewis, T. Y. Huang, W. B. Jackson, and A. Chiang, "Mechanism and device-to-device variation of leakage current in polysilicon thin film transistors," in *Tech. Dig. IEDM*, 1990, pp. 867–870.

[8] M. Hack, I.-W. Wu, T. J. King, and A. G. Lewis, "Analysis of leakage currents in polysilicon thin film transistors," in *Tech. Dig. IEDM*, 1993, pp. 385–388.

[9] R. E. Proano, R. S. Misage, and D. G. Ast, "Development and Electrical Properties of Undoped Polycrystalline Silicon Thin-Film Transistors," *IEEE Trans. Electron Devices*, vol. 36, pp. 1915–1922, 1989.

[10] M. Hack and I.-W. Wu, "Analysis of leakage currents in multiple gate poly-Si thin film transistors for active matrix liquid crystal displays," in *Tech. Dig. IEEE*, Device Res. Conf., Boulder, CO, June, 1994, p. IIIA-7.

[11] I.-W. Wu, A. G. Lewis, and A. Chiang, "Effects of solid-phase crystallization and LDD doping on leakage current distributions in poly-Si TFT's with multiple gate structures," in *Proc. 12th Int. Disp. Res. Conf.*, 1992, pp. 455–458.

[12] J. Chen, T. Y. Chan, I. C. Chen, P. K. Ko, and C. Hu, "Subbreakdown drain leakage current in MOSFET," *IEEE Electron Device Lett.* EDL-8, pp. 515–517, 1987.

[13] M. Orlowski, S. W. Sun, P. Blakey, and R. Subrahmanyan, "The combined effects of band-to-band tunneling and impact ionization in the off regime of an LDD MOSFET," *IEEE Electron Device Lett.*, vol. 11, pp. 593–595, 1990.