Limited Reaction Processing: *In-Situ* Metal–Oxide–Semiconductor Capacitors

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Abstract—**Limited reaction processing (LRP) has been used to fabricate *in-situ* silicon-silicon dioxide-polycrystalline silicon layers for metal-oxide-semiconductor (MOS) capacitors. The process consists of multiple *in-situ* rapid thermal processing steps to grow or deposit different layers. Capacitors have been fabricated from these layers and analyzed by capacitance-voltage measurements for interfacial fixed charge and interface state density. The capacitors exhibit excellent characteristics.**

I. Introduction

THE metal-oxide-silicon (MOS) capacitor structure forms a crucial element in modern integrated circuit technology. The capacitor typically consists of an insulating layer (silicon dioxide) grown thermally on a polished silicon wafer. A conducting layer (originally metal but now usually heavily doped polycrystalline silicon) is then deposited on the insulator to form the "gate" electrode. Conventionally, the oxide is grown in one reactor and the wafer is physically transported to a second reactor for the polycrystalline silicon (polysilicon) deposition.

We report here the *in-situ* fabrication of the multilayer MOS structure using multiple rapid thermal processing steps. *In-situ* multilayer fabrication might avoid the inevitable chemical and particulate contamination that occurs when wafers are carried from the oxidation furnace to the polysilicon reactor. Such contamination could diffuse through the oxide during later high-temperature steps to the substrate–oxide interface where it would affect the performance of MOSFET's, etc.

II. Fabrication

Various individual rapid thermal processing steps such as silicon epitaxy [1] and thermal oxidation [2]–[4] have already been demonstrated in separate reactors. However, by changing the ambient gases between high-temperature cycles (from oxygen to silane, e.g.), multiple thin layers of different composition (oxides, polysilicon, etc.) can be grown in a single reactor without removing the sample from the processing chamber. In our experiments, the "limited reacton processing" (LRP) system described in [1] was used for the multiple-level *in-situ* growth. Because the system is essentially a cold wall reactor without a susceptor, only the wafer gets heated during a deposition or growth cycle. Thus "history" effects from one cycle to the next from wall and susceptor deposition should be negligible.

To fabricate the capacitor structure, the two steps of rapid gate oxidation and polysilicon deposition were sequentially performed in the LRP chamber without disturbing the wafer between the steps. The wafers used for the experiments were 2-in diameter phosporus-doped (100) silicon wafers with a resistivity of $\sim 3\ \Omega\cdot$cm. After a chemical cleaning, the wafers were loaded into the LRP chamber. The gate oxidation was performed in an oxygen ambient with 4-percent HCl at a temperature of 1150°C and a pressure of 500 torr. A typical oxidation time of 2 min yielded an oxide thickness of from 290 to 310 Å. Because of the reduced pressure and relatively short time at high temperature, a direct comparison of the oxide thickness to that expected with conventional equipment is not possible. After the high-temperature step, the process gases were changed, and a layer of heavily boron-doped polysilicon was deposited using a combination of silane, diborane, and hydrogen as the source gases. It should be noted that the source gas flow was stabilized before the heating lamps were turned on, so that the wafer temperature and not the gas flows determined the start and stop of the deposition reaction. The polysilicon layers were deposited at 580°C at a pressure of 1.5 torr. The layer thickness was about 0.4 μm, and the sheet resistivity of the layers ranged from 50 to 100 Ω. Conventional deposition of "polysilicon" below 600°C usually results in amorphous rather than polycrystalline material [5]. However, defect etching indicated that our deposited polysilicon layers were indeed polycrystalline. We have not pursued the cause of this result.

To provide a comparison with conventional processing, a control wafer was processed exactly as above, except that it was removed from the LRP chamber after the oxidation and given a chemical cleaning to simulate conventional handling. It was then reloaded into the LRP chamber for the polysilicon gate deposition.

After the polysilicon deposition, conventional processing and photolithography were performed on all samples to change the uniform layers (Fig. 1(a)) into the final capacitor structure shown in Fig. 1(b). The final processing step was a 375°C forming gas anneal (90-percent N_2, 10-percent H_2).

III. Results

Conventional high- and low-frequency capacitance–voltage (CV) measurements were performed to measure the quality of the substrate silicon–silicon dioxide interface (see [6] for a

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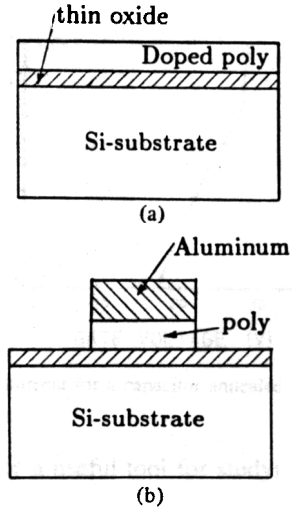

Fig (a) The structure created *in situ* by LRP and (b) the finished capacitor structure.

good review of *CV* techniques). From the high-frequency curve, the oxide thickness, substrate doping, and the interfacial fixed charge N_f can be extracted. From a combination of the two curves, the interface state density D_{it} can be calculated [6], [7]. The capacitor area was 4.5×10^{-3} cm^2. Several capacitors were measured on each sample for statistical significance. The effect of mobile ions on N_f, as revealed by bias-temperature stress measurements, was less than 1×10^{10} cm^{-2}.

The measured high- and low-frequency *CV* curves exhibited the classical shape [6], and the extracted interface state density of all samples yielded the conventional *U*-shaped curve with a minimum near midgap. The extracted substrate dopings were consistent with the resistivities of the starting wafers. Both the *in-situ* sample (LRP 91) and the sample that received an external chemical cleaning between the oxidation and the polysilicon deposition (LRP 90) showed midgap interface state densities of $2\text{–}3 \times 10^{10}$ cm$^{-2}\cdot$eV^{-1}. Sample LRP 91 had an interfacial fixed charge of $2.5 \pm 0.1 \times 10^{11}$ cm^{-2}, compared to a fixed charge of $2.1 \pm 0.1 \times 10^{11}$ cm^{-2} for sample LRP 90.(A difference in work functions between the gate and an intrinsic substrate Φ_{ms} of 0.54 eV was assumed [8].) Fixed charges and interface state densities in these ranges are typical for conventional thermal oxides grown at 1150°C and not annealed at high temperature in an inert ambient [9]. It is not known if the difference in fixed charge between the two samples is significant or represents a normal run-to-run variation. It is possible that removing LRP 90 from the chamber and subjecting it to a chemical cleaning would lead to a different Φ_{ms} than for the sample processed *in situ* because of an interfacial dipole layer [8].

After the polysilicon deposition, one of the samples processed *in situ* received a further 1150°C 15-s anneal in an argon ambient. It is well known that such anneals improve interface quality [4], [9], [10]. The high- and low-frequency *CV* curves for this sample are shown in Fig. 2, and the interface state density is shown in Fig. 3. With the anneal, the midgap interface state density decreased to $\sim 5 \times 10^9$ cm^{-2} eV^{-1}, indicative of an excellent interface. The fixed charge

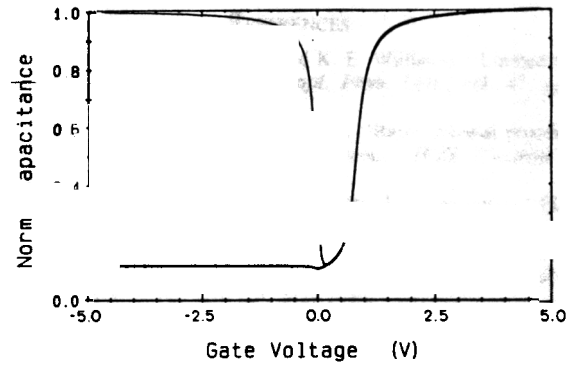

Fig. 2. Typical *CV* curves for an *in-situ* MOS capacitor (1150°C 15-s anneal) with an area of 4.5×10^{-3} cm^2. The capacitance values have been normalized to the maximum capacitance of 504 pF.

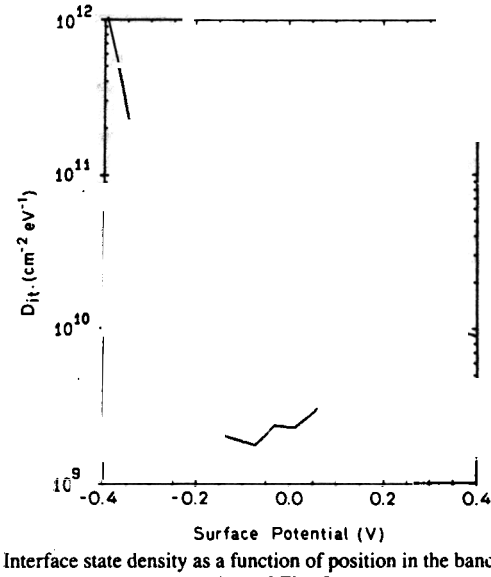

Fig. 3. Interface state density as a function of position in the bandgap for the capacitor of Fig. 2.

measured $0 \pm 1 \times 10^{10}$ cm^{-2}. Although such a interface charge is unusual, an error in the assumed Φ_{ms} of only 0.03 eV would change the calculated N_f by 2×10^{10} cm^{-2}.

To further probe the oxide quality, tunneling current measurements were performed. Fig. 4 shows the tunneling current in an annealed, *in-situ* polysilicon capacitor of area 4.5×10^{-3} cm^2. The gate was biased positive to inject electrons from the substrate into the oxide. (Because of a larger barrier height [11], hole tunneling from the gate into the oxide can be ignored.) The voltage was scanned five times, but the first four times the scan was stopped 4 V before destructive breakdown. The fact that the curves fall on top of one another indicates good oxide stability. On the fifth scan, the voltage was increased until breakdown. The breakdown field of 10 MV/cm is that expected for high-quality SiO_2 films.

IV. Summary

In summary, the use of limited reaction processing to fabricate *in-situ* multiple layers for MOS capacitors has been demonstrated. The fabricated capacitors exhibit excellent characteristics. The ability to deposit gate electrode layers *in*

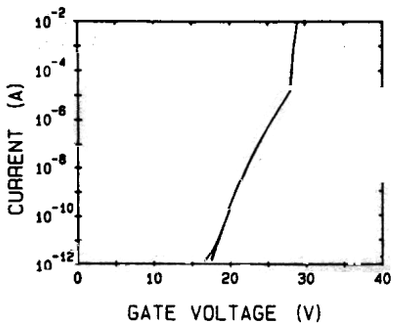

Fig. 4. Tunneling current for a capacitor annealed at high temperature.

situ should provide a useful tool for studying gate electrode–semiconductor work function differences. Larger scale experiments are still needed, however, to evaluate the process yield and uniformity implications of *in-situ* multiple layers.

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References

[1] J. F. Gibbons, C. M. Gronet, and K. E. Williams, "Limited reaction processing: Silicon epitaxy," *Appl. Phys. Lett.*, vol. 47, pp. 721–723, 1985.

[2] J. Nulman, J. P. Krusius, and A. Gat, "Rapid thermal processing of thin gate dielectrics—Oxidation of silicon," *IEEE Electron Device Lett.*, vol. EDL-6, pp. 205–207, 1985.

[3] J. Nulman, J. Scarpulla, T. Mele, and J. P. Krusius, "Electrical characteristics of thin gate implanted MOS channels grown by rapid thermal processing," in *IEDM Tech. Dig.*, 1985, pp. 376–379.

[4] A. Gat, "Rapid thermal processing of gate dielectrics," *Semiconductor Int.*, vol. 8, pp. 120–124, May 1985.

[5] T. I. Kamins, M. M. Mandurah, and K. C. Saraswat, "Structure and stability of low pressure chemically vapor-deposited silicon films," *J. Electrochem. Soc.*, vol. 125, pp. 927–932, 1978.

[6] E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology*. New York: Wiley, 1982.

[7] M. Kuhn, "A quasi-static technique for MOS C-V and surface state measurement," *Solid State Electron.*, vol. 13, pp. 873–885, 1970.

[8] T. W. Hickmott and R. D. Isaac, "Barrier heights at the polycrystalline silicon-SiO_2 interface," *J. Appl. Phys.*, vol. 52, pp. 3464–3475, 1981.

[9] B. E. Deal, "The current understanding of charges in the thermally oxidized silicon structure," *J. Electrochem. Soc.*, vol. 121, pp. 198C–205C, 1981.

[10] A. I. Akinwande, C. P. Ho, and J. D. Plummer, "Experimental determination of the temperature dependence of argon annealed fixed oxide charge at the Si/SiO_2 interface," *Appl. Phys. Lett.*, vol. 45, pp. 263–265, 1984.

[11] M. Lenzlinger and E. H. Snow, "Fowler-Nordheim tunneling into thermally grown SiO_2," *J. App. Phys.*, vol. 40, pp. 278–283, 1969.