25-nm p-Channel Vertical MOSFET's with SiGeC Source-Drains

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Abstract— The scaling of vertical p-channel MOSFET's with the source and drain doped with boron during low temperature epitaxy is limited by the diffusion of boron during subsequent side wall gate oxidation. By introducing thin SiGeC layers in the source and drain regions, this diffusion has been suppressed, enabling for the first time the scaling of vertical p-channel MOSFET's to under 100 nm in channel length to be realized. Device operation with a channel length down to 25 nm has been achieved.

I. INTRODUCTION

VERTICAL MOSFET's are attractive structures for short-channel MOSFET's because the channel length (L) may be determined by the thickness of an epitaxial layer instead of by lithography resolution. The chip area can also be reduced in some cases by using vertical structures [1], [2]. Furthermore by using ultrathin pillars (width <100 nm), the channel region can be fully depleted by surrounding gates, resulting in improved subthreshold slope and suppression of short-channel effects [3], [4]. Sub-100-nm n-channel vertical MOSFET's have already been reported [5], [6]. However the shortest previous results for vertical p-channel MOSFET's have L of 0.25 μm [7] for a uniform pillar structure and 0.13 μm for edges of selective epitaxy facets [8]. The main problem is the source/drain dopant (boron) diffusion during gate oxidation after epitaxy and pillar-formation, or during annealing after source and drain dopant implantation. In this work, we introduced novel SiGeC layers in source and drain to stop boron diffusion and hence successfully scaled the channel length down to 25 nm for the vertical p-channel MOSFET's.

II. DEVICE DESIGN AND FABRICATION PROCESS

The cross section of our initial vertical p-channel MOS-FET's without any SiGeC layers is shown in Fig. 1. The p^+np^+ epitaxial layers were grown by rapid thermal chemical vapor deposition on a Si (100) p-type substrate [9]. Twenty-six sccm dichlorosilane was used as Si source. The system pressure was maintained at 6 torr with a hydrogen flow of 3 slpm. Epitaxial layers were doped *in situ* using B_2H_6 and PH_3. Following a p^+ buffer layer grown at 1000 °C with a boron doping of 6×10^{19} cm^{-3}, an n-type Si channel (doping $1–5 \times 10^{18}$ cm^{-3}) was grown at 700 °C with undoped spacer layers on each side of the channel. In this work we used wide rather than ultrathin pillars, so the channel was doped in order to suppress punchthrough. Special steps were necessary to achieve a
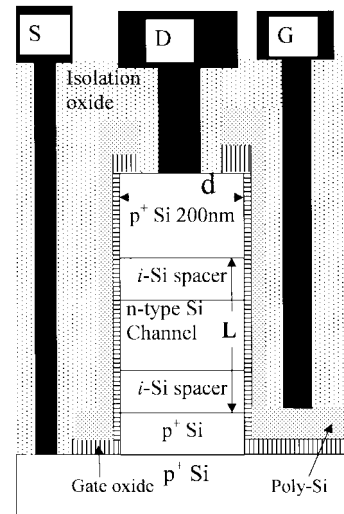
Fig. 1. Cross section of vertical p-channel MOSFET's with Si only (no SiGeC layers).
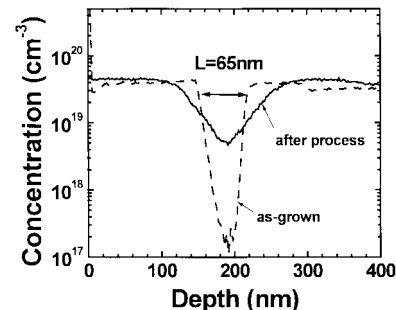

Fig. 2. SIMS profiles from as-grown samples (dashed line) and after wet oxidation at 750 °C and 700 °C poly-Si deposition (solid line) for structures with Si only (no SiGeC layers). The SIMS primary ion beam was Cs$^+$ with energy of 3 keV.

sharp phosphorous profile in the channel and will be discussed elsewhere. The channel length is defined as the epitaxial layer thickness between the two p^+ layers, with the edge of the p^+ profile defined as the point when the boron concentration [as measured by secondary ion mass spectroscopy (SIMS)] drops to $1/\sqrt{2}$ of its value in the heavily doped source/drain, multiplied by 1.1 to account for the fact that the side walls were not perfectly vertical. Fig. 2 gives SIMS profiles of boron in the as-grown p^+np^+ structures, which demonstrate the abrupt profiles before any further high temperature processes. The boron slopes are 8 and 12 nm/dec on upper and lower edges, respectively, and are limited by SIMS resolution. (The worse profile on lower interfaces is caused by the primary Cs$^+$ beam knocking in B atoms further into the substrate.) Vertical islands

were created by optical lithography and reactive ion etching. The island edges were aligned with the [011] and [01$\bar{1}$] crystal direction on the substrate. The slope of the walls was $\sim25°$ off from perfectly vertical.

Sacrificial and gate oxidations were performed at 750 °C in wet O_2 to give either a 6- or 10-nm sacrificial oxide followed by a 6- or 10-nm gate oxide. These oxide thickness and all others reported in our work were all measured on a planar (100) crystal Si control wafer oxidized simultaneously with the FET's. Higher oxide thickness are expected on the side walls, which have a nominal (110)-like surface orientation. (An oxidation rate enhancement of 60–80% has been reported on a (110) versus a (100) surface at 800 °C in dry O_2 for oxide thickness in the 6–10 nm range on (100) surfaces [10].) Because the Si islands in this work are large ($\sim50 \times 50$ μm^2), two-dimensional effects on the side walls (versus those in small pillars) can probably be neglected. The 200 nm p$^+$-polysilicon gates were deposited at 700 °C with *in situ* doping of 2×10^{21} cm^{-3} (from SIMS) giving a sheet resistance of 10 $\Omega/\square$. No gate depletion effects were observed in planar MOS capacitors using the same gates as a result of the high active doping concentration levels in the gates. The final process steps were poly-Si dry-etching and back-end processing.

III. DEVICE CHARACTERISTICS

Fig. 2 also gives the SIMS result from the same sample after all the high temperature processing. It shows that boron in the source and drain has diffused into channel, which limits the channel length in practice to $\gg$100 nm. Note in the literature vertical p-channel MOSFET's by a similar process were limited to $L > 130$ nm [7], [8], although a high pressure (10 bar) wet oxidation at low temperature (600 °C) was required to limit diffusion [8], [11]. For our process, devices with $L = 0.5$ μm are well behaved, but those with $L = 0.1$ μm (as grown) are shorted. Simulations showed most of this diffusion to be caused by the well known oxidation enhanced diffusion (OED) effect, in which injected interstitials greatly increase the diffusion of boron [12].

Previous work has shown that SiGeC can getter interstitial Si generated during gate oxidation or implantation, so that OED or TED effects both in SiGeC and in nearby Si can be suppressed [13], [14]. To use this principle for vertical MOSFET's, 20 nm $Si_{0.976}Ge_{0.2}C_{0.004}$ layers grown at 625 °C were sandwiched between the p$^+$ Si and the undoped spacers. Germane and methylsilane were used as the gas sources [15]. In addition to reducing the OED and TED effects, these layers also have the advantage that the boron diffusion coefficient in them is 80 times lower than in Si under the same N_2 annealing condition [16], [17]. The SIMS profiles after all the high temperature processing is shown in Fig. 3(a). The schematic structure is given in the inset. Note that in contrast to Fig. 2, the samples with SiGeC layers kept sharp boron profiles, so that it should be possible to reduce the channel length to under 50 nm. In the sample of Fig. 3(a), the SiGeC was not doped, so that it was part of the channel. To remove the uncertainties about the effects of SiGeC and oxides grown on SiGeC on the channel carrier transport, we then heavily doped the SiGeC layers. This insured the channel region exists entirely in Si, and still allowed the device to benefit from the reduction of boron diffusion in the SiGeC region and nearby.
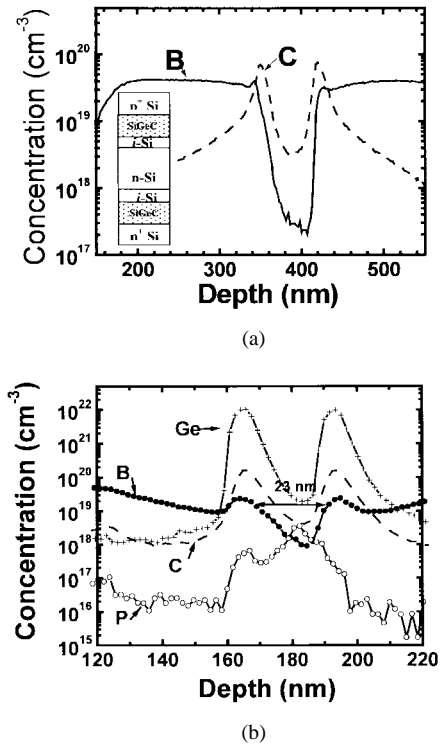

(a)

(b)

Fig. 3. (a) SIMS profiles for vertical p-channel MOSFET's with 20 nm undoped $Si_{0.976}Ge_{0.2}C_{0.004}$ epitaxial layers after the same high temperature process conditions as in Fig. 2. The mesa structure is shown in the inset. (b) SIMS profiles for a $L = 25$ nm device sample with highly B-doped SiGeC layers after all the high temperature processing.

Fig. 3(b) shows the SIMS profile in an actual $L = 25$ nm device sample after all the high temperature processing in which the SiGeC layers were doped.

Well-behaved drain currents and subthreshold $I–V$ curves for a transistor with channel length of 70 nm are given in Fig. 4. L was measured by SIMS (as defined earlier) after all high temperature processing. A transconductance of 100 mS/mm at $V_{DS} = -1.1$ V has been achieved with a 6 nm gate oxide on planar control wafer. Due to the high channel doping (2.5×10^{18} cm^{-3}), the subthreshold slopes are relatively large, 190 mV/dec. Longer channel length devices ($L = 0.1$ μm) with lower doping (0.9×10^{18} cm^{-3}) and the same gate oxide thickness had better slopes (88 mV/dec). To further scale the device, we also fabricated vertical p-channel MOSFET's with a 25-nm channel length. These devices suffered from the onset of punchthrough, but the gate still can control the drain current in the linear region (Fig. 5). Note the strained SiGeC has a bandgap 0.15 eV lower than Si, with most of the offset in the valence band [18]. It has been predicted that narrower bandgap in source region would help reduce the floating body effects [19], but their effect in present p-channel devices (low avalanche coefficient versus n-channel) and low drain voltage is uncertain. Carriers crossing the heavily-doped SiGeC/Si interface may suffer from series resistance. The total series resistance in our device is 25 Ω for $W = 200$ μm. It is not certain if it is due to the Si/SiGeC interface or spreading and contact resistance. Improvements of the subthreshold and punchthrough behavior will be expected using an ultrathin pillar to fully deplete an intrinsic channel region by surrounding gates.
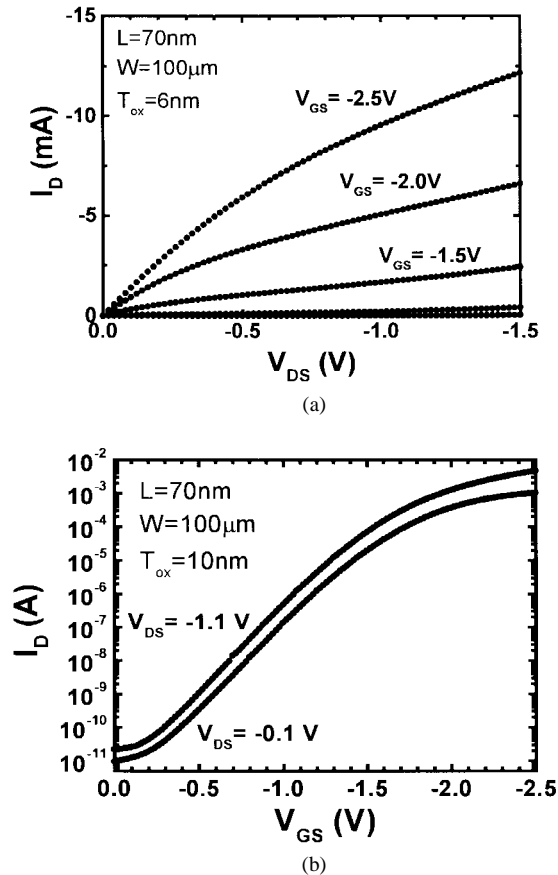
(a)

(b)

Fig. 4. (a) Output current–voltage (I–V) and (b) subthreshold drain current versus gate voltage characteristic for $L = 70$ nm. Gate oxide was 6 or 10 nm measured on planar Si surface.

(a)

(b)

Fig. 5. (a) Output I–V and (b) subthreshold drain current versus gate voltage for devices with $L = 25$ nm. Gate oxide was 10 nm measured on planar Si surface.

IV. SUMMARY

In summary, by introducing SiGeC diffusion barrier layers, for the first time boron dopant diffusion from source and drain into the channel region can be suppressed during the gate oxidation of vertical p-channel MOSFET's. Devices with a channel length down to 25 nm have been fabricated versus a previous state of art of 130 nm. Still better performance can be expected by using a surrounding gate structure with ultrathin pillars.

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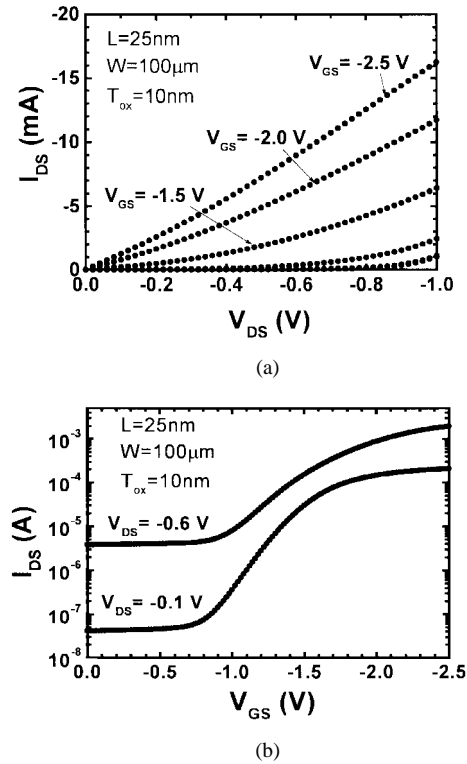[8] D. Behammer, L. Vescan, R. Loo, J. Moers, H. Mück, Lüth, and T. Grabolla, "Selectively grown vertical Si-pMOS transistor with short-channel lengths," *Electron. Lett.,* vol. 32, p. 406, 1996.
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