Thin-Film Transistors in Polycrystalline Silicon by Blanket and Local Source/Drain Hydrogen Plasma-Seeded Crystallization

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***Abstract*—Thin film n-channel transistors have been fabricated in polycrystalline silicon films crystallized using hydrogen plasma seeding, by using several processing techniques with 600 to 625 °C or 1000 °C as the maximum process temperature. The TFT's from hydrogen plasma-treated films with a maximum process temperature of 600 °C, have a linear field-effect mobility of ∼35 cm^2/Vs and an ON/OFF current ratio of ∼10^6, and TFT's with a maximum process temperature of 1000 °C, have a linear field-effect mobility of ∼100 cm^2/Vs and an ON/OFF current ratio of ∼10^7. A hydrogen plasma has also then been applied selectively in the source and drain regions to seed large crystal grains in the channel. Transistors made with this method with maximum temperature of 600 °C showed a nearly twofold improvement in mobility (72 versus 37 cm^2/Vs) over the unseeded devices at short channel lengths. The dominant factor in determining the field-effect mobility in all cases was the grain size of the polycrystalline silicon, and not the gate oxide growth/deposition conditions. Significant increases in mobility are observed when the grain size is in order of the channel length. However, the gate oxide plays an important role in determining the subthreshold slope and the leakage current.**

***Index Terms*—Crystallization, hydrogen plasma, polycrystalline silicon, thin-film transistors.**

I. Introduction

POLYCRYSTALLINE silicon (polysilicon) is widely used in active-matrix displays and in silicon-on-insulator technologies. Crystallization of amorphous silicon (*a*-Si), either as deposited or amorphized by ion implantation of as grown polysilicon, is an excellent precursor material for polysilicon films with large grain size and smooth surface [1]. Various techniques have been used to crystallize *a*-Si, namely solid phase crystallization (SPC) by annealing in a furnace [1] or a rapid thermal annealer [2] at temperatures in excess of 500 °C, laser induced crystallization [3], ion-beam or electron-beam induced crystallization [4] or zone melt recrystallization [5]. Of these techniques, SPC has the advantage of high reproducibility and control of the device quality of the polysilicon films and of surface roughness. Given the upper limit of ∼600 °C for processing on glass [6], the long anneal times (about 20 hrs or higher) at 600 °C [1] make the process unattractive for manufacturing. Various techniques have been employed to shorten the crystallization time, such as metal-induced crystallization [7] germanium-induced crystallization [8], and plasma treatments before the crystallization [9]–[11]. These plasma treatments include electron cyclotron resonance (ECR) plasma with oxygen, helium, or hydrogen at 400 °C [9], [11], and radio frequency (rf) hydrogen plasma at room temperature [10]. It has also been shown that rf or ECR hydrogen plasma treatment at the substrate temperature of 300 °C of hot-wire *a*-Si:H films reduces the threshold laser power for crystallization of the films [12].

Of these methods, the plasma-induced crystallization potentially introduces the least contamination to the films. An rf hydrogen plasma exposure at room temperature can significantly reduce the crystallization time compared to untreated films, and can be as short as 4 h at 600 °C, the lowest of the room temperature plasmas [10].

In this paper, we report the performance of thin film transistors (TFT's) fabricated in such polysilicon films crystallized from plasma-enhanced chemical vapor deposited (PECVD) *a*-Si:H using a room temperature rf hydrogen plasma treatment. TFT's with maximum process temperature of 600 °C and 1000 °C as function of channel length are compared. The hydrogen plasma treatment is also then locally applied to the source/drain region of the TFT's to seed the lateral crystallization into the channel region. The process leads to larger grains in the channel region and a twofold increase in the mobility at short channel length to ∼75 cm^2/Vs for process temperature of 600 °C.

Non self-aligned n-channel TFT's fabricated in polysilicon films crystallized after an ECR oxygen plasma treatment at 400 °C, with a maximum process temperature of 600 °C, has also been reported [11]. The process details were, however, not reported. The TFT's had a field-effect mobility of 35 cm^2/Vs and ON/OFF current ratio of ∼10^6, which are similar to the values in this work.

II. Precursor Silicon Film Deposition and Crystallization

The TFT's in this work were all fabricated in polysilicon films which were first deposited as hydrogenated amorphous silicon

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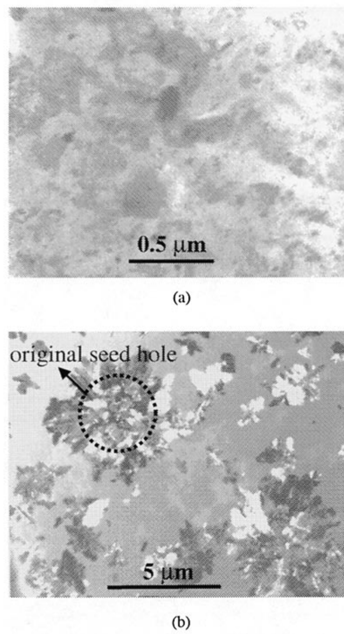


Fig. 1. Plan-view transmission electron micrograph of polysilcon films, (a) blanket hydrogen plasma treated and annealed with grain size of ~ 0.5 μm, and (b) laterally crystallized from seeded regions, showing grains up to 3 μm in size.

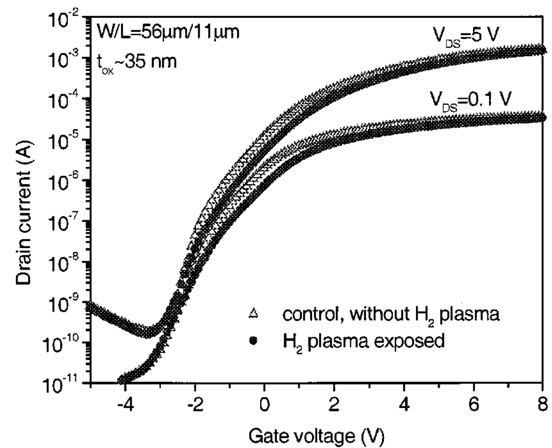


Fig. 2. Drain current versus gate voltage characteristics of high-temperature poly-Si TFT's made of films annealed at 600 °C with and without H_2 plasma treatment prior to anneal with thermal oxide grown at 1000 °C.

(a-Si:H) by PECVD at 150 or 250 °C using pure silane, at pressure of 500 mtorr and rf power density of ~0.02 W/cm^2. The substrates were either Corning 1737 or 7059 glass or silicon wafers coated with ~500 nm of SiO_2 deposited by PECVD at 250 °C, using SiH_4 and N_2O, pressure of 400 mtorr and rf power density of 0.1 W/cm^2. In experiments with blanket seeding, the films were then exposed to a room temperature RF hydrogen plasma for 1 h. Typical plasma conditions were; rf power density of 0.8 W/cm^2, pressure of 50 mtorr and flow rate of 50 sccm. Some films were not treated to plasma as controls. The samples were then crystallized by annealing at 600 or 625 °C in N_2 in a furnace. The exposure of an a-Si:H film to the hydrogen plasma leads to the formation of silicon crystal nuclei, which act as seeds during subsequent annealing [13]. The typical grain size for plasma treated or untreated control polycrystalline films as observed by TEM is ~0.5μm [Fig. 1(a)]. The grains of the completely crystallized polysilicon film are predominantly oriented in the [111] direction normal to the substrate surface, irrespective of prior treatment [13].

III. TFT Fabrication and Results

A. High-Temperature TFT's (≤1000 °C)

1) Fabrication: TFT's were first fabricated after the 600 °C crystallization anneal by a high-temperature process with thermally grown gate oxide. 150 nm of a-Si:H was deposited at substrate temperature of 150 °C on SiO_2 covered silicon substrates. A polysilicon top-gate self-aligned process was then used to make n-channel TFT's. The films were either not exposed to a plasma before crystallization (anneal time of 20 h) or exposed to a hydrogen plasma (anneal time 4 h) before crystallization [14]. During the plasma treatment, the samples were placed on a large silicon wafer to eliminate the aluminum contamination from the Al_2O_3 electrode [13]. After crystallization at 600 °C in N_2, device islands were patterned by dry etching with SF_6/CCl_2F_2 plasma at rf power density of 0.16 W/cm^2 and pressure of 100 mtorr. 35-nm dry oxide was grown at 1000 °C and then annealed in N_2 at the same temperature for ~20 min. The n$^+$ a-Si:H gate, ~250 nm thick, was deposited by PECVD at ~300 °C using SiH_4, PH_3 and H_2, at rf power density of ~0.02 W/cm^2, and pressure of 500 mtorr. The gate was then patterned by dry etching in SF_6/CCl_2F_2 plasma. The source and drain implant was phosphorus at 60 keV and dose of 2×10^{15} cm^{-2}. This was followed by implant anneal at 850 °C in N_2 for 30 min. As the last process step, an rf hydrogenation step was performed to passivate the grain boundaries in the polysilicon film [15] at 350 °C, at a rf power of 0.6 W/cm^2 for 60 min. This step was optimized to realize maximum field-effect mobility and minimum leakage current.

2) Results: In all cases, the field-effect mobility was calculated from the maximum value of the transconductance at $V_{\rm DS} = 0.1$ V. Effective channel length was used in the calculation, which was derived from difference between the drawn channel length and the x-intercept of the straight line fit to $1/I_{\rm DS}$ versus drawn channel length for fixed $[V_{\rm GS} - V_{\rm TH}]$. Hence, $L_{\rm effective} = L_{\rm drawn} - \Delta L$, where ΔL is the x-intercept. But as the field-effect mobility is not expected to be constant for all the channel lengths, the straight line fit is limited to $L_{\rm drawn} > 5$ μm and extrapolated to yield the effective channel length. The threshold voltage was deduced from the x-intercept of the straight line fit to $I_{\rm DS}$ vs. $V_{\rm GS}$ for $V_{\rm DS} = 0.1$ V. $I_{\rm OFF}$ is the minimum value of $I_{\rm DS}$ when $V_{\rm DS} = 5$ V, and $I_{\rm ON}$ is the maximum value of $I_{\rm DS}$ when $V_{\rm DS} = 5$ V. Fig. 2 shows typical TFT characteristics, which were similar and well behaved for devices in films both with and without the hydrogen plasma treatment, with no significant difference between two kinds of devices. The threshold voltage was ~0.1 V, the subthreshold slope was ~0.5 V/decade and the ON/OFF current ratio was in excess of 10^7, for both the control and the hydrogen-plasma-treated samples.

Within experimental error, the control and hydrogen plasma samples had similar linear region field-effect mobilities. They were ~75 cm^2/Vs at long channel length, but rose up to ~100

TABLE I
PROCESS CONDITIONS AND TFT RESULTS FOR DEVICES FABRICATED WITH BLANKET PLASMA TREATMENT, WITH MAXIMUM PROCESS TEMPERATURE OF 600 °C. EXCEPT FOR DEVICES 4 AND 10, THE CRYSTALLIZATION TIMES ARE THE MINIMUM REQUIRED TO SATURATE THE CHANGE IN UV REFLECTANCE (MEASURE OF DEGREE OF CRYSTALLIZATION)

Sample No.	*a*-Si:H growth temp(°C)	Plasma pre-treatment		Anneal at 600 °C (h)	Gate oxide		TFT characteristics (L_{eff} ~ 3.5 μm)			
		Type	On Si wafer		Temp (°C)	Anneal in O_2	μ_{linear} cm^2/Vs	V_{TH} (V)	S (V/dec)	I_{ON}/I_{OFF}
Standard deviation of the data							± 1.5	± 0.3	± 0.2	2x
1	150	-	-	20	250	No	38	0.8	1.6	10^6
2	150	H_2	Yes	4	250	No	33	-7.5	1.7	10^6
3	150	H_2	Yes	20	250	No	33	0.8	1.4	10^6
4	150	-	-	60	250	No	37	-6	2.4	10^6
5	250	-	-	12	350	Yes	42	0.2	2.6	$2x10^5$
6	250	O_2	No	8	350	Yes	38	3.4	1.4	$4x10^5$
7	250	H_2	No	5	350	Yes	35	3.2	1.6	$7x10^5$
8	250	-	-	12	250	No	30	0.1	2.0	$3x10^5$
9	250	H_2	Yes	5	250	No	24	-7	1.8	$5x10^5$
10	250	H_2	Yes	8	250	No	24	-0.8	1.6	$5x10^5$

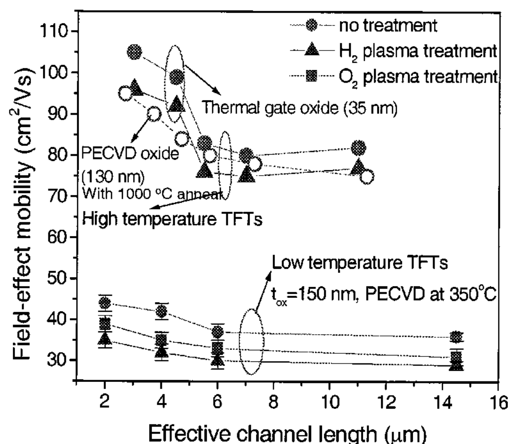


Fig. 3. Field-effect mobility of high-temperature TFT's as a function of channel length, for untreated (with thermal oxide and PECVD oxide) and plasma-treated films.

cm^2/Vs at channel length of ~2 μm (Fig. 3). An increase in mobility at short channel lengths in polysilicon TFT's has been observed by others [16], [17]. It has been attributed to grain sizes on the order of a channel length, leading to large portion of the channel with no grain boundaries obstructing the motion of electrons from the source to the drain. Thus, our results imply a grain size of few microns, much larger than the as-crystallized film. The apparent increase in grain size over that after the 600 °C crystallization, might result from a grain ripening effect during the high-temperature oxidation and the ion implantation anneal steps, during which the grains oriented in the minimum energy configuration grow at the expense of others [18]. High temperature processing might also result in the annealing of the structural defects within the grains of the polysilicon [19], leading to improved performance of the TFT's.

B. Low-Temperature TFT's (≤600 °C)

1) Fabrication: N-channel TFT's were fabricated by a standard self-aligned top-gate process, similar to that for the high-temperature TFT's, except for the low process temperature [14]. Table I lists the different process conditions for different samples. After the films were completely crystallized at 600 °C, the active area was defined by dry etching and ~150 nm gate oxide was deposited by PECVD at either 350 °C or 250 °C, using 35 sccm of SiH_4, 160 sccm of N_2O, at a pressure of 400 mtorr and rf power of 0.1 W/cm^2. The gate oxide was then annealed for ~2 h in O_2 at 600 °C in some cases. A few samples had gate oxide deposited by magnetron PECVD at 250 °C. Rest of the processing is similar to that of the high-temperature TFT's discussed in the previous section. However, the source/drain anneal was done at 600 °C to limit the maximum processing temperature.

2) Results: Well-behaved characteristics were obtained in all cases, as can be seen from Table I. Typical characteristics of drain current versus gate voltage and versus drain voltage are shown in Fig. 4(a) and (b), respectively, for a device in a film treated with a hydrogen plasma before and a 4-h 600 °C crystallization step (sample 7 in Table I). Typical results are mobilities in the range of 30 to 40 cm^2/Vs, subthreshold slopes from 1 to 2 V/decade, and ON/OFF current ratios from 10^5 to 10^6. In the subsequent sections, the effects of annealing time and plasma treatment, the effect of growth temperature of the precursor *a*-Si:H film, and the effect of the gate oxide on device performance will be examined.

a) Effect of Hydrogen Plasma Treatment and Anneal Time: The hydrogen plasma treatment resulted in any slight reduction of field-effect mobility of the TFT from ~38 cm^2/Vs for the untreated sample (sample 1, Table I) to ~33 cm^2/Vs for the hydrogen plasma-treated sample (samples 2, Table I). The subthreshold slope was ~1.7 V/decade and the ON/OFF current ratio was ~10^6 for both the hydrogen plasma-treated and untreated samples. But threshold voltages were not the same, with the hydrogen plasma-treated sample having a threshold voltage of −7.5 V compared to 0.8 V in case of the untreated control sample. As in the case of the high-temperature TFT's, the samples were placed on a Si wafer during the hydrogen plasma-seeding step to minimize the aluminum contamination in the films, hence the threshold voltage shift is not due to aluminum sputter effect.

To ensure that the field-effect mobility in the case of the hydrogen-plasma-treated sample was not smaller due to the

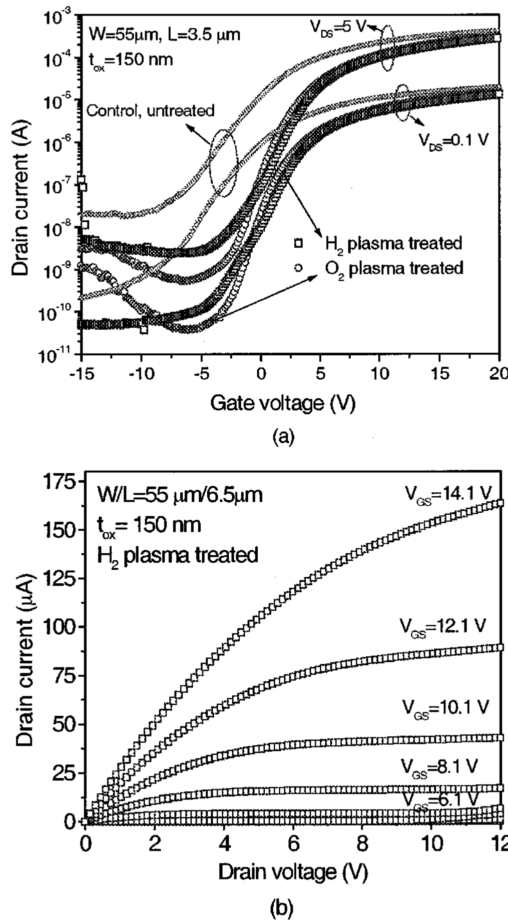


Fig. 4. (a) Drain current versus gate voltage, and (b) drain current versus drain voltage for TFT's in polysilcon films with and without plasma treatment prior to anneal (samples 5, 6, and 7).

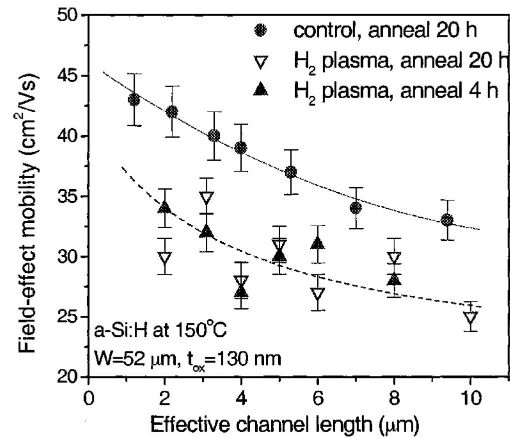


Fig. 5. Field-effect mobility of polysilicon TFT's in hydrogen-plasma-treated films annealed for 4 h and 20 h (samples 2 and 3), and control untreated film annealed for 20 h (sample 1) at 600 °C, for different channel lengths.

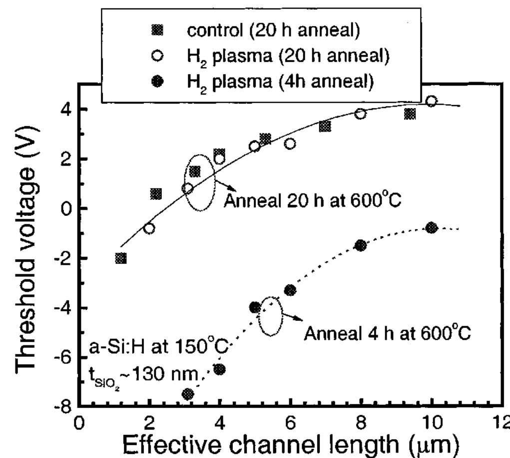


Fig. 6. Threshold voltage of polysilicon TFT's in hydrogen-plasma-treated films annealed for 4 h and 20 h (samples 2 and 3) and control untreated film annealed for 20 h (sample 1) at 600 °C, for different channel lengths.

shorter anneal time and to discern the effect of anneal time on threshold voltage, transistors were also fabricated in films annealed at 600 °C in N_2 for various anneal times. Samples 2 and 3 were hydrogen-plasma-treated before and annealed for 4 h and for 20 h at 600 °C, respectively. Samples 1 and 4 were untreated and annealed later for a total of 20 h and 60 h at 600 °C, respectively. All the samples were placed on a 5″ Si wafer during the hydrogen plasma treatment to reduce the effect of aluminum sputtering onto the sample [13]. The gate insulator in this case was PECVD SiO_2 deposited at 250 °C. The field-effect mobility of the transistors from hydrogen-plasma-treated films (2 and 3) was independent of the annealing time (Fig. 5), with both samples having a mobility of ~30 cm²/Vs. A similar effect was observed for the TFT's from control untreated films (1 and 4). The very long anneal in the case of sample 4 (~20 h crystallization anneal and ~45 h implant damage anneal after the ion implantation step at 600 °C) also did not result in any change in field-effect mobility (Table I). On the other hand, the threshold voltage did depend strongly on the annealing time for the hydrogen-plasma-treated samples, with the V_{TH} for the long-channel TFT's increasing from -1 V to 4 V ($L > 10\ \mu$m) when the annealing time increased from 4 h to 20 h (Fig. 6). But the threshold voltages for samples 1 and 3, which were both annealed for 20 h, are nearly the same (Fig. 6). This indicates that the plasma treatment, with the sample placed on a Si wafer during exposure, itself does not affect the threshold voltage (V_{TH}) of the TFT's, and that V_{TH} depends strongly on the annealing time of the films for the same gate oxide. All the *a*-Si:H films deposited by PECVD have a high oxygen content of $3–4 \times 10^{18}$ cm^{-3} (as measured by SIMS) [13] and even at the crystallization temperature of 600 °C, enough oxygen related thermal donors might be created to dope the polysilicon films slightly n-type [20]. This would lead to negative threshold voltages making it difficult to turn the transistors off. Long annealing might reduce the doping effect of the oxygen in the film due to dissolution of the thermal donors [20], [21], and hence change the TFT's characteristics from normally ON to normally OFF. The fairly high negative threshold voltage in the case of sample 4 (-6 V) might be due to dopant diffusion into the channel region during the long implant (~45 h at 600 °C) damage anneal. This could lead to the channel being doped slightly n-type and hence result in large negative threshold voltage.

The field-effect mobility of the low-temperature TFT's in polysilicon films with or without plasma treatment did not

change appreciably as the channel length was reduced (Figs. 3 and 5). This suggests that the grain sizes are much less than 2 μm, (which was the smallest channel length) as was confirmed by TEM measurement.

b) Aluminum Sputter Effect on V_{TH}: Some of the plasma treated samples (samples 5 and 6) show higher threshold voltages of ~3 V than the 0.2 V for the sample without the plasma treatment (sample 7). We believe that the higher threshold voltage is a result of the sputtering of aluminum from the aluminum oxide coated electrode on to the sample during the plasma exposure, which we found to dope the channel region p-type ($N_{\mathrm{Al}} \sim 5 \times 10^{18}$ cm^{-3} as measured by SIMS [13], [14]). Placing the samples on a Si wafer during the plasma treatment reduced the aluminum contamination effect, and the TFT's made in these films did not show the positive threshold voltage shift.

c) Effect of Growth Temperature of Original a-Si:H and of Gate Oxide: The field-effect mobility of the TFT's from control untreated films (samples 1 and 8) was reduced to ~30 cm^2/Vs from ~38 cm^2/Vs for channel length of 3.5 μm, when the growth temperature of the original *a*-Si:H film was changed from 150 °C to 250 °C (Table I). As the growth temperature for *a*-Si:H is lowered, the hydrogen content in the film is increased and the crystallization time increases [13], suggesting that the grain sizes are larger [22]. A similar trend was seen for the hydrogen-plasma-treated samples, in which the field-effect mobility reduced to ~24 cm^2/Vs from ~33 cm^2/Vs for channel length of 3.5 μm (samples 2 and 9) when the growth temperature was raised from 150 °C to 250 °C (Table I). There was no significant change in threshold voltage in either case.

Various gate oxides were evaluated: a 250 °C PECVD oxide, a 350 °C PECVD oxide some of which were annealed in O_2 at 600 °C, and a 250 °C magnetron sputtered oxide. The highest field-effect mobilities and best subthreshold slopes in both unseeded and plasma-seeded samples were with the 350 °C/600 °C-oxygen-anneal oxide. All the PECVD oxides had high interface-state densities of ~10^{12} cm^{-2} eV^{-1}, as deduced from *C–V* measurement of MOS capacitors on crystalline Si substrates. However, this was not thought to limit the mobility of the low-temperature TFT's. This was because the field-effect mobility of the transistors with a 1000 °C anneal after the 600 °C crystallization anneal and PECVD oxide was ~75 cm^2/Vs versus ~82 cm^2/Vs for the TFT's with thermal gate oxide grown at 1000 °C at long channel lengths (Fig. 3).

C. Laterally Seeded Low-Temperature TFT's

1) Selective Crystallization: Our aim is to increase the mobility in polycrystalline silicon low-temperature ($\leq$600 °C) transistors by increasing grain sizes, within a reasonable thermal budget. A large grain size can be achieved by a very high-temperature anneal (~1000 °C), after the polysilicon is first formed, so that the large grains grow at the expense of the small leading to an overall increase in grain sizes [18] and mobility in the 1000 °C process vs. the 600 °C process. An alternative is the lateral grain growth of polysilicon from the source and drain regions into the adjacent *a*-Si:H channel region to directly form large grain polysilicon in the channel at 600 °C. This technique involves selective seeding by hydrogen plasma treatment of the source and drain regions masked by the gate. Note that other groups have done similar lateral crystallization using metals like Ni [7], or germanium [16], or patterned light absorption masks [17].

Selective crystallization with plasma seeding can be done by masking the plasma with an oxide [11], [13]. 100 nm of SiO_2 was deposited by electron-beam evaporation on top of 150 nm of *a*-Si:H film deposited at 150 °C. The SiO_2 was then patterned and the samples were exposed to hydrogen plasma. Then all the remaining SiO_2 was stripped and the samples were annealed in the furnace for ~4 h at 600 °C. The exposed areas crystallized completely as expected, while the unexposed areas remain amorphous [13]. The amorphous/polycrystalline difference of the two regions was also confirmed by UV reflectance measurements. Note that the size of the crystalline area increases with time. This shows that the crystalline/amorphous interface front moves out of the seeded areas to the unexposed areas, with the lateral crystalline growth rate being ~0.5μm/h at 600 °C [13]. The lack of crystalline grain nucleation in the unexposed area, which is a result of the higher activation energy for nucleation than the activation energy of crystal growth, leads to larger silicon grains in the lateral growth area than in the plasma seeded areas. This was confirmed by plan-view transmission electron microscopy (TEM) measurements of the films, which shows that the lateral grain growth from seeded regions results in grains as large as ~3μm [Fig. 1(b)]. The grains in the seeded regions themselves, as in case of the blanket crystallization, are only ~0.5μm in size [Fig. 1(a)]. The TEM sample preparation involved chemically etching a hole in the substrate to realize an electron-transparent film at the edge of the hole. The chemical etchant used was pure HF for glass substrates, and a mixture of HF, HNO_3 and CH_3COOH for Si substrates. In this case, the TEM samples were prepared in films deposited on glass substrates, as HF etches only glass and does not etch the polysilicon film. On the other hand, the silicon etchant also etches the polysilicon thin film during the overetch time, hence damaging the film. Further work is in progress to prepare TEM samples in polysilicon films on SiO_2/Si substrates using a dimpler and an ion-milling machine to avoid etching of the polysilicon film, so that grain size of polysilicon films after a high-temperature anneal can be measured.

2) Laterally Seeded TFT Fabrication: We used the hydrogen-plasma seeding technique to fabricate laterally seeded TFT's with higher mobility. The source/drain regions were used as the seeded regions to promote lateral crystal growth in the channel. No additional lithography steps were required because the patterned gate was used as the mask for the hydrogen plasma seeding treatment. The transistors were fabricated using a 150 nm *a*-Si:H layer deposited at a substrate temperature of 150 °C. The active islands were then patterned by dry etching in SF_6/CCl_2F_2 plasma. The gate insulator used was PECVD SiO_2 deposited at a substrate temperature of 250 °C. Note that the gate oxide is deposited on *a*-Si:H and the crystallization anneal is done with the gate oxide covering the channel regions. This is in contrast to the low-temperature TFT's discussed in Section III.B where, the gate oxide was deposited after the amorphous film was completely crystallized.

TABLE II
LATERALLY SEEDED LOW-TEMPERATURE TFT CHARACTERISTICS FOR VARIOUS GROWTH, ANNEAL, AND PROCESS CONDITIONS. ALL TFT'S HAD 250 °C PECVD OXIDE EXCEPT FOR SAMPLES 15 AND 16. THE COLUMN, "AFTER ION IMPLANTATION" REFERS TO WHETHER THE H_2 SEEDING TREATMENT AND LATERAL CRYSTALLIZATION WAS DONE BEFORE OR AFTER THE S&D ION IMPLANTATION STEP

S. No.	*a*-Si:H growth temp (°C)	Plasma pre-treatment		If Magnetron PECVD Oxide	Anneal temp(°C)/ time (h)	TFT characteristics (L_{eff} ~ 2 μm)			
		Seeding	After ion implant			μ_{linear} cm²/Vs	V_{TH} (V)	S (V/dec)	I_{ON}/I_{OFF}
Standard deviation of data						± 3	± 0.5	± 0.2	2x
11	150	Yes	Yes	No	600/20	72	-4	1.6	10^7
12	150	No	Yes	No	600/20	37	-4	1.7	$2x10^6$
13	150	Yes	Yes	No	625/5	68	-4	1.6	10^7
14	150	No	Yes	No	625/5	30	-4	1.7	$3x10^6$
15	150	Yes	Yes	Yes	600/20	50	2.4	1.5	$3x10^6$
16	150	Yes	Yes	Yes	600/60	48	2.3	1.6	10^6
17	150	Yes	No	No	600/25	44	-5	2.0	$4x10^6$
18	150	No	No	No	600/25	32	-5	2.4	$8x10^5$
19	250	Yes	Yes	No	600/12	28	-2	2.6	10^4
20	250	No	Yes	No	600/12	27	-1.5	2.6	10^4

A 250 nm of phosphorus doped *a*-Si:H was then grown for the gate. After patterning the gate, the samples were implanted with phosphorus to form the source and drain contacts. A few samples were then exposed to hydrogen plasma (seeded) to create seed nuclei in the exposed source and drain and gate electrode regions and annealed at 600 °C and 625 °C along with unseeded control samples. Both the crystallization and the implant anneal were done simultaneously. The anneal time was chosen such that the channel region of the longest channel (∼15 μm) TFT's and the n^+ *a*-Si:H gate was completely crystallized, considering the crystal growth velocity is ∼0.5μm/h at 600 °C [13]. The hydrogen plasma seeding improved TFT performance, and also reduced the crystallization time for the crystallization of the phosphorus doped gate [13]. Transistors were also fabricated with the lateral crystallization anneal of the channel done prior to the ion implantation step. This involved two 600 °C steps, one to crystallize the channel and another to anneal the implant damage, and therefore a higher thermal budget.

3) Laterally Seeded TFT Results: Table II lists the characteristics of the laterally seeded TFT's under various process conditions, with the measurement conditions being the same as those mentioned in Section III-A. The transistors (sample 11 and 12) showed excellent characteristics as can be seen in Fig. 7 with ON/OFF current ratios of $\sim 10^7$ and subthreshold slopes of about 1.7 V/decade. The threshold voltages of the TFT's decreases as the channel length is reduced due to the short channel effect as discussed. The dopant diffusion during the long anneal (∼20 h at 600 °C) could lead to shorter effective channel length and therefore lead to an apparent increase in field-effect mobility as deduced from the drawn channel length. Therefore, the effective channel length was calculated as described previously in Section III-A. The ΔL values are nearly the same (∼0.3μm) for both the seeded and the unseeded TFT's [Fig. 8(a) and (b)].

The mobility of the transistor for different channel lengths is shown in Fig. 9. At long channel lengths, the field-effect mobilities are ∼37 cm²/Vs, slightly higher than in the unseeded process. Not known if significant. At short channel lengths, <5μm, the control devices show negligible change in mobility, but the laterally seeded devices show a large increase in mobility up to ∼72 cm²/Vs. This is attributed to the larger grain

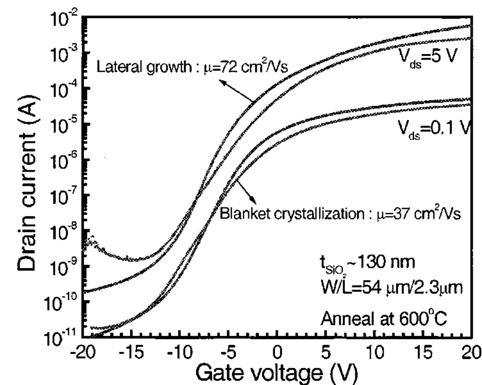


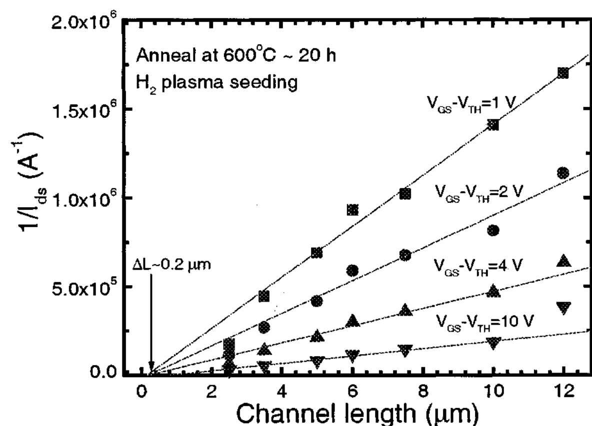
Fig. 7. Drain current versus gate voltage of the seeded and unseeded control poly-Si TFT's (sample 11 and 12) with maximum processing temperature of 600 °C.

size in the channel region of the laterally seeded transistor. The negligible change in mobility as channel length is reduced in the control devices means that, the effective grain size is much smaller than the smallest channel length (2 μm) as seen in Section III-B. (Note that when the device size is on the order of the grain size, the performance may be subject to statistical variations due to statistical variations in grain distribution, as in conventional polysilicon devices.)

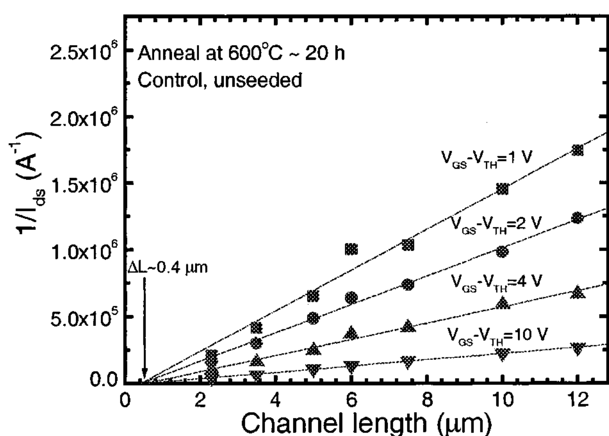
The leakage current of the laterally seeded TFT's is ∼3 pA/μm compared to ∼35 pA/μm for the unseeded control devices. The large grains in case of the laterally seeded devices leads to fewer grain boundaries in the channel region, and hence fewer number of trap states, and therefore led to lower leakage current. This dependence of leakage current of polysilicon TFT's on the grain size of the polysilicon has also been reported elsewhere [23].

In the subsequent section, the effects of crystallization anneal temperature and length of anneal, effect of lateral crystallization done before or after the ion implantation step, and the effect of the growth temperature of the precursor *a*-Si:H film. The process conditions to realize optimum laterally seeded transistor performance will then become clear.

4) Effect of Annealing Temperature and Time, and Lateral Crystallization Before Ion Implantation: We also studied the



(a)



(b)

Fig. 8. Plot of $1/I_{\rm DS}$ as a function drawn channel length for various values of $|V_{\rm GS} - V_{\rm TH}|$ to extract the effective channel length for (a) the laterally seeded TFT's, and (b) unseeded, control TFT's. Note the straight line is fitted for the longer channel lengths as the method implicitly assumes fixed field-effect mobility.

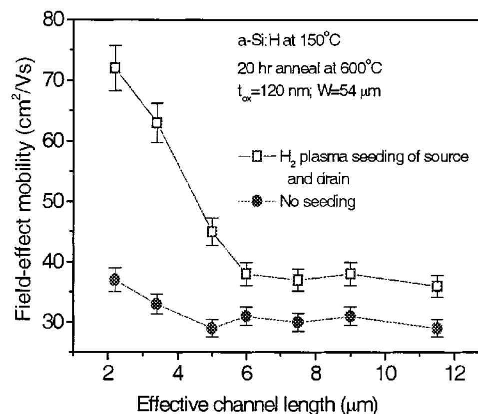


Fig. 9. Field-effect mobility calculated at $V_{\rm DS} = 0.1$ V as a function of effective channel length in the seeded and unseeded TFT's. The crystallization temperature was 600 °C.

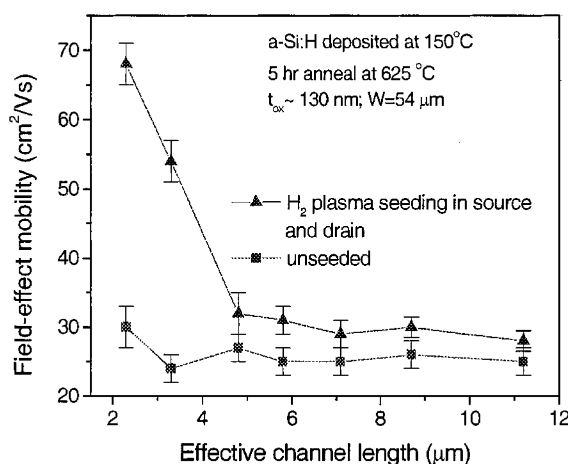


Fig. 10. Linear regime mobility calculated at $V_{\rm DS} = 0.1$ V as a function of channel length in seeded and unseeded TFT's. The crystallization temperature was 625 °C.

effect of annealing temperature (samples 13 and 14 versus 11 and 12) on the grain size and hence on the electron mobility. The annealing temperature was changed to 625 °C, from the 600 °C used in the previous experiments. We found that the time taken to crystallize was reduced, but that the mobility became smaller in the control samples (sample 14), probably because of an increase in nucleation density leading to smaller grains [1]. Fig. 10 shows the linear field-effect mobilities in the seeded and the unseeded transistors (13 and 14) sample with the crystallization temperature of 625 °C. The mobility in the control sample is ~25 cm^2/Vs when annealed at 625 °C, compared to ~35 cm^2/Vs when annealed at 600 °C. But the seeded TFT's have nearly the same mobility irrespective of the annealing temperature. The advantage of using higher temperature (625 °C vsersus 600 °C) is that the annealing time is reduced but the disadvantage is that one has to use more expensive glass substrates (for display applications) with higher strain point temperatures [6].

A few of the samples were also annealed for longer times up to 60 h at 600 °C (sample 16). These samples had gate oxide deposited by magnetron PECVD at 250 °C. The longer anneal did not result in any significant change in any of the TFT's characteristics, in fact the mobility of the TFT's reduced slightly to ~48 cm^2/Vs compared to ~50 cm^2/Vs for the sample annealed for 20 h at 600 °C (sample 15 versus 16). The laterally seeded TFT annealed for 20 h at 600 °C had mobility of ~50 cm^2/Vs when the gate oxide was deposited by magnetron PECVD, compared to ~72 cm^2/Vs for the laterally seeded TFT with regular PECVD oxide. This reduction in mobility was also seen in case of the TFT's made in blanket-crystallized films discussed in Section III.B. Both the laterally seeded and control TFT's, with the magnetron oxide have fairly high threshold voltages of ~2.5 V irrespective of the annealing time, while the TFT's with the PECVD oxide (sample 11) have fairly negative threshold voltage of −4 V at $L = 2$ μm. The subthreshold slope of the laterally seeded TFT's was ~1.6 V/decade, and was nearly the same for both magnetron PECVD or regular PECVD oxide.

The effect of crystallization anneal before ion implantation (samples 17 and 18) on the performance of the TFT's was examined. In addition to increasing the number of annealing steps, this also resulted in a reduction in the mobility of the seeded transistor to ~44 cm^2/Vs at a channel length of ~2 μm compared to ~72 cm^2/Vs in the single-step anneal (sample

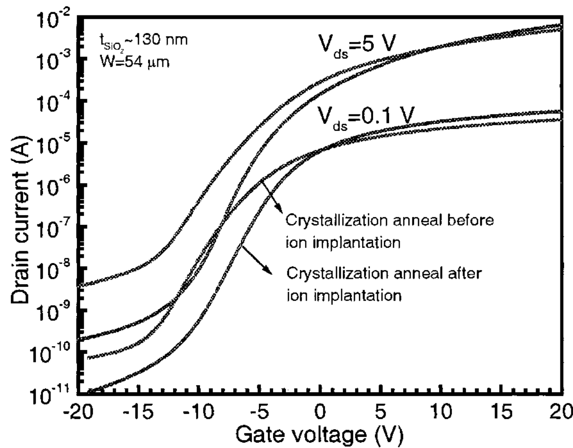


Fig. 11. Drain current versus gate voltage of laterally seeded TFT's with lateral crystallization done before and after the ion implantation step (sample 17 and 11).

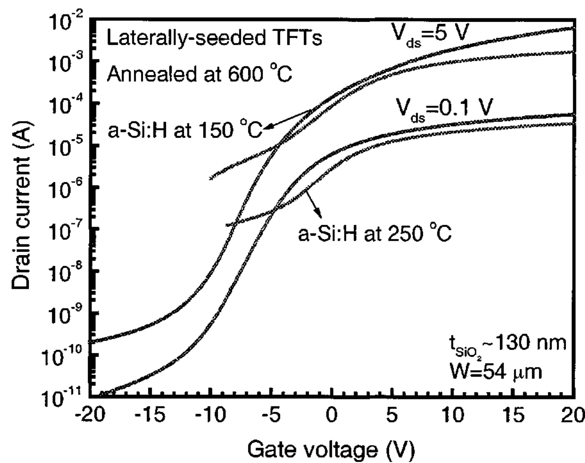


Fig. 12. Drain current versus drain voltage for the laterally seeded TFT's from crystallization at 600 °C of *a*-Si:H films deposited at 250 °C and 150 °C (sample 19 and 11).

17 versus 11), for annealing at 600 °C. The leakage current was also higher with the ON/OFF current ratio being $\sim 10^6$ for TFT's with lateral crystallization anneal done before the ion implantation, compared to $\sim 10^7$ for the single-step anneal TFT's (Fig. 11). The source/drain ion implantation amorphizes the exposed regions. But its effect on the preexisting crystalline grains in the channel during the subsequent implant damage anneal is not clear.

5) Effect of Growth Temperature of a-Si:H: The deposition temperature of the precursor *a*-Si:H film also affects the performance of the laterally seeded TFT's (Fig. 12). When the growth temperature of the *a*-Si:H film was changed to 250 °C (samples 19 and 20) from 150 °C (samples 11 and 12), the amount of hydrogen in the film was reduced and the incubation time for thermal generation of seed nuclei also dropped [13], [23]. During the crystallization after the hydrogen-plasma seeding in the exposed source and drain regions, spontaneous nucleation might occur in the unexposed channel regions before the lateral crystal growth from the seeded regions can crystallize the whole channel. Therefore, the grain size in the channel region may not be enhanced. This was indeed the case, and the field-effect mobility of the TFT's was $\sim$28 cm^2/Vs for both the laterally seeded sample and the unseeded control sample for all channel lengths (Fig. 12). Hence, the deposition temperature of the precursor *a*-Si:H film has to be chosen such that, the incubation time for nucleation of seeds is the longest, for the lateral seeding to work effectively.

IV. Conclusion

TFT's with excellent characteristics with both high and low thermal budgets have been fabricated in polycrystalline silicon films which was crystallized from *a*-Si:H using a hydrogen plasma seeding technique. The method is very attractive for high performance circuits on large-area glass substrates. The hydrogen plasma enhanced crystallization effect can be controlled spatially by masking, resulting in polycrystalline silicon and amorphous silicon areas on the same substrate. Selective seeding by hydrogen plasma treatment can also be applied to growing crystal grains laterally from the seeded regions into the unexposed regions. This produces large grains in the lateral growth region. We have fabricated high mobility poly-Si TFT's with mobilities as high as 75 cm^2/Vs at a maximum process temperature of 600 °C, utilizing this lateral crystallization effect without laser processing.

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