performance of devices does not have a clear dependence on the work functions of the cathode metals, and air-stable Ag is found useful for building efficient devices with **performance comparable to devices using reactive Mg:Ag alloys.**

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Chapter 6

Integration Issues in Organic LED Displays

6.1 Direct Integration of Multiple Color OLEDs

6.1.1 Introduction

A long sought goal in the display field has been the integration of light emitting devices (LEDs) of three different colors onto a single substrate. While OLEDs have shown extreme versatility in terms of colors and freedom of substrates in recent years, the integration of OLEDs of different colors has proven difficult because of difficulties associated with the processing and patterning of the organic materials or reactive metal contacts. Therefore most of the multicolor display work to date in this field has been based on fabricating a single type of emitter with an external color control scheme. As such, the fabrication of organic emitters is the final process step and no further patterning and processing of organic devices are needed. These methods include: (i) integrating organic white emitters with pixelated red, green and blue color filters [1], (ii) integrating organic blue emitters with pixelated red and green down-conversion materials [2,3], (iii) adjusting the emission of a single type of broad-band organic emitter by integrating with pixelated microcavities [4].

There are several concerns for the above methods. For method (i), the color filters throw away at least two thirds of light. For method (ii), a down-conversion materials even

with 100% conversion efficiency still leads to a loss of power efficiency, and the reported quantum efficiencies for the down-conversion are only ~50% and ~30% for green and red, respectively The use of very efficient down-conversion materials will also cause the reduction of contrast in a bright environment by absorbing and re-emitting the background

For method (iii), the cavity has a direction-dependent resonance frequency which in turn causes angular color variation. Also, the microcavity changes the angular distribution of emission intensity away from the nearly ideal Lambertian emission, leading to variation of luminance (brightness) with viewing angle. Both of these will cause a viewing-angle problem and compromise the general advantage of OLEDs.

To take full advantage of OLEDs and reach maximum power efficiency for an organic display, the integration of individually optimized red, green and blue devices onto a common substrate is a clearly desirable alternative The integration structure can be either (i) vertically stacked red, green and blue emitters [5,6] or (ii) laterally patterned red, green and blue emitters. The stacked OLEDs make use of the transparency of organic materials used in OLEDs and transparent (or semitransparent) contacts [5,6]. To apply them in a matrix-addressing array, both methods require pixelation engineering. The pixelation for both structures may be achieved without post-OLED patterning in small-molecule OLEDs by utilizing pre-OLED patterned structures on the substrates and some features of vacuum deposition (e.g. shadowing effects [7], oblique deposition [8] etc.` For polymer-based OLEDs, patterning of films cannot be avoided in integrating OLEDs

with different polymer layers, mainly because the polymer films are continuous by the way they are coated The patterning of films inevitably requires the use of solvents, acid or water. The direct exposure of organic materials to solvents and water can lead to the degradation or even complete failure of devices. In the first part of this chapter, we demonstrate a way to integrate three different polymer-based OLEDs on a same substrate, with each consisting of a different organic layer for a different color.

6.1.2 Structures and Processing for Direct Integration of Polymer OLEDs

In virtually all polymeric OLEDs to date only the top metal contact or the bottom ITO contact has been patterned to define the area of the device, not the organic layer. Fig. 6.1(a) shows one such structure The integration of devices with different organic layers onto a common ITO layer would involve patterning the organic layers as well. A straightforward integration approach is to sequentially fabricate different sets of devices by preparing the metal contact on each organic layer and then patterning the organic layer to form a patterned device before processing with the next layer of organic materials. The final desired structure of such an approach is shown in Fig. 6.1(b), but does not answer the question of how to successfully pattern the organic film. This approach leaves the organic layer exposed on the device edge, where it may be attacked by water, solvents etc during later processing. For example, in the integration of polymer-based devices, the spin-coating of a second polymer after the completed fabrication of a first device, e.g. the leftmost device in Fig. 6.1(b), would lead to degradation of the existing device, because the solvent carrier in the second spin-coating step would dissolve the first polymer through the device sidewall. With such an approach, we indeed observed irregular shorting, leakage and degradation of existing devices caused by the attack of solvents through the unprotected device sidewalls, though macroscopically the devices still looked the same.

To overcome this problem, we then rendered the exposed edge of the device electrically inert using a second structure as shown in Fig. 6.1(c). In this structure, a thin insulating layer is deposited on top of the ITO and the active device regions are defined by opening windows on the insulating layer to access the ITO. The use of the insulating layer allows the top metal contacts to extend out of the active areas and leave some distance (e.g. ~1 mm) between the edge of the metal coverage and the actual electrically active region, due to the high intrinsic resistance of the organic film This strategy successfully kept the active regions intact in any following polymer coating and leaves the device characteristics unchanged, as will be shown later. The devices work well in dry nitrogen

Polymer

ITO

Al
Ag
Mg:Ag
Polymer
ITO
Glass
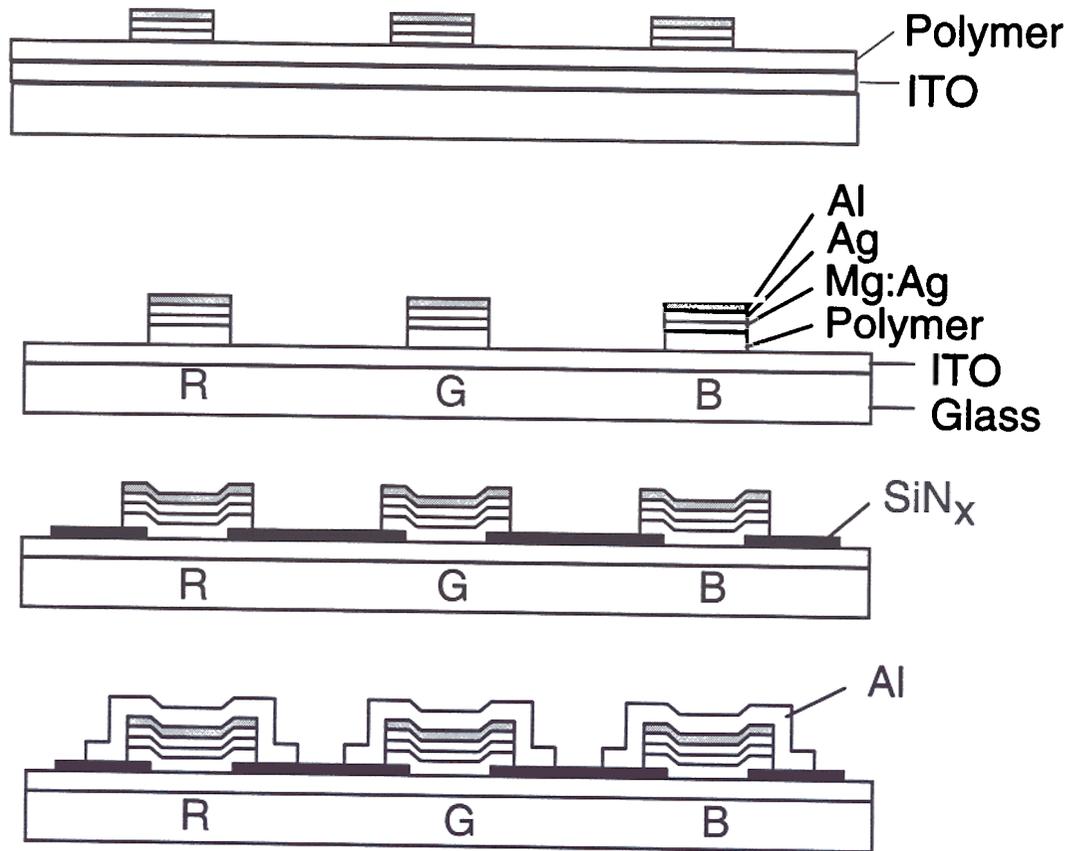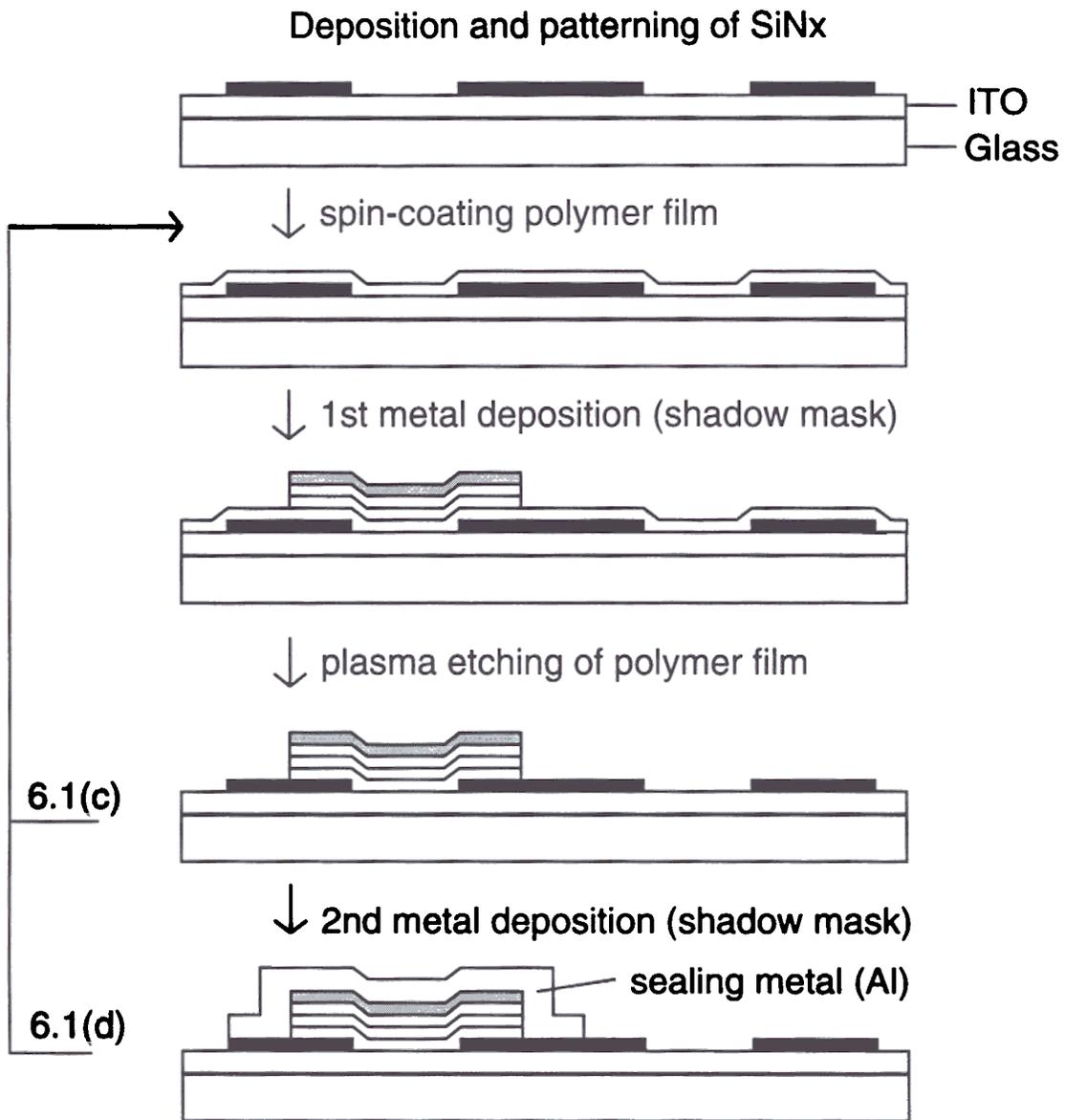
R   G   B

SiN$_x$

R   G   B

Al

R   G   B

Fig. 6.1: Cross sections of (a) conventional OLED structure and of three integration schemes: (b) a straightforward integration scheme with only the patterning of organic films. (c) an integration scheme with a patterned insulator on the ITO. The sizes of the active regions and the metal contacts are 2mm × 2mm and 4mm × 4mm, respectively.(d) an integration scheme with a patterned insulator on the ITO and a metal sealing layer over each device.

Deposition and patterning of SiNx

— ITO
— Glass

↓ spin-coating polymer film

↓ 1st metal deposition (shadow mask)

↓ plasma etching of polymer film

6.1(c)

↓ 2nd metal deposition (shadow mask)

sealing metal (Al)

6.1(d)

Fig. 6.2: Processing flowchart for the integration structure in **Fig. 6.1(c)** and **Fig. 6.1(d)**

atmosphere, but to prevent any possible attack of the organic materials by air, moisture or processing liquids through the edge of the device, a refined structure as shown in Fig 6.1(d) has also been fabricated. After the etching of each polymer thin film and before the coating of the next polymer, a thick layer of air-stable metal, like Al in our case, is deposited to seal the whole device. Note that except for the difference in ways of organic deposition, all the above schemes can in principle be applied to OLEDs based on molecular organic materials.

The details of processing are now described in the following and are illustrated in Fig. 6.2:

    clean the ITO/glass substrate as described in Chapter 3.

    A thin layer of insulating silicon nitride SiN_x of ~1000 Å is deposited on top of cleaned ITO by plasma-enhanced chemical vapor deposition (PECVD) at 250 °C.

(3)   The active device windows in the SiN_x are then patterned by photolithography and standard CF_4 reactive ion etching (RIE).

(4)   Remove the photoresist and clean the substrate again

(5)   Oxygen plasma treatment of exposed ITO for OLEDs

(6)   The polymer thin film for the first set of devices, which are orange in this case, is then spin-coated to cover the whole surface.

(7)   After spin-coating, the top metal contacts for the first set of devices are thermally evaporated through a shadow mask. The metal contact has three layers in a stack, with ~500 Å Mg:Ag alloy overcoated by ~500 Å silver and ~1000 Å aluminum. Al is used because of its stability in the following oxygen plasma process.

(8)   The structure is then exposed to an oxygen plasma (4 minutes for ~1000-Å-thick doped polymer thin films, which etches away photoresist and organics where exposed, but does not etch the aluminum layer or any layers underneath. Therefore, this plasma etching is self-aligned and does not need an extra mask. Also, the use of dry etching avoids the risk of excessive exposure of the organic films to solvents in

the case of wet etching. ITO exposed by this oxygen plasma etching is found to be clean and proper enough for the next set of OLEDs, and there is no need for further solvent wet cleaning, which is desired to avoid. This oxygen plasma process has therefore dual functions: etching organic thin films and preparing the ITO surface for the next set of OLEDs.

(9) If the structure of Fig. 6.1(d) is applied, the evaporation of the aluminum sealing layer for the first set of devices is then performed through another shadow mask before the spin-coating of the polymer film for the next set of green devices.

(10) The steps from step (6) to step (8) or (9) are then repeated to finish the integration of devices.

In semiconductor processing, oxygen plasma has long been a useful tool for etching organics or removing organic residues from surfaces, such as stripping photoresist or etching polyimides, etc. Using oxygen plasma to pattern organic layers in OLEDs and its effect on OLEDs has never been reported, to our best knowledge. The oxygen plasma treatment or etching for this integration experiment was carried out in a small barrel-type oxygen plasma etcher (Plasmod, March Corp.). The estimated plasma conditions on the Plasmod reactor are ~300 mtorr (base pressure ~180 mtorr), flow rate ~50-60 sccm, ≤100 W. ~1000-Å-thick doped polymer thin films of any compositions used in this experiment were fully etched in 3-4 minutes. The etching rate is therefore ~300 Å/min. In some of the blends, ~30 wt.% of Alq was dispersed into the polymer PVK. Since the aluminum oxide is not volatile, how the Al atoms in these thin films are removed in the oxygen plasma is not fully understood. One possible route we can imagine is that Alq molecules are broken to form smaller volatile compounds through the interaction with the oxygen plasma and some of these compounds contain the Al atoms.

In the above processing, the patterning of all metal layers is carried out by mechanical alignment of shadow masks for metal evaporation for our array of 2mm ×

157

2mm devices Eventually, to make a high resolution display containing a large array of small devices of at most several hundred μm, the patterning of metal layers by photolithography and etching will probably be needed instead of by shadow masks.

6.1.3 Results and Discussions

The orange, green and blue OLEDs used in this work are composed of PVK/Alq/nile red (100:40:0.2 by wt.), PVK/Alq/coumarin 6 (100:40:1 by wt.) and PVK/PBD/coumarin 47 (100:40:1 by wt.), respectively. The electroluminescence spectra of the three devices are shown in Fig. 6.3(a). I-V characteristics of discrete devices on separate substrates are shown in Fig. 6.3(b), along with the brightness vs. voltage characteristics (L-V). The external quantum efficiencies were 0.7%, 0.5% and 0.5% photon/electron for orange, green and blue, respectively.

The effect of integration processing on devices was checked by comparing the characteristics of devices when they were just freshly made to those of the same devices after they underwent the integration processing steps. Because most OLEDs fabricated use continuous organic layers, we first test if the patterning of organic layers by plasma etching would affect the device characteristics. Fig. 6.4 compares the L-V and I-V curves of a same blue device in the structure of Fig. 6.1(a) and Fig. 6.1(b) with a continuous and patterned organic layer through just one single oxygen plasma etching step. There is hardly any change of the device characteristics in I-V or light emission, indicating that these organic devices can sustain the plasma etching The lack of change in the device characteristics also suggests that the current is confined in the cathode contact area in devices with an unpatterned organic layer, that the fringing current flows outside of the contact area is negligible, and that the plasma process does not induce edge leakage current in such a mesa structure.

Fig. 6.5 compares the L-V and I-V curves of an orange device in the structure of Fig. 6.1(c) before and after the integration processing, which in this case means two spin-
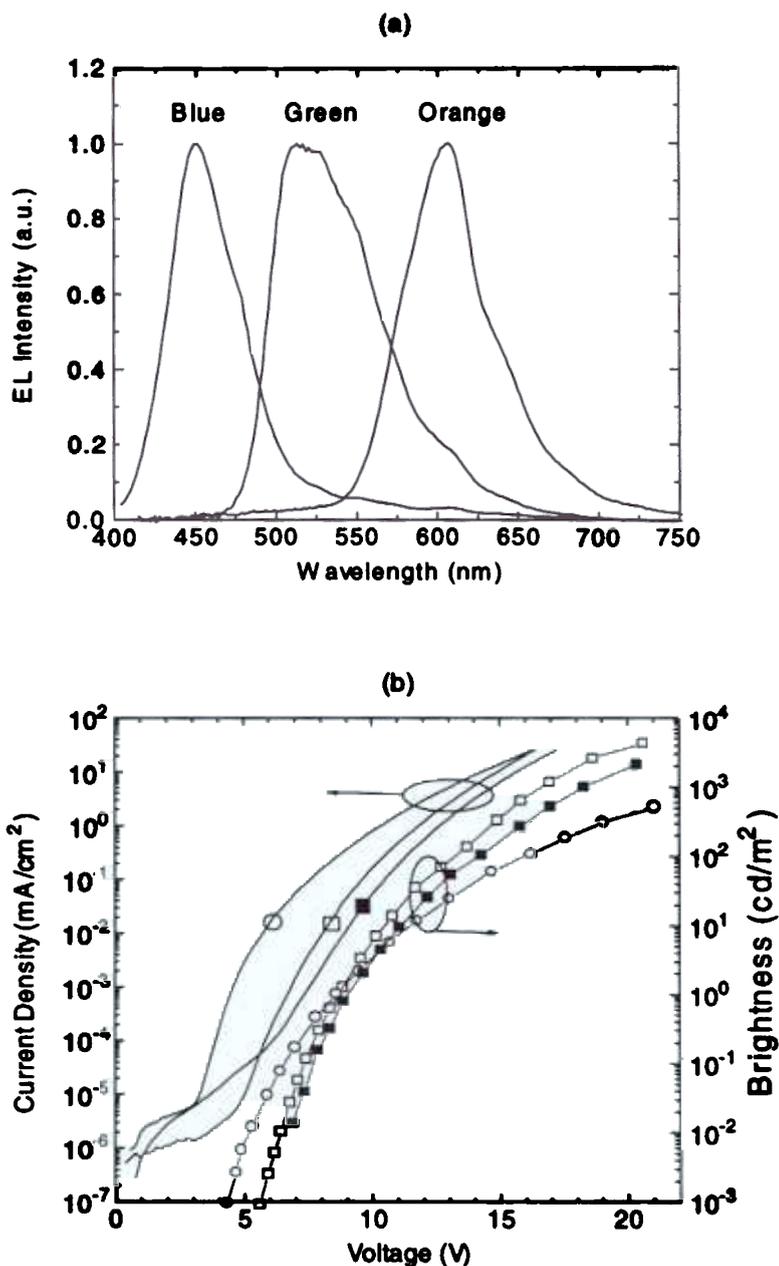
Fig. 6.3: (a) EL spectra and (b) forward current-voltage and brightness-voltage characteristics of the orange (open square), green (solid square) and blue (open circle) devices. The compositions of the orange, green and blue LEDs are ITO/PVK:AlQ:nile red (100:40:0.2 wt.)/Mg:Ag, ITO/PVK:AlQ:coumarin 6 (100:40:1.0 wt.)/Mg:Ag, and ITO/PVK:PBD:coumarin 47 (100:40:1.0 wt.)/Mg:Ag, respectively. Typical organic film thicknesses are ca. 1000-1100 Å.
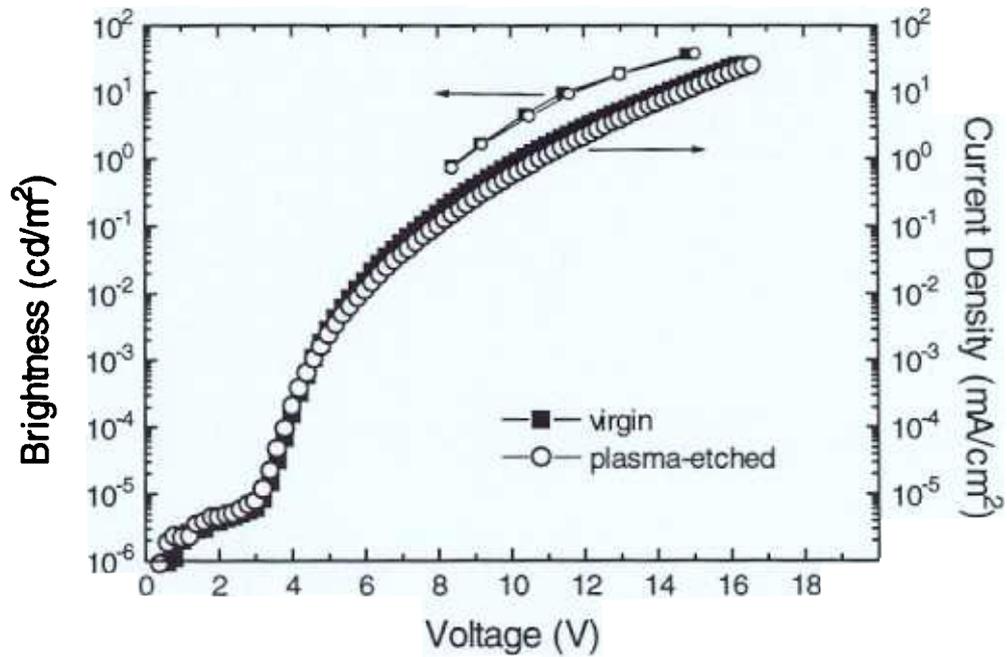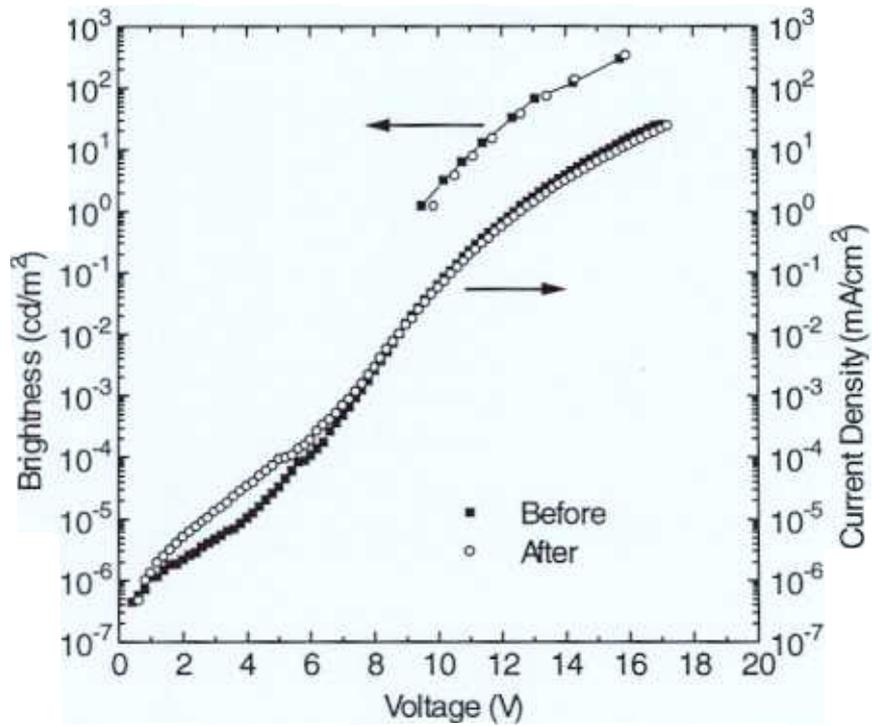
159

Fig. 6.4: L-V and I-V curves of the same blue device in the structure of **Fig. 6.1(a)** and **Fig. 6.1(b)** with a continuous and patterned organic layer through just one single oxygen plasma etching step.

Fig. 6.5:Brightness-voltage and current-voltage characteristics of the same orange device in the structure of **Fig. 6.1(c)** before (solid square) and after (open circle) integration processing.

coating steps and two oxygen plasma etching steps. The device characteristics are unchanged after integration processing, as seen in Fig. 6.5, and are virtually identical to those of discrete devices as shown in Fig. 6.3.

Fig. 6.6(a) shows the photograph of OLEDs in the structure of Fig. 6.1(c). It was taken after the devices were removed from the glove box and were left in the air for ~3 hours. Damage was observed around the outside edge of the extended metal layer. Because such damage was not observed for the same devices in the nitrogen atmosphere, it was presumably caused by the reaction of Mg with the air permeating through the attacked polymer region. In contrast, we did not observe such damage under the same condition for the OLEDs in the structure of Fig. 6.1(d), whose photograph is shown in Fig. 6.6(b). The metal sealing layer in the structure of Fig. 6.1(d) has therefore successfully protected the polymer layer from the attack of the solvent. In the present experiment, the EL efficiencies of the OLEDs with the structure of Fig. 6.1(d) is ~40% lower than those of the OLEDs with the structure of Fig. 6.1(c). It is because the ~1000Å thick PECVD SiN_x used in the present devices is leaky. It conducts a current comparable to the OLED current between the sealing metal and the ITO. Using a thicker or better insulator should eliminate this problem. Finally, a color photograph of the integrated orange, green and blue devices with the structure of Fig. 6.1(d), all operating simultaneously in the air, is shown in Fig. 6.7.

6.1.4 Future Work

In summary, by combining photolithography, shadow masking and plasma dry etching, we have demonstrated the integration of individual polymer-based OLEDs with different organic layers onto a single substrate. Although it can be used for low-resolution, multicolor indicator applications, these devices are still large and widely separated, not readily suitable for high-resolution display applications. The shadow mask alignment for the cathode contacts and protective sealing metal layers is the main obstacle

162
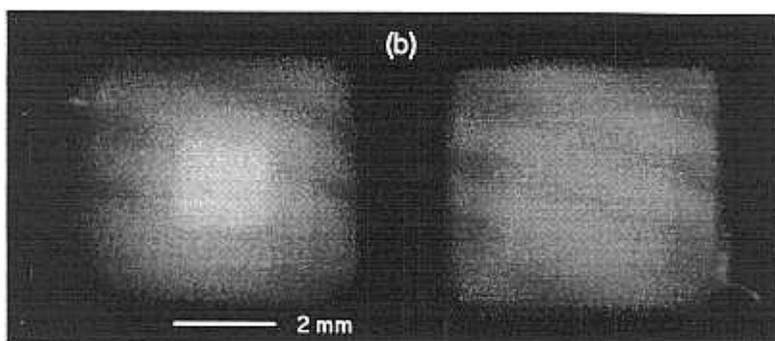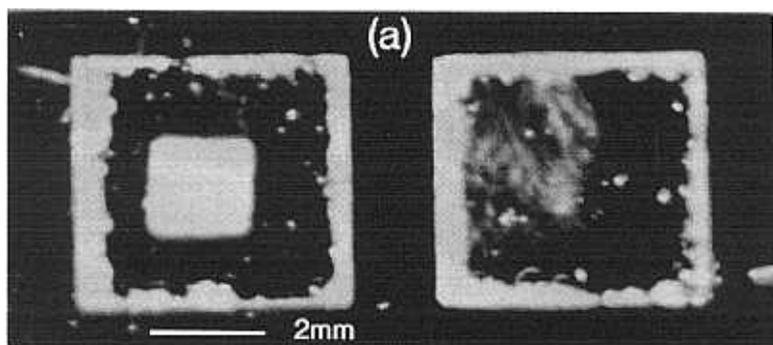
Fig. 6.6: (a) Photograph of OLEDs in the structure of **Fig. 6.1(c)**. (b) Photograph of OLEDs in the structure of **Fig. 6.1(d)**. Both were taken after they were removed from the dry glove box and were left in the air for ~3 hours. OLEDs on the left side in both photographs were turned on. Note the damage around the outside edge of the extended metal layer in (a).
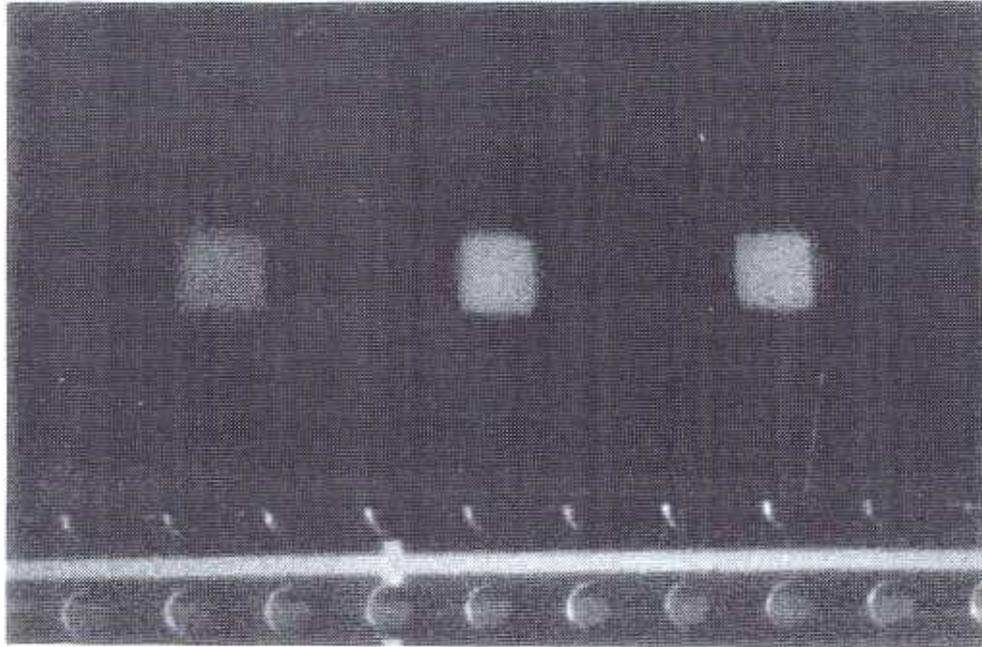
Fig. 6.7: Photograph of working integrated orange, green and blue devices. The approximate brightnesses were 60, 100, 100 and cd/m^2 for the blue, green and orange devices, respectively.

for using the same technique to make ~100 μm devices. Using photolithography and acid wet etching for the patterning of top metal layers, however either degrades the metal layers when reactive metals, such as Mg, are used, or degrades the organic layers even when only stable metals are used. Fig. 6.8(a) and Fig. 6.8(b) show examples for either case. Fig. 6.8(a) is the picture of patterned Al/Ag/Mg:Ag stripes on the glass substrate by acid (aqua regia) wet etching. Apparently, Mg was attacked by water in the acid and worm-like damage was seen in the picture. Fig. 6.8(b) is the picture of patterned Al stripes on a PVK thin film spun-cast on a glass substrate. "Cracks" of the PVK film and "bubbles" below the Al film occuring during the wet etching of Al were observed. It is obvious that the direct exposure of reactive metals or organic thin films to processing liquids causes degradation and is detrimental to devices. Therefore, further scaling down of directly integrated devices and the patterning of top cathode layers might require the combination of photolithography, dry etching of metal layers and refined device structures.

6.2 Integration of OLEDs and TFTs on Thin Steel Foils

6.2.1 Passive Matrix OLED Displays

Since the OLED technology is a thin-film technology with reasonable performance, the application of OLEDs for flat panel displays has been considered. For simple, low-information-content, alphanumerical displays, each OLED element can be independently controlled by a driving circuit. For a high-information-content, dot-matrix display, a dedicated driver for each pixel is impossible and therefore multiplexing of drivers and addressing of pixels are needed. The OLED pixel arrays can be driven either by (i) a passive matrix addressing scheme or (ii) an active matrix addressing scheme.

The schematic circuit diagram of a passive matrix OLED display (PMOLEDs) is shown in Fig. 6.9(b), with each pixel represented by a diode. The PMOLEDs can be simply implemented by sandwiching the organic layers between the crossed anode and
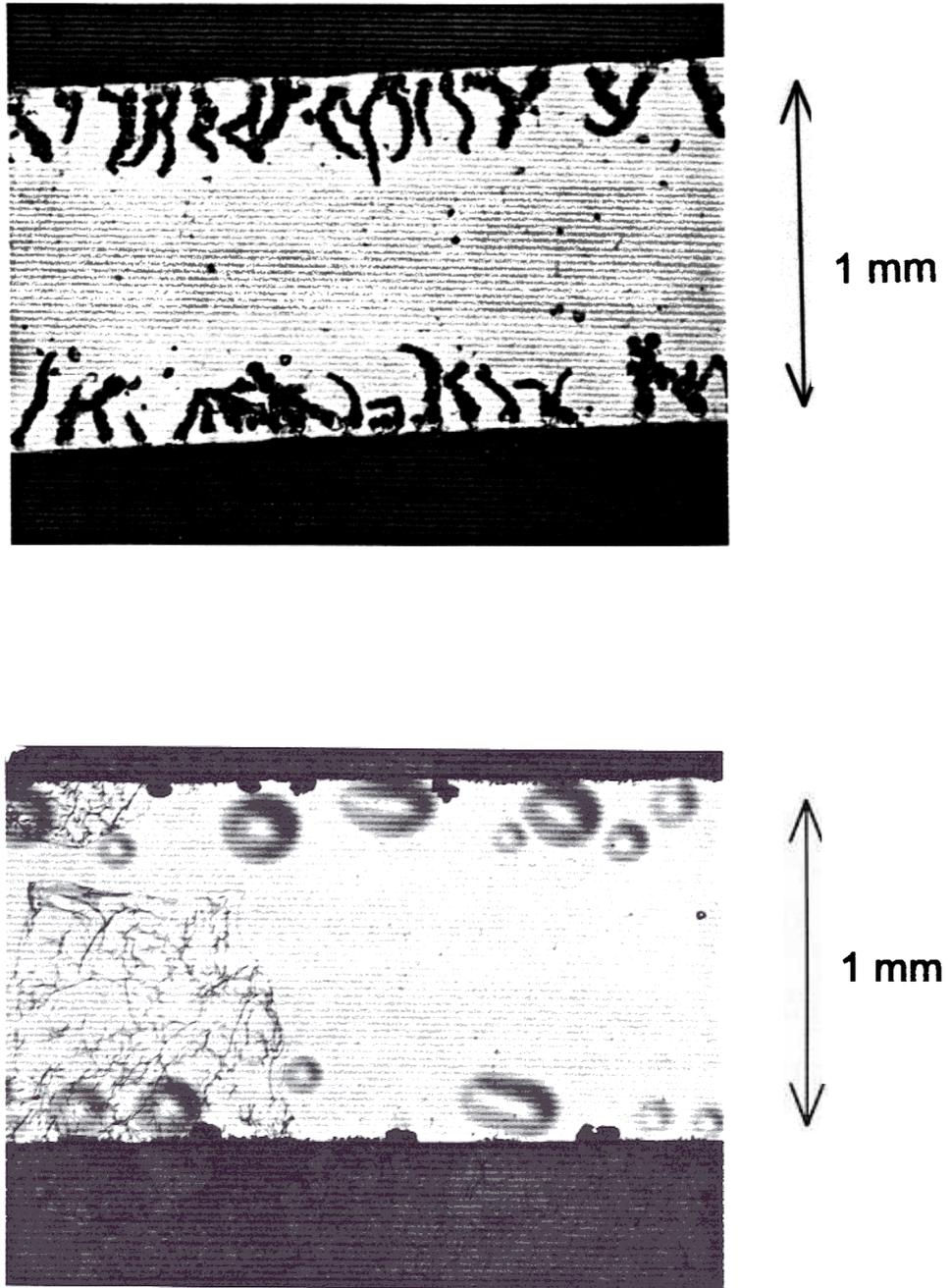
Fig. 6.8: Photographs of (a) patterned Al/Ag/Mg:Ag stripes on the glass substrate by acid (aqua regia) wet etching. and of (b) patterned Al stripes (by aqua regia) on a PVK thin film spun-cast on a glass substrate.
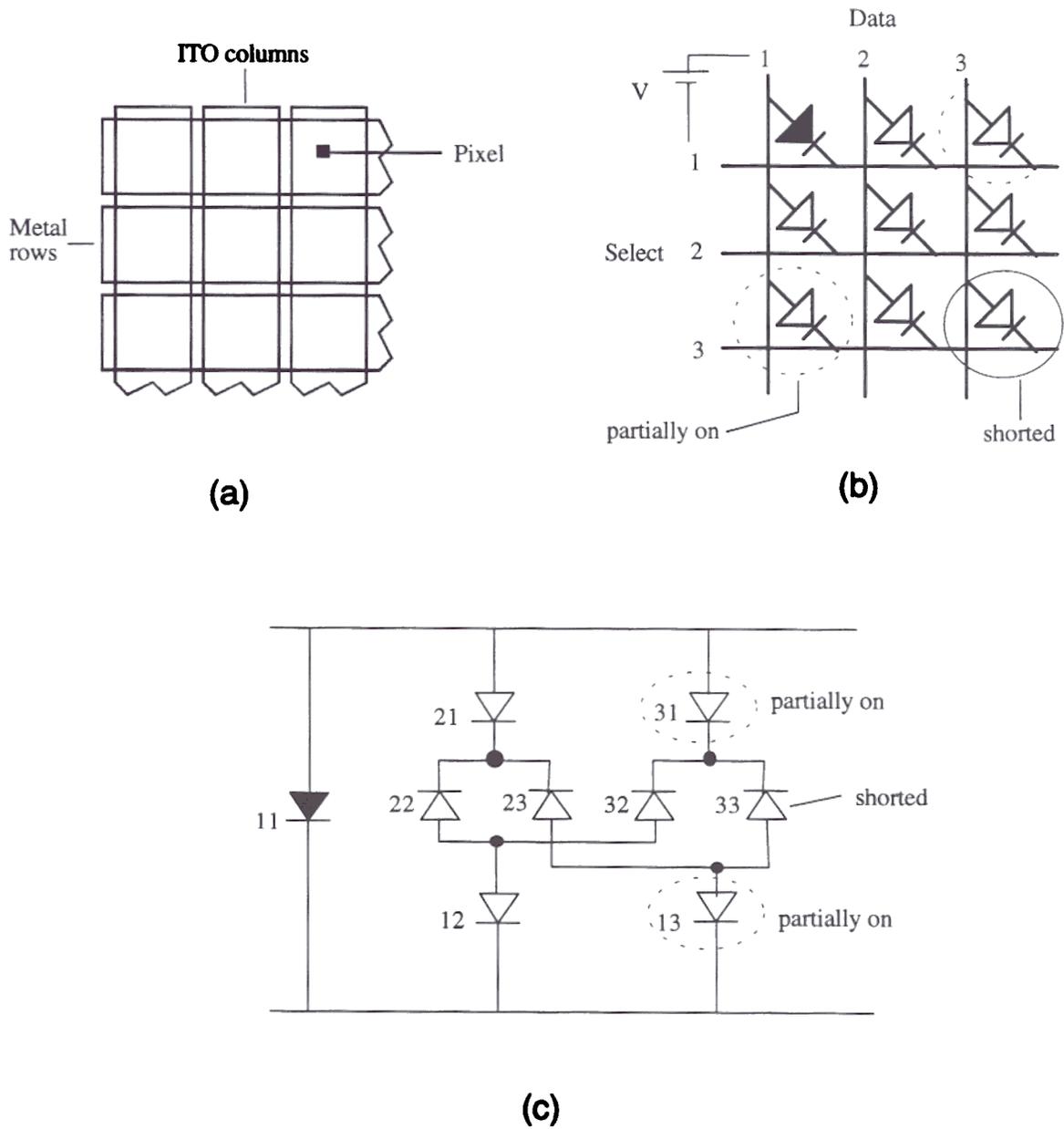
Fig. 6.9: (a) Configuration and (b) schematic circuit diagram of the passive matrix OLED array. (c) Equivalent circuit of (b) to illustrate the cross-talk of OLEDs in the array.

cathode contact stripes, as shown in Fig. 6.9(a). In a standard passive matrix driving scheme, the rows are scanned sequentially with a frame rate $\geq$50Hz and the data signals are presented at the column electrodes. For a display with N rows, a pixel in the array is at most driven for 1/N of the time. Since the OLEDs do not have a memory effect and are off unless they are driven, to achieve an average brightness of 100 cd/m^2, then each OLED has to be driven at N$\times$100 cd/m^2. With 1% EL efficiency, a high current density of several hundred mA/cm^2, corresponding to hundreds of μA for a 300 μm $\times$ 300 μm pixel, will be needed to achieve such a peak brightness. Besides the reliability issues of running OLEDs under such a harsh condition, there are several other considerations when high driving currents are used to produce high peak brightnesses. These include: (i) the drop of the OLED luminous efficiency at high brightness levels, as discussed and shown in Chapter 4 (section 4.4, Fig. 4.17), (ii) the maximum brightness that an OLED can achieve under duty-cycled driving conditions, and (iii) the voltage drop on the electrode lines.

Since the drive voltage at very high brightness levels could be double the drive voltage at 100 cd/m^2, the luminous efficiency can drop by over 50%. The maximum brightness that an OLED can achieve directly limits the number of row lines and therefore the physical size or the resolution of a passive-matrix OLED display. We now further analyze (iii), the voltage drop on the electrode lines as follows. Consider an OLED array with $N_r \times N_c$ pixels, a negligibly small gap between pixels and a pixel size of $L_c \times L_r$, where N_r and N_c are the numbers of row lines and column lines, and L_c and L_r are the column line width and the row line width, respectively. The sheet resistances of the column and row lines are R_c and R_r, respectively. Under a dc driving condition, the current density required to achieve a certain brightness B_0 for an OLED pixel is J_0. Then, under the passive matrix addressing scheme and the average brightness B_0 (all OLEDs fully on with a peak brightness of $N_r \times B_0$ in the row dwell time in the worst case), P_c, the time-average power consumption on column lines with all OLEDs on and P_r, the time-average power

consumption on row lines with all OLEDs on, can be (approximately) expressed as follows:

$$P_c = \frac{N_c}{N_r} \sum_{i=1}^{N_r} (N_r J_0 \times L_c L_r)^2 (R_c \frac{L_r}{L_c} \times i)$$

$$(J_0 L_c L_r)^2 (R_c \frac{L_r}{L_c}) \frac{N_c N_r^2 (N_r + 1)}{2}$$

$$P_r = \sum_{i=1}^{N_c} (R_r \frac{L_c}{L_r})[(N_r J_0 \times L_c L_r)(N_c - i + 1)]^2$$

$$= (J_0 L_c L_r)^2 (R_r \frac{L_c}{L_r}) \frac{N_r^2 N_c (N_c + 1)(2N_c + 1)}{6}$$

With the voltage drop V_{LED} on the OLEDs (at the brightness of $N_r \times B_0$), the time-average power consumption on OLEDs, P_{LED} is:

$$P_{LED} = (N_r J_0 \times L_c L_r) \times V_{LED} \times N_c \qquad (6.3)$$

The P_c-to-P_{LED} and P_r-to-P_{LED} ratios are:

$$\frac{P_c}{P_{LED}} \approx \frac{\frac{1}{2}(J_0 \times L_c L_r)(R_c \frac{L_r}{L_c})N_r^2}{V_{LED}} \equiv \frac{V_c}{}$$

$$\frac{P_r}{P_{LED}} \approx \frac{\frac{1}{3}(J_0 \times L_c L_r)(R_r \frac{L_c}{L_r})(N_r N_c^2)}{V_{LED}} \equiv \frac{V_r}{}$$

where V_c and V_r are defined as the average voltage drop across the column line and the average voltage drop across the row line. When compared to the OLED voltage, they give the ratio between the power consumption on the electrode lines and the power consumption on the OLEDs. In the OLED structure, at least one electrode is a transparent conductor, which usually has a rather high sheet resistance of a few tens of Ω

169

/square for practical thicknesses. Metal electrodes of a few thousand Å have a sheet resistance of 0.1 Ω/square or even lower. Since the currents from all columns flow into a same row line, the total row current becomes very large as N_c is large. In addition, from the equation 6.5 and 6.6, V_c and V_r are proportional to N_r^2 and $(N_r N_c^2)$, respectively. Therefore, the transparent conductor is not preferred as the row line for the sake of current capacity and power consumption. Metal electrode lines are preferred as row lines because of its lower resistivity. In Fig. 6.10(a), V_c is plotted vs. the number of row lines or R_c for a typical case. Fig. 6.10(b) shows the V_r vs. the number of lines for a typical case. As the number of lines becomes larger than 500, V_r, V_c and therefore the power consumption on the electrode lines could become comparable to those of the OLEDs. From the considerations (i) and (iii), we can conclude that the power efficiency of a large PMOLED array could drop by over a factor of 4 in a worst case, as compared to the value produced by an OLED under a low dc driving condition.

Finally, there is one more consideration for PMOLEDs. The simple structure in Fig. 6.9(a) and its circuit in Fig. 6.9(b) is based on the "diode" (i.e. rectified) behavior of each individual OLED in the array. A shorted or leaky (under reverse bias) OLED in the PMOLED array will cause cross-talk between OLEDs and perturb the normal operation of the array. This is illustrated in Fig. 6.9(c), which is the equivalent circuit of Fig. 6.9(b) when a forward bias is applied to one of the OLEDs.

6.2.2 Active Matrix OLED Displays

In an active matrix scheme, each pixel is continuously and independently driven and therefore it need not be driven to a high peak brightness. The problems associated with the high peak brightness in the PMOLEDs mentioned above can therefore be solved by an active matrix addressing scheme. Besides, in the active matrix OLED (AMOLED)
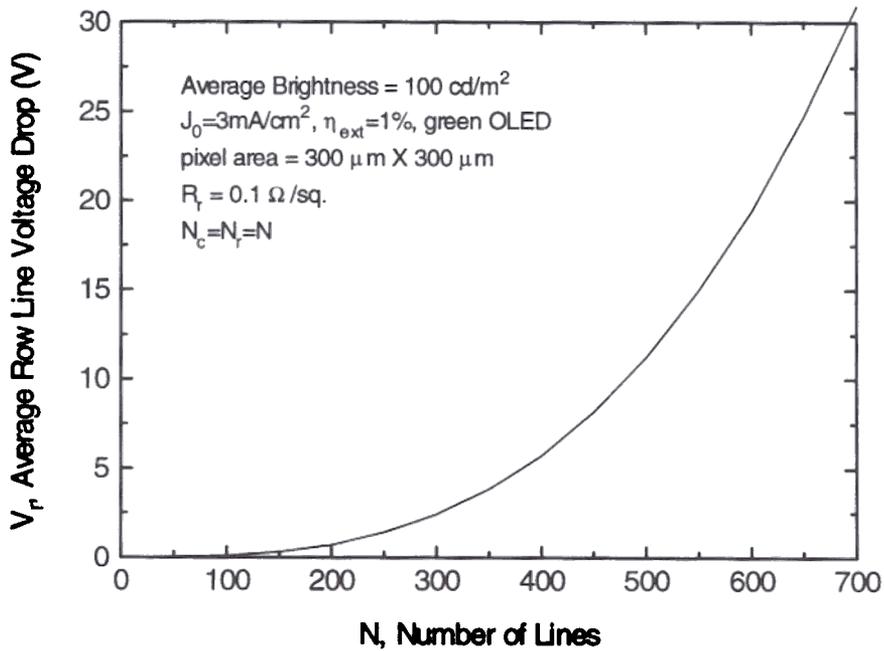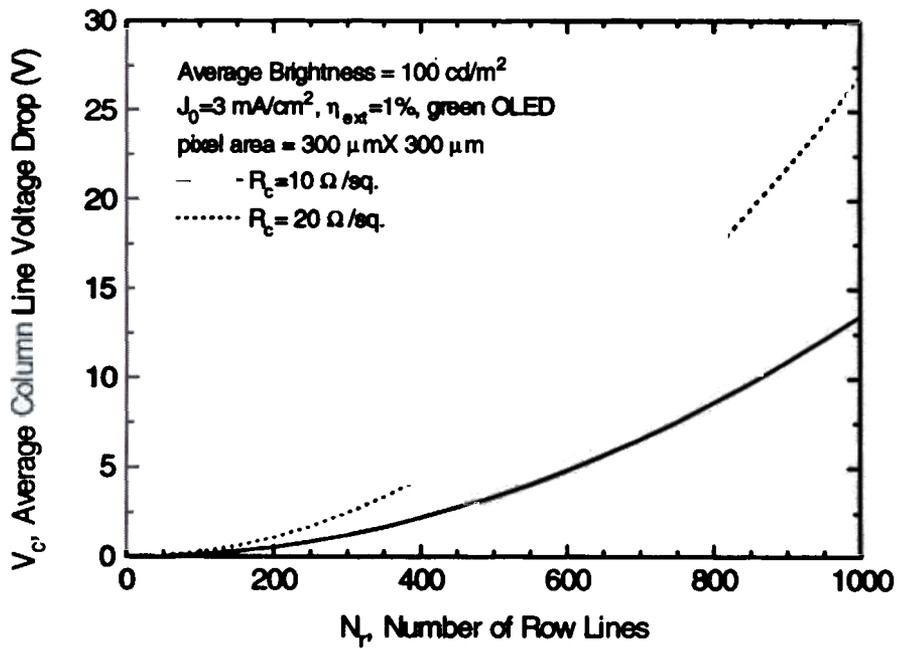
Fig. 6.10: (a) The average voltage drop across the column line, V_c, and (b) the average voltage drop across the row line, V_r, vs. the number of lines, N, in the PMOLED array, for different sheet resistances.

array, a defective OLED will not cause the cross-talk problem and will remain as a point defect in the array. One possible pixel circuit for an AMOLED is shown in Fig. 6.11(a). Similar pixel circuits have been previously used in active-matrix (inorganic) thin-film EL displays (since the early 1970s!!) [9,10]. In this circuit, each pixel contains two field effect transistors (FETs) and separate supply and ground connections. The transistor T1 functions as the switching and addressing element as the transistor in an AMLCD pixel, while the transistor T2 is used to drive the OLED. The function of the whole circuit is like a "sample and hold" circuit: When T1 is on, new data presented at the column line is 'sampled" into the storage node. After T1 is switched off, the voltage "held" at the storage node forces T2 to continuously drive the OLED. Depending on whether n-channel or p-channel transistors are used and whether the anode or the cathode of the OLED is connected to the transistor T2, of course, there could be variations of the pixel circuit shown in Fig. 6.11(a). These variations are shown in Fig. 6.11(b)-(d). T2-OLED circuits in Fig. 6.11(a) and Fig. 6.11(d) are in the configuration of source followers. That is, the source voltage of T2 shifts with the voltage appearing on the gate of T2 in the same direction. Instead, T2's in Fig. 6.11(b) and Fig. 6.11(c) function as current sources to the OLEDs. The current is independently modulated by the voltage between the gate and the source. Since the source is connected to a constant voltage (ground or V_{dd}), the current is only dependent on the characteristics of the transistor T2 as long as T2 stays in the saturation mode. From the circuit point of view, the current-source configuration is simpler and more straightforward.

However, there are also considerations with regard to the fabrication of the AMOLED array. In the structures of Fig. 6.11(b) and Fig. 6.11(d), the structure of the OLED is "inverted" so that the metal cathode of the OLED is at the bottom and is in contact with the drain of the n-channel transistor or the source of the p-channel transistor. The fabrication of the "inverted" OLEDs is in general more difficult because of the challenges associated with the formation of the ITO anode contact on top of the organic
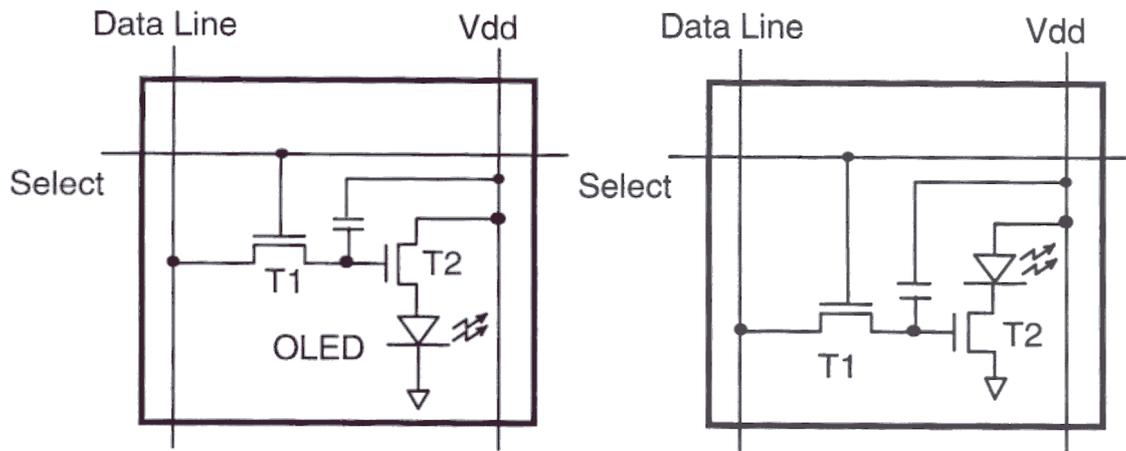
(a)
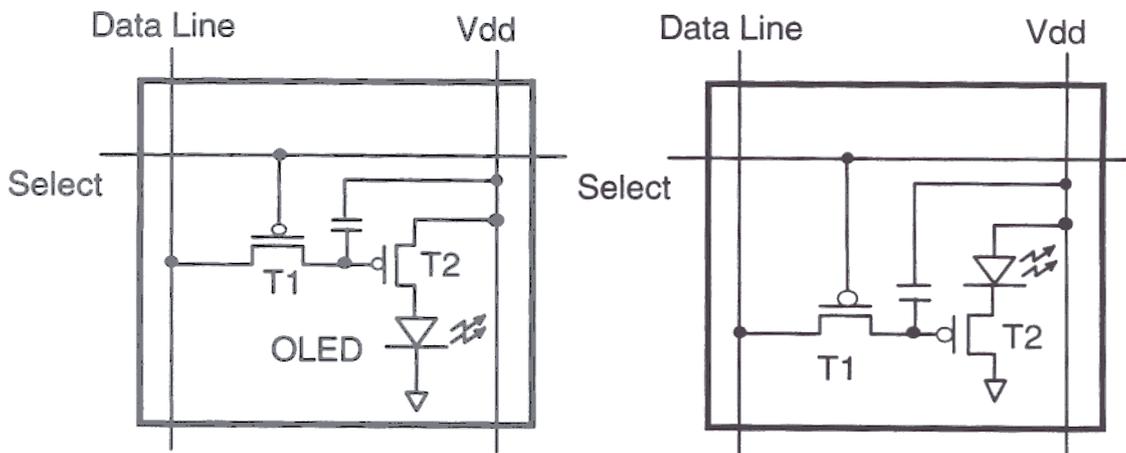
(c)

Fig. 6.11: Pixel circuits for an active matrix OLED array. (a) and (b) use n-channel FETs. (c) and (d) use p-channel FETs. (a) and (d) are in the source-follower configuration. (b) and (c) are in the current-source configuration.

layer and the interface between the metal cathode and the organic layer [11,12]. Nevertheless, recently there were two reports of the "inverted" OLEDs using other organic materials [11,12]. Such an "inverted" OLED structure poses some potential processing difficulties in patterning the reactive bottom cathode contacts for each pixel in an AMOLED array. In contrast, in the AMOLED array using the "conventional" (anode at the bottom) OLED structure, only the bottom anode is patterned and there is no need to pattern the blanket top reactive cathode contact. This has actually been another important advantage of the AMOLEDs. Therefore, in terms of the OLED fabrication, the structures in Fig. 6.11(a) and Fig. 6.11(c) are more feasible in practice. The structures of Fig. 6.11(a) and Fig. 6.11(c) use n-channel and p-channel transistors, respectively. For crystalline Si (x-Si) and polycrystalline Si (p-Si) technologies, both n-channel and p-channel transistors are available. For the amorphous Si (a-Si) technology, which is the currently dominant technology for active matrix LCDs (AMLCDs), only n-channel transistors are available because of the poor field effect mobility of holes in a-Si. Fabricating the "conventional" OLED structure on top of a p-channel a-Si thin film transistors (TFTs) to form a current source structure as in Fig. 6.11(c) is therefore not practical. From the considerations both in transistors and OLEDs, we have therefore chosen the structure of Fig. 6.11(a) to demonstrate the integration of a-Si TFTs with the OLEDs.

6.2.3 Power Consumption and Transistor Requirements in AMOLEDs

As in the PMOLED array, of course there is also power consumption on different electrode wires in the AMOLED array. In the following, the structure of Fig. 6.11(a) is used as an example to estimate the power consumption on electrode wires. Data lines and select lines are only used to drive capacitors. There are no large dc currents on these lines. The cathodes of all OLEDs can be connected to the ground through the blanket top cathode contact. Therefore, the power consumption on these electrode lines are negligibly

174

small compared to the power consumption on OLEDs or V_{dd} lines. We now further analyze the power consumption on the V_{dd} lines. Again, consider an AMOLED array with $N_r \times N_c$ pixels, a negligibly small gap between pixels and a pixel size of $L_c \times L_r$, where N_r and N_c are the numbers of rows and columns, and L_c and L_r are the pixel width and the pixel height, respectively. Under a dc driving condition, the current density required to achieve a certain brightness B_0 for an OLED pixel is J_0. Then, under the active matrix addressing scheme and the brightness B_0 (all OLEDs fully on with a brightness of B_0 in the worst case), P_{dd}, the total power consumption on the V_{dd} lines in the whole array can be (approximately) expressed as follows:

$$
\begin{aligned}
P_{dd} &= N_c \sum_{i=1}^{N_r} (R_{dd} \frac{L_r}{L_{dd}})[(J_0 \times L_c L_r \times A)(N_c - i + 1)]^2 \\
&= N_c (J_0 L_c L_r A)^2 (R_r \frac{L_r}{L_{dd}}) \frac{N_r(N_r + 1)(2N_r + 1)}{6}
\end{aligned}
$$

where R_{dd} and L_{dd} are the sheet resistance and the width of the V_{dd} lines, respectively. A is the aperture ratio (%) of the pixel (i.e. the ratio between the actual OLED area and the pixel area). With the voltage drop V_{LED} on the OLEDs (at the brightness of B_0), the total power consumption for all OLEDs in the whole array, P_{LED}, is:

$$
P_{LED} = N_c \times N_r \times (J_0 \times L_c L_r \times A) \times V_{LED}
$$

The P_{dd}-to-P_{LED} ratio is:

$$
\frac{P_{dd}}{P_{LED}} \approx \frac{\frac{1}{3}(J_0 L_c L_r A)(R_{dd} \frac{L_r}{L_{dd}})N_r^2}{V_{LED}} = \frac{V_p}{V_{LED}}
$$

where V_p is defined as the average voltage drop across the V_{dd} line. When compared to the OLED voltage, it gives the ratio between the power consumption on the V_{dd} lines and the power consumption on the OLEDs. In Fig. 6.12(a), V_p is plotted vs. the number of row lines or L_r/L_{dd} for a typical case. As long as $R_{dd} \times (L_r/L_{dd})$ is kept small (i.e. $<1\Omega$
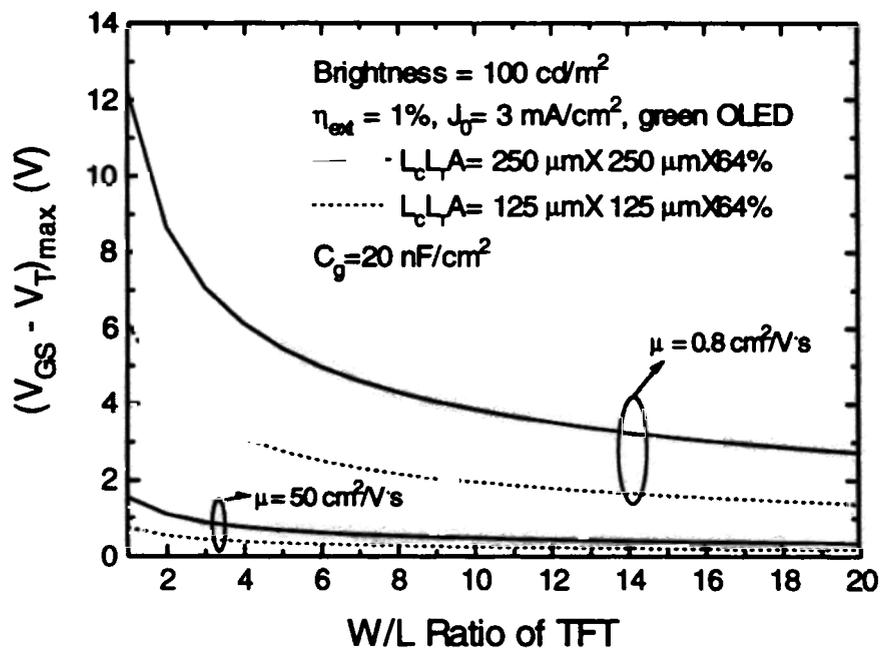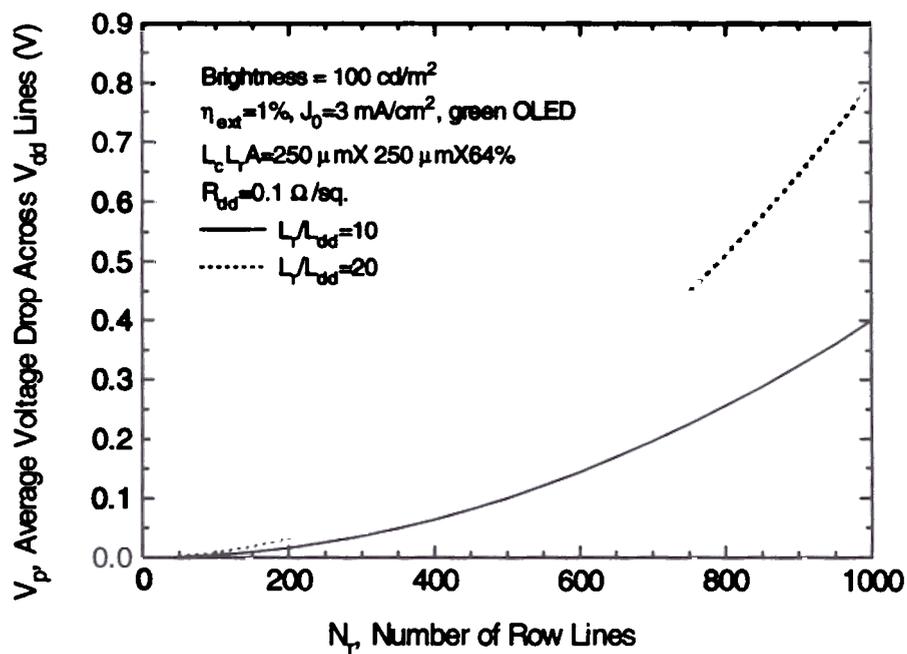
175

Fig. 6.12: (a) The average voltage drop across the V_{dd} line, V_p, vs. the number of row lines and (b) minimum V_{DS} on the transistors to insure the drive transistor T2 always in saturation for the circuits of **Fig. 6.11**.

/square) by using V_{dd} lines of low sheet resistance (e.g. Al lines) and larger width, the power consumption on the V_{dd} lines is small compared to the OLED power consumption.

The main tradeoff of using the active matrix, in addition to its cost, is the power consumption on the transistors. The transistor T1 is only on during the row dwell time. In contrast, there is a continuous current flow through the transistor T2. The main penalty will therefore come from T2. It is more a problem if the transistors are thin film transistors (TFTs) usually used in large-area active-matrix displays, because of their low carrier mobility and therefore higher drive voltage. We now consider the power dissipation in transistors T2. Consider a n-channel TFT in the saturation mode, where the formula for the drain current I_D is as follows [13]:

$$ I_D = \frac{1}{2}\mu_{FE}\, C_g \frac{W}{L}(V_{GS} - V_T)^2 \qquad V_{DS} \geq V_{GS} - V_T \qquad (6.9) $$

μ_{FE}: field effect mobility

V_T: threshold voltage

V_{GS}: gate to source voltage

C_g : the gate capacitance per unit area

W and L: the channel width and length

Then, the supply voltage V_{DD} must be large enough to give enough V_{DS} (drain to source voltage) swing to keep the transistor T2 always in the saturation mode:

$$ V_{DS} \geq (V_{GS} - V_T)_{max.} = \sqrt{\frac{2J_0 L_c L_r A}{C_g \mu_{FE} \frac{W}{L}}} \qquad (6.10) $$

In the above equation, and $(V_{GS}-V_T)_{max.}$ is $(V_{GS}-V_T)$ at $I_D = I_{OLED} = J_0 L_c L_r A$. Because of the voltage drop along the V_{dd} lines, each TFT has a slightly different V_{DS}

with the same drain (or OLED) current. The total power consumption on the T2's in the whole array, P_{FET}, is:

$$P_{FET} = \sum_{T2's} (I_D \times V_{DS}) = \sum_{T2's} (I_{OLED} \times V_{DS})$$

$$\geq N_cN_r(J_oL_cL_rA)(V_{GS}-V_T)_{max.}+N_c\sum_{i=1}^{N_r}(J_oL_cL_rA)^2(R_{dd}\frac{L_r}{L_{dd}})(\frac{(i)(i+1)}{2}) \quad (6.11)$$

$$\approx N_cN_r(J_oL_cL_rA)[(V_{GS}-V_T)_{max.}+\tfrac{1}{6}(J_oL_cL_rA)(R_{dd}\frac{L_r}{L_{dd}})N_r^2]$$

The P_{FET}-to-P_{LED} ratio is:

$$\frac{P_{FET}}{P_{LED}} \geq \frac{(V_{GS}-V_T)_{max.}}{V_{LED}}+\frac{\tfrac{1}{6}(J_oL_cL_rA)(R_{dd}\frac{L_r}{L_{dd}})N_r^2}{V_{LED}} \quad (6.12)$$

The second term in the equation (6.13) is similar to that in the equation (6.9). Fig. 6.12(b) shows $(V_{GS}-V_T)_{max.}$ as a function of the W/L ratio of the TFT for different OLED areas and different μ_{FE}, with OLEDs of 1% external quantum efficiency. From this figure, it is clear that the voltage drop and therefore the power consumption on the transistor are small compared to those of the OLED itself, if the transistor mobility is high enough, as in the case of crystalline Si (x-Si) transistors or polycrystalline Si (p-Si) TFTs. Even with the low mobility of amorphous Si (a-Si) TFTs, the voltage drop and the power consumption on the TFT can be reduced to a level comparable to those of the OLED itself by matching the W/L (~8) ratio of the TFT to the OLED current requirement. Therefore, the reduction of the power efficiency by the incorporation of the active matrix could be controlled within a factor of two, as compared to the value produced by an OLED under a low dc driving condition. In terms of the power efficiency, AMOLED is a better choice than PMOLED when the number of lines is large. Although we use n-channel transistors as examples, the above discussion is valid for any structure in Fig. 6.11. There is no major difference in the power consumption among these structures.

178

Both of the OLED and TFT thin-film technologies are conventionally fabricated on breakable glass substrates. With the dream of making a flat panel display that is unbreakable, lightweight and flexible, there have been some successful demonstrations of OLEDs or LCDs fabricated on plastic substrates [14-17]. The fabrication of a-Si TFTs on plastics, however, has been more problematic because of the difficulties associated with mechanical and chemical instabilities of plastics at the processing temperature of a-Si TFTs (~300 °C) [18]. Therefore, the integration of both OLEDs and TFTs on a flexible plastic substrate to make an unbreakable active matrix display is still problematic. One major reason for making AMLCDs and LCDs on glass or plastic substrates is the requirement of substrate transparency for the transmissive type of displays, in which the light emitted from lamps mounted in the back has to pass through the substrate to reach the liquid crystal light valves. Since OLEDs are emissive themselves and can be made to emit light from the front surface of the structure [7,19], the transparency of substrates is not inherently required for OLED/TFT integration, lending more freedom to our choice of substrates. Besides, the top (surface)-emitting OLED-TFT structure has the potential to achieve a nearly 100% aperture ratio, an advantage over the bottom-emitting OLED-TFT structure. Thin steel foils, which have excellent mechanical strength, flexibility, light weight and thermal stability, have been previously demonstrated by Theiss et al. to be compatible with TFT processing [18,20]. In the following, we demonstrate the integration of a-Si TFTs with top-emitting OLEDs onto stainless steel thin foils through the collaboration with Dr. S.D. Theiss and G. Gu in Prof. Wagner's and Prof. Forrest's groups, respectively.
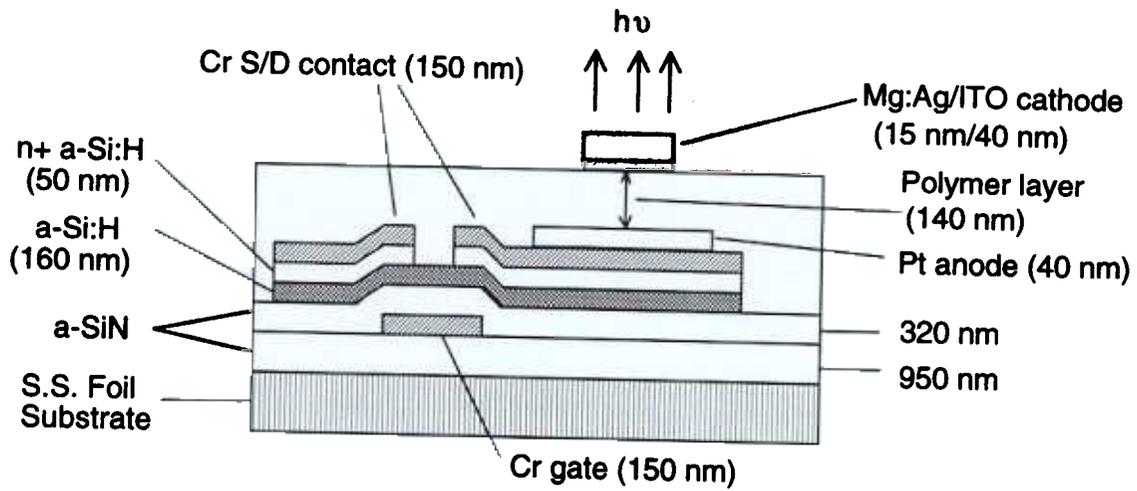
6.2.4 Structures and Processing for OLED/TFT Integration on Thin Steel Foils

OLEDs are carrier-injection devices conventionally built on glass substrates precoated with indium tin oxide (ITO) used as the bottom, hole-injecting anode contact. In this configuration, light emits through the transparent ITO layer and the glass substrate.
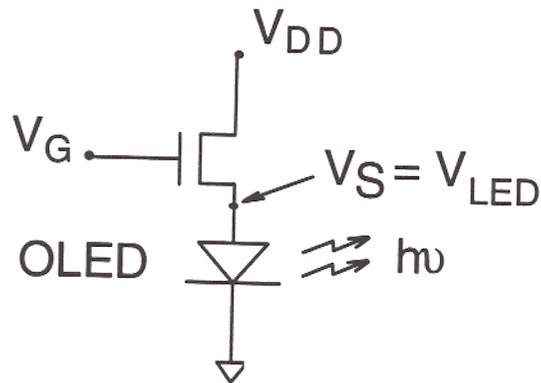
To make top-emitting OLEDs on the opaque steel substrate, the transparent bottom anode contact has been replaced by the high work function metal Pt, which is found to have a hole injection efficiency comparable to ITO, as described in Chapter 5. On the other hand, semitransparent cathode contacts needed for top surface emission can be formed by using thin (<20 nm) layers of low work function metals such as Ag [21]. These thin single-layer metal films, however, cannot provide efficient electron injection and have high sheet resistance, leading to rather low quantum efficiency (<0.01%) and high drive voltage. In this device, we therefore employ double-layer cathode contacts invented by Gu et al.[5], in which a thin (100-170 Å) semitransparent Mg:Ag layer provides for electron injection, while a transparent and conducting ITO cap layer provides for high conductivity and environmental robustness. A transmittance of ~70% can be achieved using this cathode composition [5].

A schematic cross section of the integrated TFT/OLED is shown in Fig. 6.13(a), with the circuit shown in Fig. 6.13(b). The steel foil substrates are 200-μm thick, one-side polished, grade 430 stainless steel, and possess an rms surface roughness of ~70 nm. An insulating barrier layer, a-SiN$_x$:H, was first deposited to electrically isolate the active devices. a-Si TFTs with an inverted-staggered structure and a W/L ratio of 776/42 μm (~18), were then fabricated on top of the barrier layer. All a-Si:H and a-SiN$_x$:H layers were deposited at a pressure of 500 mtorr in a three-chamber plasma enhanced chemical vapor deposition (PECVD) system, in which undoped a-Si:H (at 250 °C), n$^+$ a-Si:H (at 260 °C) and a-SiN$_x$:H (at 310 °C) are deposited in separate chambers. Chromium gate and drain/source contacts were deposited by a separate thermal evaporating system. The details of material growth and TFT device fabrication have been previously described [18,20]

After fabrication of the TFTs, top-emitting OLEDs were then deposited on the surface of the 2mm×2mm Cr source/drain contact pads. OLEDs were fabricated by sequential e-beam deposition and patterning of 400 Å thick Pt anode contacts through a

180

hυ

Cr S/D contact (150 nm)

Mg:Ag/ITO cathode
(15 nm/40 nm)

n+ a-Si:H
(50 nm)

Polymer layer
(140 nm)

a-Si:H
(160 nm)

Pt anode (40 nm)

a-SiN

320 nm

S.S. Foil
Substrate

950 nm

Cr gate (150 nm)

(a)

V_{DD}

V_G

$V_S = V_{LED}$

OLED   hυ

(b)

Fig. 6.13: (a) Schematic cross section of the integrated OLED/TFT on the steel foil substrate. The active area of the OLED is determined by the size of the Mg:Ag/ITO cathode contact, which is a circle with a diameter of 250 μm. The TFT has a W/L of 776 μm/42 μm. (b) The circuit of the integrated OLED/TFT structure.

181

shadow mask, spin-coating of a continuous layer of 1400-1700 Å active luminescent polymer, followed by the deposition of semitransparent double-layer Mg:Ag (10:1)/ITO top cathode contacts through a shadow mask. The OLEDs consist of single-layer doped polymer thin films, with the composition of PVK:PBD:C6 (100:40:0.3 by wt.). The Pt anode was treated by the oxygen plasma as described in Chapter 5 (section 5.2) before the deposition of the organic layer. Mg:Ag was deposited by thermal co-evaporation from two separate sources, and ITO was deposited from a mixed In_2O_3:SnO_2 (90 : 10 wt%) target by RF magnetron sputtering in an Ar/O_2 ambient at room temperature [5]. The overlap of the anode and cathode contact areas gives a 250-μm-diameter circular OLED, without the need to separately isolate the organic layers. All OLED fabrication steps were performed at room temperature. The contacts to the drain, gate, source and Pt anode were made by probing through the organic layer.

6.2.5 Results and Discussions

The transfer and output characteristics of the a-Si TFT on the steel foil are shown in Fig. 6.14(a) and Fig. 6.14(b), respectively. The saturation characteristics of the same TFT are shown in Fig. 6.14(c). From these characteristics, we obtained a threshold voltage of ~3.5 V, a subthreshold slope of 0.9 V/decade, an electron mobility of 0.6 cm^2/V·s (from the saturation characteristics), and an on/off current ratio of >10^5. The characteristics of TFTs with or without OLEDs are similar.

Fig. 6.15 shows typical current-voltage (I-V) characteristics for the isolated TFTs and the isolated OLEDs in the integrated TFT/OLED on steel foil substrates, and the integrated TFT/OLED itself. The on/off characteristics of TFTs measured as a function of the gate-to-source voltage V_{GS} at the drain-to-source voltage V_{DS} = 40V are shown. The forward current of the OLED vs. the OLED voltage V_{LED} are also shown in Fig. 6.15, and are similar to previous results for devices built on ITO-coated glass substrates and capped with opaque Mg:Ag contacts, except for a higher (~50%) drive voltage. The
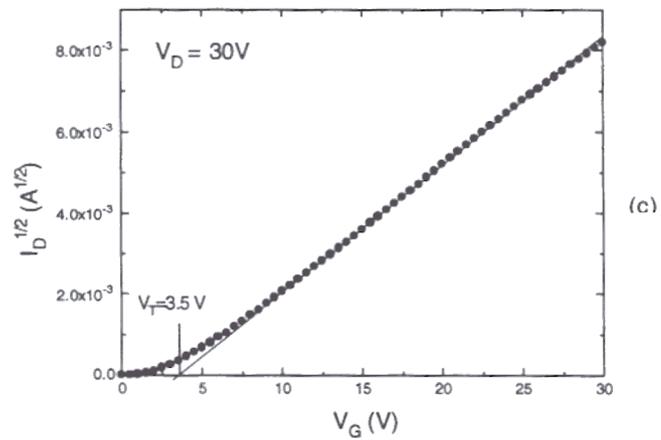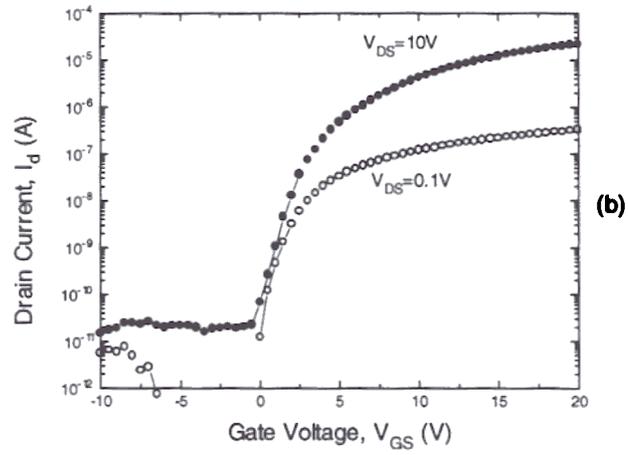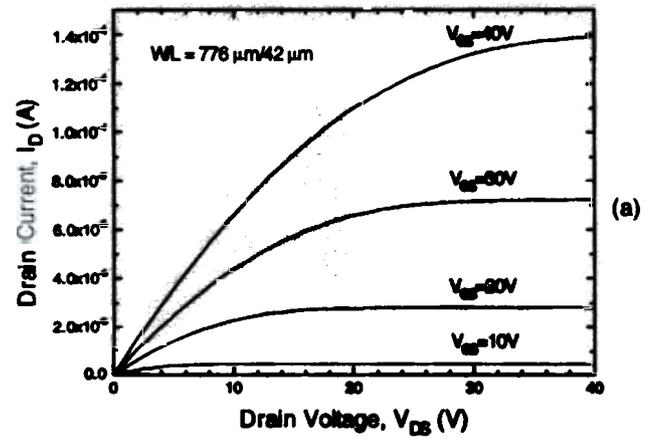
Fig. 6.14: (a) Transfer characteristics, (b) subthreshold characteristics and (c) saturation characteristics of the a-Si TFT on steel foils.
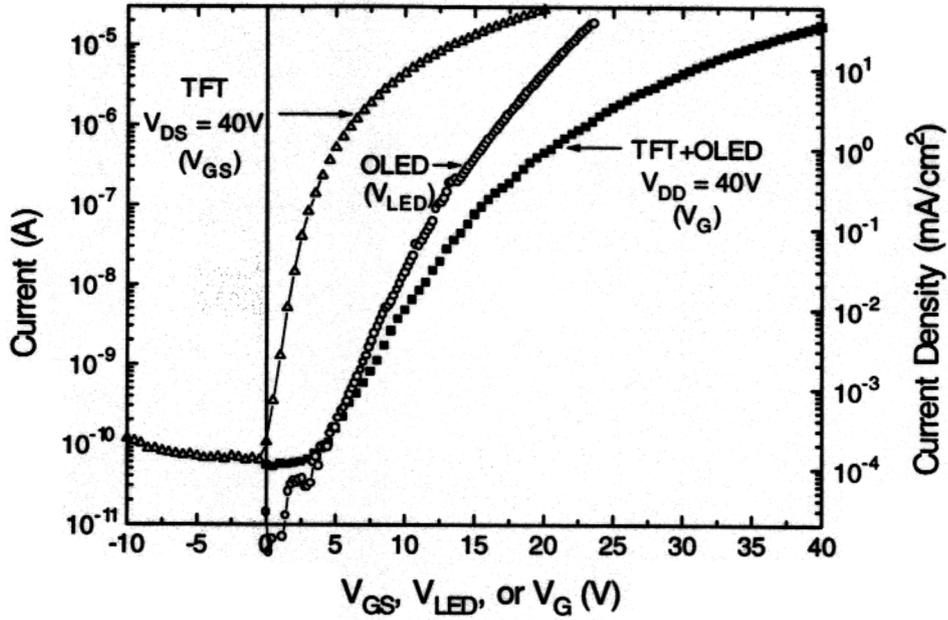
Fig. 6.15: I-V characteristics of the TFT (vs. the gate-to-source voltage V_{GS}), the OLED (vs. the OLED voltage V_{LED}) and the integrated OLED/TFT structure (vs. the gate voltage V_G). The lefthand ordinate is for all three curves and the right ordinate is for the OLED and the integrated OLED/TFT.

higher voltage is partly due to the thicker polymer layers (1400 vs. 1000 Å) used to compensate for the roughness of the steel surface, and is probably also due to the additional resistance at the Mg:Ag/ITO interface resulting from the oxidization of Mg:Ag by ITO [5]. For the integrated TFT/OLED circuit, the drain current measured as a function of the gate voltage V_G at $V_{DD} = 40V$ is also shown in Fig. 6.15. At a given current level, $V_G = V_{GS} + V_{LED}$ required to maintain that current, as expected from the source-follower configuration. Clearly, the TFT can successfully switch the OLED on and off through the gate voltage V_G.

The electroluminescence spectrum of the top-emitting OLED is shown in Fig. 6.16, and is compared with that of a conventional bottom-emitting OLED made on an ITO-coated glass substrate. Both spectra are similar, except for a slight red shift in the spectrum of the top-emitting structure due to the semitransparent cathode contact [5]. Light intensity vs. forward bias voltage of the OLED and vs. V_G ($V_{DD} = 40V$) in the integrated OLED/TFT structure are shown in Fig. 6.17. Light emission is proportional to the current (inset of Fig. 6.17). This Pt/PVK:PBD:C6/Mg:Ag/ITO device has an external EL quantum efficiency η_e ~0.06% photon/electron. The efficiency is lower than our conventional ITO/organic/opaque Mg:Ag devices (typically with η_e ~1% at 7 to 18 V and 25 mA/cm^2 for ~1400 Å thick organic thin films), indicating that the present devices are not inherently limited by the organic materials. In Fig. 6.18, the I-V and L-I characteristics of the conventional ITO/PVK:PBD:C6/opaque Mg:Ag, ITO/PVK:PBD:C6 /thin Mg:Ag/ITO and the Pt/PVK:PBD:C6/thin Mg:Ag/ITO are compared. For the ITO/PVK:PBD:C6 /Mg:Ag/ITO device, the light intensity is the summed optical output from both surfaces. In the OLED using the ITO anode on glass and the thin Mg:Ag/ITO cathode, the efficiency drops from 1% for the conventional OLED to 0.15% and the drive voltage increases. Further replacing the ITO anode with Pt, the I-V characteristics remain unchanged while the efficiency further drops to 0.06%. We attribute the reduction of the efficiency to the lower optical transparency of the Mg:Ag/ITO cathode contacts than the
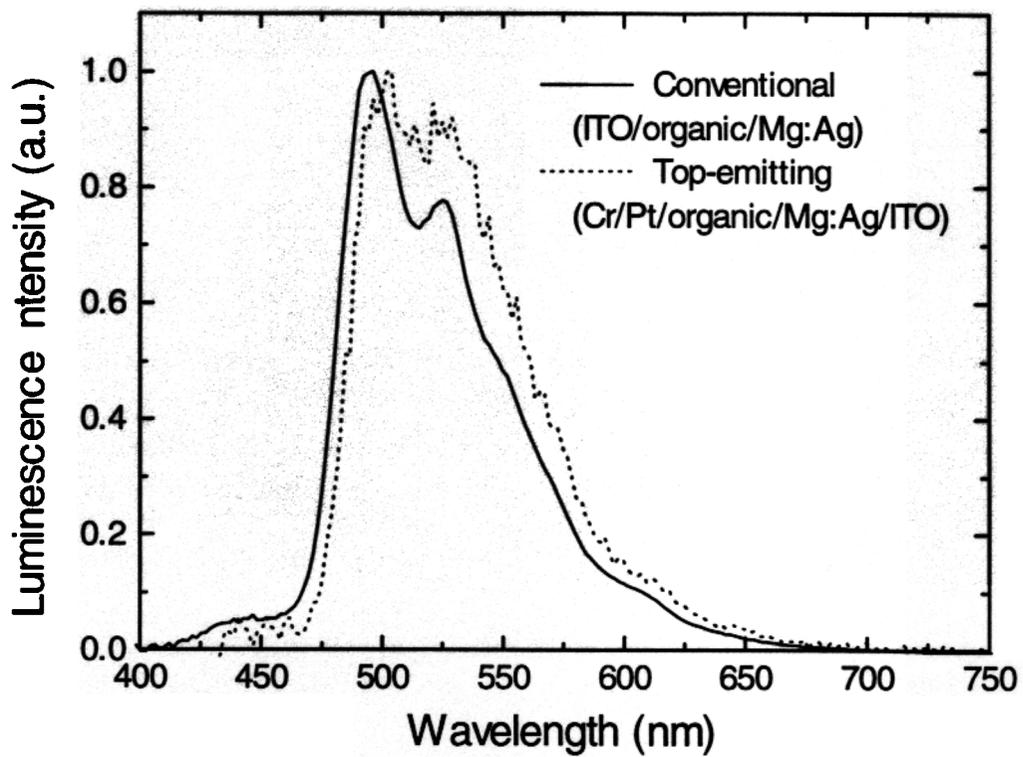
185

Fig. 6.16: Electroluminescence spectra for the Cr/Pt/polymer/Mg:Ag/ITO top-emitting structure and the conventional ITO/polymer/Mg:Ag bottom-emitting structure.
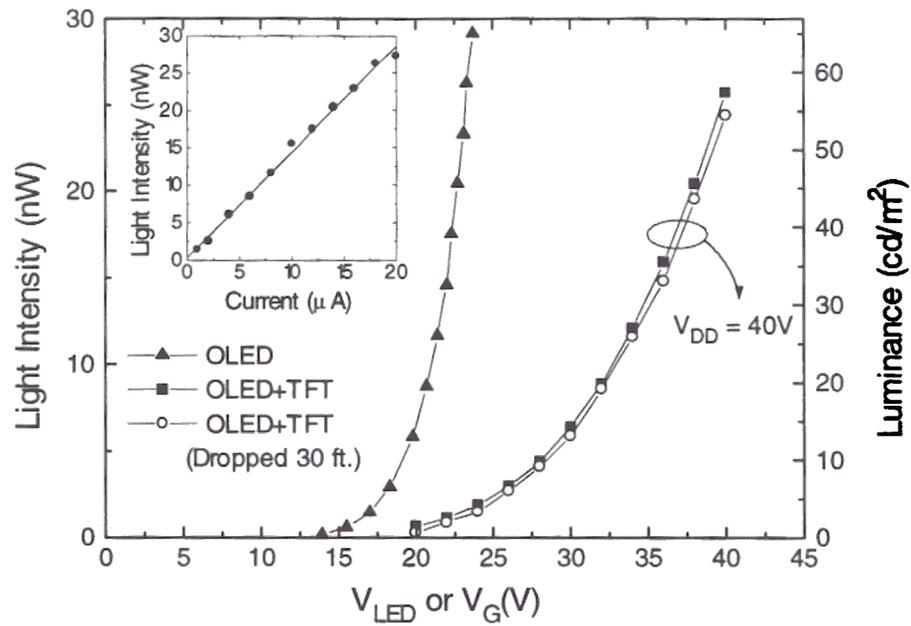
Fig. 6.17: Light intensity vs. the OLED voltage V_{LED} for the OLED, and vs. the gate voltage V_G for the integrated OLED/TFT. The right ordinate shows the corresponding luminance unit. The inset shows the light intensity vs. the OLED current.
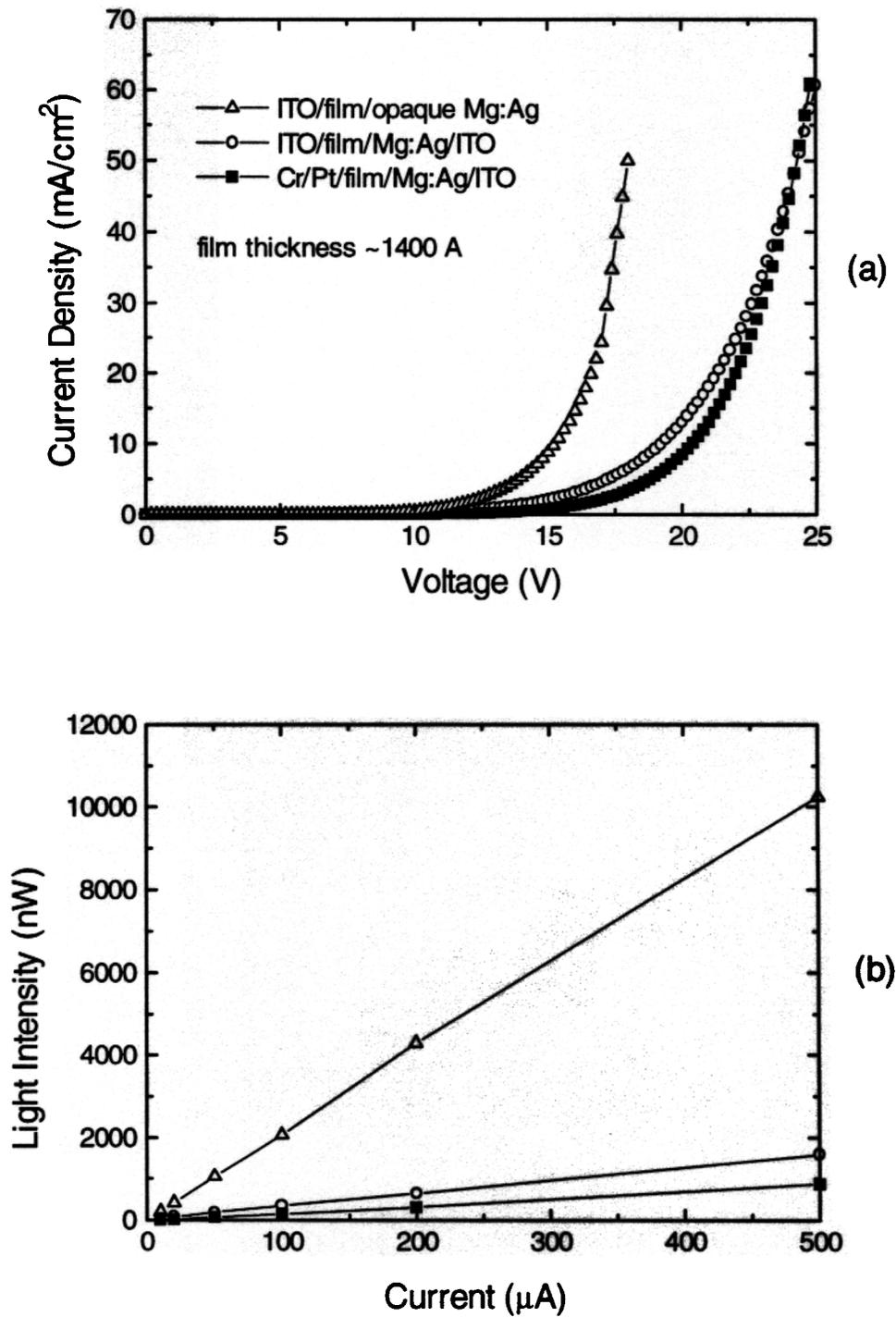
Fig. 6.18: (a) I-V and (b) L-I characteristics of the conventional ITO/PVK:PBD:C6/ opaque Mg:Ag, ITO/PVK:PBD:C6 /thin Mg:Ag/ITO (summed optical output from both surfaces) and the Cr/Pt/PVK:PBD:C6/thin Mg:Ag /ITO devices. Device diameter = 1mm.

ITO anode and the low reflectivity of Pt bottom anode contacts (~60%) to visible light. Since the drive voltages are increased when the opaque Mg:Ag cathode is replaced with the semitransparent Mg:Ag/ITO cathode, the electron injection ability may also be reduced by the thin Mg:Ag/ITO cathode in these devices, but this is not well understood.

Due to the ruggedness of the steel foil substrate, the finished sample can withstand considerable mechanical stress. Dropping the finished foil (4 cm× 4 cm) over 30 feet onto concrete had no significant effect on the characteristics of the devices, as shown in Fig.

1 mm thick glass substrates were destroyed under such a test. The photograph in Fig. 6.19 shows a TFT driving an OLED on a steel foil flexed to a radius of curvature of ~

Because of the lower efficiency of the present top-emitting OLED (~0.06%, 0.22 cd/A), a high OLED current density of ~40 mA/cm^2, corresponding to the drain-to-source current $I_{DS} = 20$ μA, has to be applied to achieve a brightness close to that used in video displays (~100cd/m^2). However, an OLED with η_e=1% (3.6 cd/A) only requires a current density as low as ~3mA/cm^2 for 100cd/m^2, corresponding to I_{DS} ~ 2μA. If such a top emitter structure were achieved, this current requirement could easily be met with V_{GS} and V_{DS} below 10V with W/L <8, as is apparent from Fig. 6.12 and Fig. 6.15

6.3 Summary

In summary, we have demonstrated the integration of individual polymer-based OLEDs with different organic layers onto a single substrate. The integrated orange, green and blue devices on the same substrate show no degradation compared to discrete devices. We have also demonstrated the integration of polymeric OLEDs and a-Si TFT drivers onto lightweight, rugged and flexible steel foil substrates. By matching the W/L ratio of of the a-Si TFTs to the OLED drive current requirement, the a-Si TFTs can provide adequate current to drive OLEDs
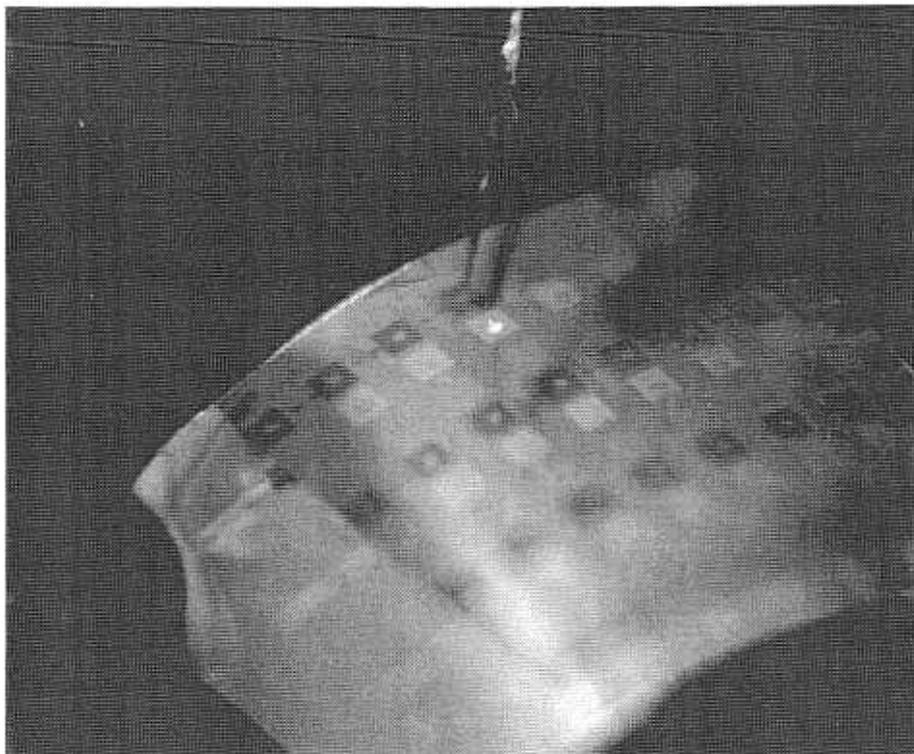
Fig. 6.19: Photograph of a TFT driving an OLED on a flexed steel foil, with probes on the drain, gate and the cathode of the OLED.

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Conclusion

7.1 Summary

This thesis has addressed three different topics related to polymer-based organic light emitting devices (OLEDs): OLEDs made with single-layer doped polymers, various anode and cathode contacts to doped polymers, and the integration issues of polymer OLEDs in the context of display applications.

Thin films of the hole-transport polymer PVK dispersed with different electron-transport and emissive agents have been the basis of this thesis work. We have experimentally identified various photophysical and electroluminescence phenomena in such doped polymer thin films. The device performance is found to be a strong function of the composition of the blend thin films, relating to the luminescence efficiency of emitting centers in the host polymer and the relative hole and electron injection/transport abilities. Various anode or cathode contacts to these doped polymer devices have also been examined. The indium tin oxide (ITO) and Pt anode contacts are improved with oxygen plasma treatment. Enhanced hole-injection efficiency substantially improves the device performance.

By sealing the organics from the harmful chemicals via carefully designed device structures and by using plasma dry etching techniques, a method has been developed to

sequentially fabricate and therefore integrate devices of different colors onto a single substrate, all with performance similar to discrete OLEDs made on separate substrates. We have also demonstrated the integration of both devices on a rugged, flexible and lightweight steel foil substrate by taking advantage of the thin-film structures and substrate versatility of both OLEDs and a-Si TFTs. The TFT in the integration structure successfully provides enough current to drive the OLED.

7.2 Future Work

There is no lack of topics for further research on polymer OLEDs, either in terms of a single OLED or in terms of their integration into display systems.

First, for OLEDs themselves, the formation of contacts and the interface between the contacts and the active organic layers are still important issues to the device performance. For example, in a paper recently reported by Hung et al. [1], a monolayer of insulating LiF inserted between the organic layer and an Al contact overlayer has substantially reduced the device voltage and increased the quantum efficiency, even to a point where results are better than those with a conventional reactive Mg:Ag alloy contact. On the anode side, a conducting polymer polyaniline inserted between the ITO anode and the active organic layer has similarly improved the device performance [2,3]. Therefore, it might be possible to further upgrade the device performance of doped-polymer OLEDs by applying different contact approaches other than those discussed in this thesis. In addition, the quenching of luminescence at the interface of single-layer doped-polymer thin films and metal contacts may be eliminated by wisely choosing an intermediate layer between the metal contact and the doped polymer layer.

Although we have demonstrated the integration of individual polymer-based OLEDs with different organic layers onto a single substrate by combining shadow masking and plasma dry etching, we have also pointed out that this approach has to be further

194

refined to produce smaller features used in high-resolution display applications. One possible approach is to incorporate the dry etching of metal layers. As for the active matrix OLED array, we can look forward to its realization with further work on integration processing.

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Appendix A

Publications and Presentations Resulting from this Thesis

Publications

[1] C.C. Wu, S.D. Theiss, G. Gu, M. Lu, J.C. Sturm, S. Wagner and S.R. Forrest, "Integration of organic LEDs and a-Si TFTs onto unbreakable and flexible metal foil substrates," submitted to *Electron Device Letters*, 1997

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