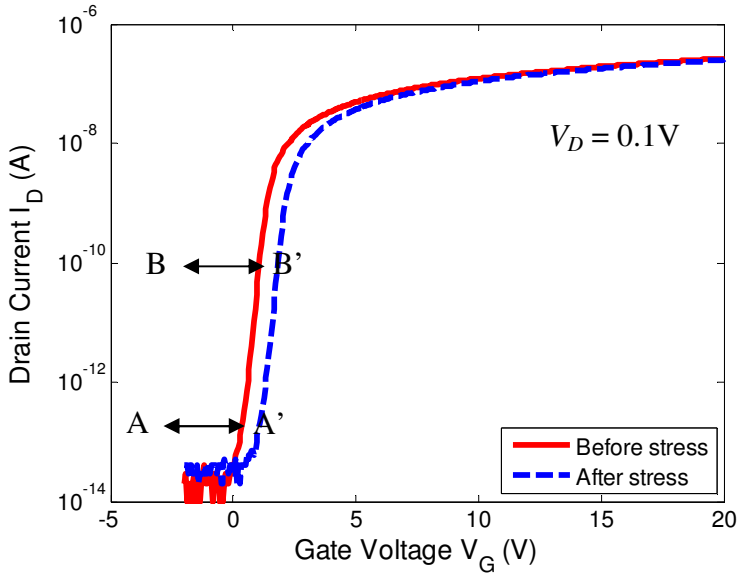
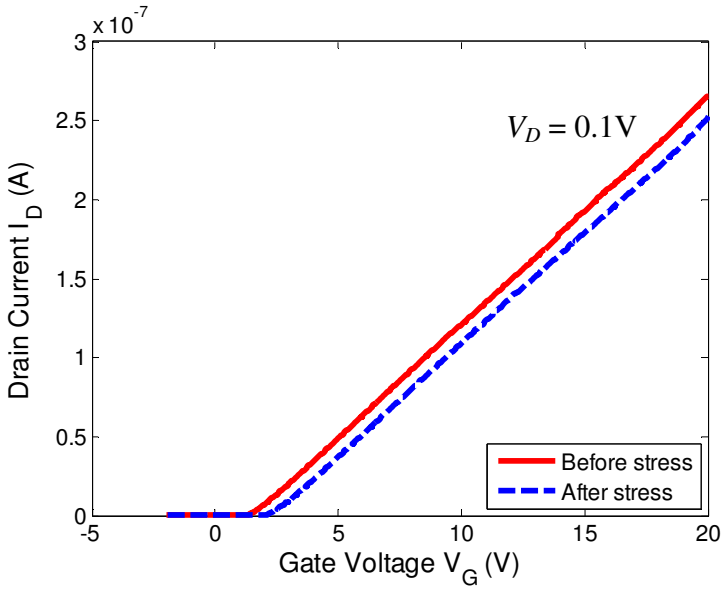


(a). Subthreshold plot



(b). Linear plot

Fig. 6.2. I_D - V_G of a-Si TFT with $W/L = 150/15$ µm before and after a 5 minutes stress with a 5 V gate voltage at 120°C.

From the transfer characteristics in Fig. 6.2(a), the sheet conductance before and after the low-gate stress can be obtained as a function of gate voltage V_G, using (6. 10). The surface potential ψ_s as function of gate voltage V_G, as calculated from (6. 9), is illustrated in Fig. 6.3.

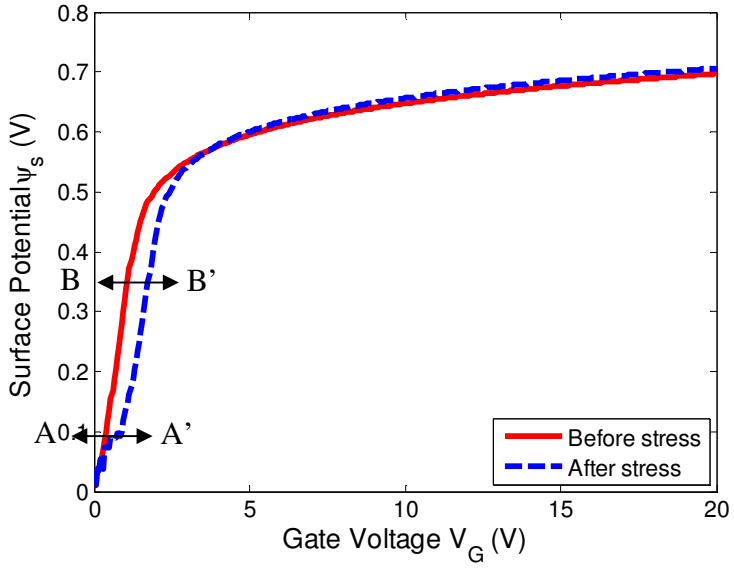


Fig. 6.3. Surface potential ψ_s as a function of gate voltage V_G before and after a 10 minutes stress with a 5 V gate voltage at 140°C.

The surface potential ψ_s increases with the increasing gate voltage and tends to saturate at high gate voltage. Using (6. 5) and (6. 6), the gap state density was then determined. Note that the work function of gate metal Cr is 4.37 eV and the electron affinity of a-Si is about 4.0 eV. We assume that the flat-band voltage $V_{FB} = 0$ V. Fig. 6.4 shows the gap state density above the Fermi level in flatband condition E_{F0}.

Before the low-gate field stress, the a-Si exhibits a peak in the mid gap state (~10^{17} eV^{-1} cm^{-3}) near the Fermi level. From 0.1 eV above the Fermi level, the gap state density increases monotonically towards the conduction band edge. The band tail has an exponential distribution over two orders of magnitude from the band edge, with an inverse logarithmic slope of ~50 meV/dec. The shape of the gap state density agrees well with the commonly accepted density of states model for a-Si [14]. The inverse slope of the band tail is higher than that determined from dispersive transport measurements [15, 16], which is about 30 meV. The higher band tail slope determined from our field-effect technique suggests that the a-Si near the a-Si / SiN_x interface is more disordered than in the bulk and we will discuss this later.

After the low-gate field stress, the mid gap state density increases to 10^{17} - 10^{18} eV^{-1} cm^{-3} (A-A' region in Fig. 6.4) and extends to about 0.3 eV above the Fermi level. From 0.3 to 0.5 eV above

the Fermi level, the density of band tail states is lower than that before the stress (B-B' region in Fig. 6.4). From 0.5 eV above the Fermi level, the tail states extend exponentially with an inverse slope of ~50 meV into the conduction band edge, following the distribution before the stress. Below 0.1 eV above the Fermi level, the extraction of defect density is affected by the limits to measure low current (~ 5×10^{-14} A). However, the observed redistribution of gap states exists up to at least 0.2 eV above the flatband Fermi level, so we are confident that this redistribution is a real effect and not caused by measurement inaccuracy.

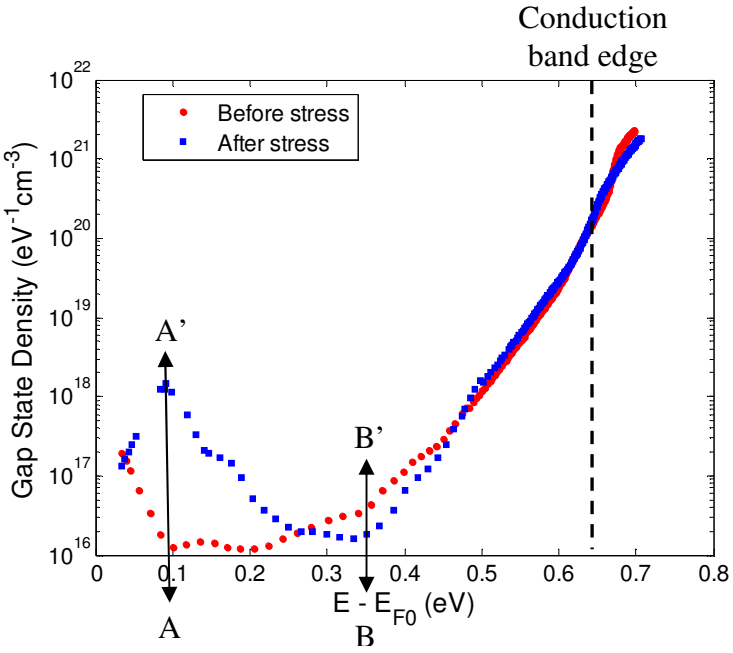


Fig. 6.4. Gap state density as a function of the gate voltage V_G before and after a 5-minute stress with a 5 V gate voltage at 120°C. The energy is relative to the Fermi level position at the flat-band condition.

6.4. *Discussion*

Because of the assumptions that are explicitly (Section 6.1.1) and implicitly made [8], the accuracy of the gap state density determined with the field-effect technique has been widely discussed [8, 17-19]. It has been shown that 90% of the field-effect conductance change is accounted for in the first 20 - 100 Å of the film, so the gap state density we obtained is actually probing the initial growth region of the a-Si on the gate SiN_x and does not necessarily represent the bulk properties [8, 18]. Fortunately, we are only interested in the a-Si property near the SiN_x /

a-Si interface in our a-Si TFT analysis. The differences in the gap state density before and after the low-field gate field stress arise from the changes in the transfer characteristics. In order to evaluate the accuracy of the obtained gap state density, we examined the transfer characteristics in Fig. 6.2(a) and relate the changes in the transfer characteristics to the redistribution of gate state density after the gate bias. Fig. 6.5 is the zoomed-in transfer characteristics to show the changes before and after the gate-bias stress corresponding to the redistribution in the mid gap state density (A-A' region) and band tail state density (B-B' region).

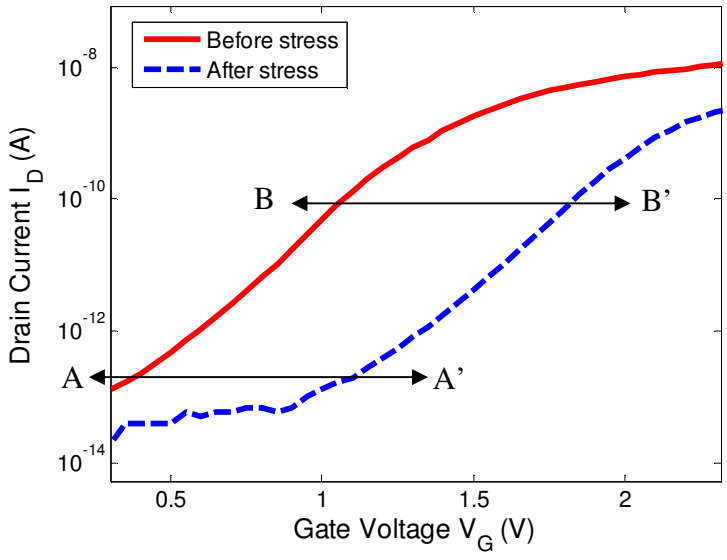


Fig. 6.5. Zoom-in of the transfer characteristics before and after a 5-minute stress with a 5 V gate voltage at 120°C.

The analysis in Section 6.1 suggests that the lower the rate at which the drain current increases with increasing gate voltage, the higher the gap state density is. This is because defect states slow down the increase in band bending and thus mobile electron concentration as gate voltage V_G increases. To clearly illustrate the changes in the transfer characteristics, we shift the transfer curve after stress in Fig. 6.5 along the x-axis and make it overlap the curve before stress (Fig. 6.6).

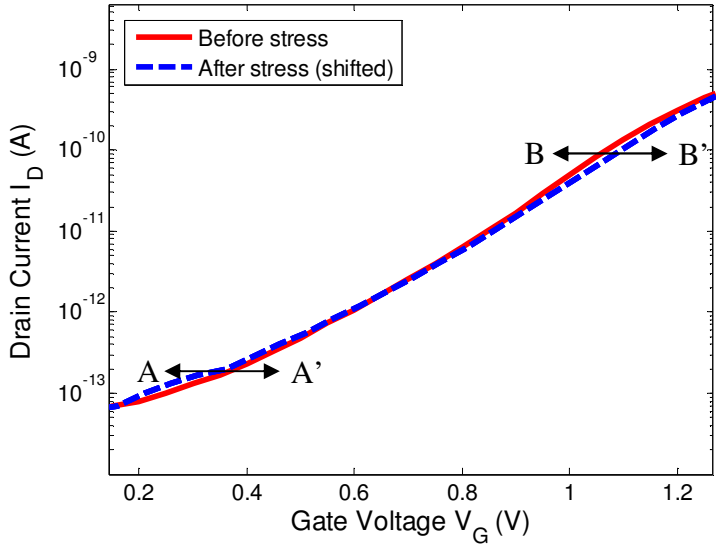


Fig. 6.6. Transfer characteristics with the after-stress curve shifted to overlap the before-stress curve.

From Fig. 6.6 in A-A' region, the rising rate of drain current vs. gate voltage became smaller after the gate stress. It explains the increased mid gap states after the gate-bias stress. In B-B' region, the rising rate of drain current vs. gate voltage became larger after the gate stress, leading to the decreased band tail states after the gate-bias stress. To a large extent, the accuracy of the field-effect technique is limited by the experimental precision [8]. Fortunately, our determination of the redistribution in the gap state density is larger than the limits of resolution caused by current measurement error, because the smallest current that can be detected in our measurement system is as low as 10^{-14} - 10^{-13} A.

6.5. *Summary and conclusion*

We biased the a-Si TFT with a constant gate voltage $V_G = 5$ V at 120°C for 5 minutes. After the low-gate field stress, the gap state density is redistributed. The density of the mid gap states increases and the density of band tail states from 0.3 to 0.5 eV above the Fermi level decreases. The mid gap states correspond to dangling bonds and the band tail states reflect weak bonds. The band tail states deeper into the gap are weaker and easier to be broken (Chapter 4). The difference in the distribution of the gap state density before and after the low-gate field stress suggests that defect creation happens in the a-Si of a-Si TFTs under low-gate field stress. It

supports the idea in our two-stage model (Chapter 4) that defect creation is the mechanism dominates in the long term.

References:

[1] B. Hekmatshoar, K. H. Cherenack, S. Wagner, and J. C. Sturm, "Amorphous silicon thin-film transistors with DC saturation current half-life of more than 100 years," in *Electron Devices Meeting, 2008. IEDM 2008. IEEE International*, 2008, pp. 1-4.

[2] B. Hekmatshoar, K. H. Cherenack, A. Z. Kattamis, K. Long, S. Wagner, and J. C. Sturm, "Highly stable amorphous-silicon thin-film transistors on clear plastic," *Applied Physics Letters,* vol. 93, Jul 21 2008.

[3] B. Hekmatshoar, S. Wagner, and J. C. Sturm, "Tradeoff regimes of lifetime in amorphous silicon thin-film transistors and a universal lifetime comparison framework," *Applied Physics Letters,* vol. 95, Oct 5 2009.

[4] K. S. Karim, A. Nathan, M. Hack, and W. I. Milne, "Drain-bias dependence of threshold voltage stability of amorphous silicon TFTs," *Ieee Electron Device Letters,* vol. 25, pp. 188-190, Apr 2004.

[5] M. J. Powell, C. Vanberkel, A. R. Franklin, S. C. Deane, and W. I. Milne, "Defect Pool in Amorphous-Silicon Thin-Film Transistors," *Physical Review B,* vol. 45, pp. 4160-4170, Feb 15 1992.

[6] M. J. Powell, C. Vanberkel, and I. D. French, "The Resolution of a-Si Thin-Film Transistor Instability Mechanisms," *Journal of Non-Crystalline Solids,* vol. 97-8, pp. 321-324, Dec 1987.

[7] A. V. Gelatos and J. Kanicki, "Bias Stress-Induced Instabilities in Amorphous-Silicon Nitride Hydrogenated Amorphous-Silicon Structures - Is the Carrier-Induced Defect Creation Model Correct," *Applied Physics Letters,* vol. 57, pp. 1197-1199, Sep 17 1990.

[8] N. B. Goodman and H. Fritzsche, "Analysis of Field-Effect and Capacitance-Voltage Measurements in Amorphous-Semiconductors," *Philosophical Magazine B-Physics of Condensed Matter Statistical Mechanics Electronic Optical and Magnetic Properties,* vol. 42, pp. 149-165, 1980.

[9] T. Suzuki, Y. Osaka, and M. Hirose, "Theoretical Interpretations of the Gap State Density Determined from the Field-Effect and Capacitance-Voltage Characteristics of Amorphous-Semiconductors," *Japanese Journal of Applied Physics Part 2-Letters,* vol. 21, pp. L159-L161, 1982.

[10] G. Fortunato and P. Migliorato, "Determination of Gap State Density in Polycrystalline Silicon by Field-Effect Conductance," *Applied Physics Letters,* vol. 49, pp. 1025-1027, Oct 20 1986.

[11] M. H. Lee and K. J. Chen, "The fabrication and the reliability of poly-Si MOSFETs using ultra-thin high-K/metal-gate stack," *Solid-State Electronics,* vol. 79, pp. 244-247, Jan 2013.

[12] T. NODA, Y. OGAWA, and T. KUROBE, "Some Consideration on Calculation of the Localized State Distribution in GD a-Si," *Ieice Transactions on Communications Electronics Information and Systems,* vol. E64, p. 7, 1981.

[13] M. S. Shur, H. C. Slade, M. D. Jacunski, A. A. Owusu, and T. Ytterdal, "SPICE models for amorphous silicon and polysilicon thin film transistors," *Journal of the Electrochemical Society,* vol. 144, pp. 2833-2839, Aug 1997.

[14] E. A. Davis and N. F. Mott, "Conduction in Non-Crystalline Systems .5. Conductivity, Optical Absorption and Photoconductivity in Amorphous Semiconductors," *Philosophical Magazine,* vol. 22, pp. 903-&, 1970.

[15] K. Winer and L. Ley, "Surface-States and the Exponential Valence-Band Tail in Alpha-Si-H," *Physical Review B,* vol. 36, pp. 6072-6078, Oct 15 1987.

[16] T. Tiedje, J. M. Cebulka, D. L. Morel, and B. Abeles, "Evidence for Exponential Band Tails in Amorphous-Silicon Hydride," *Physical Review Letters,* vol. 46, pp. 1425-1428, 1981.

[17] R. A. Street, C. C. Tsai, J. Kakalios, and W. B. Jackson, "Hydrogen Diffusion in Amorphous-Silicon," *Philosophical Magazine B-Physics of Condensed Matter Statistical Mechanics Electronic Optical and Magnetic Properties,* vol. 56, pp. 305-320, Sep 1987.

[18] N. B. Goodman, H. Fritzsche, and H. Ozaki, "Determination of the Density of States of a-Si-H Using the Field-Effect," *Journal of Non-Crystalline Solids,* vol. 35-6, pp. 599-604, 1980.

[19] A. Madan, P. G. Lecomber, and W. E. Spear, "Investigation of Density of Localized States in a-Si Using Field-Effect Technique," *Journal of Non-Crystalline Solids,* vol. 20, pp. 239-257, 1976.

Drain-Bias Dependence of Drain Current Degradation

In Chapter 5, by optimizing the deposition conditions of the gate SiN_x and a-Si, the 50% lifetime of the a-Si TFT drain current at room temperature has been improved to 4.4×10^7 sec (1.4 years). One important possible future application of the stable a-Si TFTs would be to drive OLEDs in flat panel displays [1, 2]. In this case a-Si TFTs are usually biased in saturation operating as a current source. Most studies of the instability of a-Si TFTs under low-gate field, including the two-stage model in Chapter 4, ignore the effect of drain bias and assume a uniform channel condition under gate field [1-5]. Some reports [6-9] concerning the effect of drain bias proposed a channel average threshold voltage shift, which is the threshold voltage shift without drain bias scaled down by the ratio of the number of channel charges with drain bias to that without drain bias. The scale-down was explained by the defect pool model [10], which suggests that the amount of defects created is proportional to the number of channel electrons. However, because the number of channel charges also depends on the threshold voltage shift, the channel average threshold voltage shift only approximates the actual threshold voltage shift measured in experiment [7]. Furthermore, the direct relation between drain current degradation and drain-bias has not been reported.

Based on the physical mechanism of defect creation in a-Si, this chapter first derives a differential equation for the threshold voltage shift rates in a-Si TFTs with drain-bias. The drain current is related to the threshold voltage with the gradual-channel approximation model. The threshold voltage along the channel and the drain current degradation can be numerically simulated. Then an analytical expression for the drain current degradation will be given and proved. The analytical solution agrees well with the numerical simulation and experimental results of drain current degradation of a-Si TFTs in the linear regime and in saturation. The drain current degradation vs. time is independent of drain-bias. Since defect creation in a-Si is the dominant instability mechanism of a-Si TFTs under low-gate field, the analytical method provides an easy model to characterize the stability of driver TFTs in AMOLED pixels. Finally, the analytical expression for the drain current degradation is compared with the expression in Chapter 4 derived without considering the drain-bias.

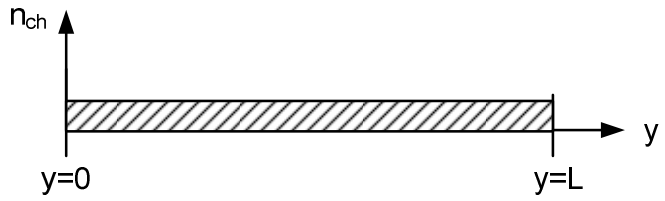
7.1. *Modeling of threshold voltage shift with drain-bias*

As discussed in Chapter 4, at the low-gate fields ($\leq 1.5 \times 10^5$ V) appropriate for driving OLEDs, defect creation in a-Si is the dominant mechanism for threshold voltage instability. Defect creation is a thermally activated process of weak bond breaking into dangling bonds. Assuming the defect creation rate is proportional to the number of channel electrons per unit volume n_{ch} [11, 12], the defect creation rate has been shown in Chapter 4 to be

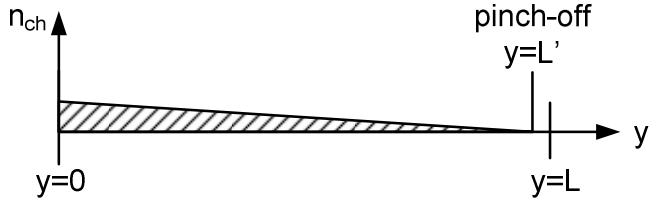
$$\frac{\mathrm{d}N_B(t)}{\mathrm{d}t} = C_1 n_{ch}(t) kT\nu(\nu t)^{T/T_0-1} \qquad (7.\ 1)$$

$N_B(t)$ is the number of broken bonds per unit volume, and C_1 is a constant.

For the a-Si TFTs under constant gate-source bias V_{GS} and drain-source bias V_{DS} , n_{ch} is not uniform from source to drain as shown in Fig. 7.1.



(a) $V_{DS} \ll V_{GS} - V_T$



(b) $V_{DS} \geq V_{GS} - V_T$

Fig. 7.1. Drain-bias effects on the distribution channel electrons (a) TFT operated in the linear region (very low drain Voltage). (b) TFT operated in the saturation region. The pinch-off point is indicated by L'.

The position $y = 0$ is the source, and $y = L$ is the drain. As a result, the density of broken bonds is not uniform along the channel.

The local electron density is given by

$$\int n_{ch}(y,t)\mathrm{d}x = C_{ins}[V_{GS} - V_T(y,t) - V_{ch}(y,t)]/q \qquad (7.\ 2)$$

The integration is over the channel thickness x, $V_T(y,t)$ is threshold voltage at position y and time t, and $V_{ch}(y,t)$ is the voltage profile in the channel at time t.

Because dangling bonds will capture channel electrons and raise the threshold voltage, the threshold voltage can be related to the number of broken bonds with

$$V_T(y,t) = q\int N_B(y,t)\mathrm{d}x\,/C_{ins} \qquad (7.\ 3)$$

C_{ins} is the capacitance of the gate SiN_x.

Thus, the threshold voltage shift can be modeled with a differential equation

$$\frac{\partial V_T(y,t)}{\partial t} = C_1[V_{GS} - V_T(y,t) - V_{ch}(y,t)]kT\nu(\nu t)^{T/T_0-1} \qquad (7.\ 4)$$

If we define "activation energy" $E_{act} \equiv -kT_0\ln(C_1kT_0)$, (7. 4) becomes

$$\frac{\partial V_T(y,t)}{\partial t} = [V_{GS} - V_T(y,t) - V_{ch}(y,t)]\frac{\beta}{t_0}\left(\frac{t}{t_0}\right)^{\beta-1} \qquad (7.\ 5)$$

with

$$t_0 = \nu^{-1}\exp\left(E_{act}/kT\right) \qquad (7.\ 6)$$

and

$$\beta = T/T_0 \qquad (7.\ 7)$$

Equation (7. 5) gives the rate of threshold voltage shift at position y, which depends on the voltage $V_{ch}(y,t)$ in the channel.

7.2. *Numerical simulation of drain current degradation*

With the gradual-channel approximation [13] by assuming the voltage varies gradually along the channel, the drain current can be related to the voltage along channel by

$$I_D(t) = WQ_n(y,t)\mu_n \frac{\partial V_{ch}(y,t)}{\partial y} \qquad (7.\ 8)$$

W is the channel width and μ_n is the electron field mobility. $Q_n(y,t)$ is the charge per unit area at the position y (Fig. 7.1), which from (7. 2) can be written as

$$Q_n(y,t) = C_{ins}[V_{GS} - V_T(y,t) - V_{ch}(y,t)] \qquad (7.\ 9)$$

Now we consider the boundary conditions. At time $t = 0$, $V_T(y, t = 0) = V_{T0}$. The initial drain current at $t = 0$ can be solved from (7. 8) for TFTs operating in the linear regime and in the saturation regime as

$$I_D(t=0) = \begin{cases} \mu_n C_{ins} \frac{W}{L}\left[\left(V_{GS} - V_{T0} - \frac{1}{2}V_{DS}\right)V_{DS}\right], & V_{DS} < V_{GS} - V_{T0} \\ \mu_n C_{ins} \frac{W}{2L}[(V_{GS} - V_{T0})^2], & V_{DS} \geq V_{GS} - V_{T0} \end{cases} \qquad (7.\ 10)$$

At the source $y = 0$, the channel voltage

$$V_{ch}(y = 0, t) = 0 \qquad (7.\ 11)$$

For the TFTs operating in the linear regime, channel voltage at the drain $y = L$ is

$$V(y = L, t) = V_{DS} \qquad (7.\ 12)$$

For the TFTs operating in saturation, if the drain voltage does not exceeds $V_{GS} - V_T$ too much, we have $L \approx L'$ for the long channel TFTs. Thus channel voltage at the drain $y = L$ is

$$V_{ch}(y = L, t) = V_{GS} - V_T(y = L, t) \qquad (7.\ 13)$$

With the boundary conditions (7. 10) - (7. 13), $V_T(y,t)$, $V_{ch}(\mathrm{y},\mathrm{t})$ and $I_D(t)$ can be obtained by solving the differential equation set (7. 5) and (7. 8) numerically in the finite difference scheme, which replaces the derivatives with finite differences. In forward finite difference scheme, (7. 5) and (7. 8) become (7. 14) and (7. 15), respectively.

$$\frac{V_T(y_n, t_{m+1}) - V_T(y_n, t_m)}{\Delta t} = [V_{GS} - V_T(y_n, t_m) - V_{ch}(y_n, t_m)]\frac{\beta}{t_0}\left(\frac{t_m}{t_0}\right)^{\beta-1} \qquad (7.\ 14)$$

$$I_D(t_m) = WC_{ins}[V_{GS} - V_T(y_n, t_m) - V_{ch}(y_n, t_m)]\mu_n \frac{V_{ch}(y_{n+1}, t_m) - V_{ch}(y_n, t_m)}{\Delta y} \qquad (7.\ 15)$$

The numerical simulation can be carried out in the following steps,

1. Starting from t = 0, with the boundary conditions for $I_D(t=0)$ in (7. 10) and $V_T(y, t=0) = V_{T0}$, $V_{ch}(y, t=0)$ can be obtained from (7. 15);
2. Using (7. 14), $V_T(y, t_1)$ can be solved with the obtained $V_{ch}(y, t=0)$ from step 1;
3. Combining $V_T(y, t_1)$ from step 2 and boundary conditions in (7. 11) - (7. 13), we can solve $I_D(t_1)$ and $V_{ch}(y, t_1)$ numerically from (7. 15);
4. Repeat step 2 and step 3 to find $V_T(y, t_m)$, $I_D(t_m)$ and $V_{ch}(y, t_m)$ step by step in the time scheme.

Simulation results will be shown in Section 7.4 in comparison with analytical solutions and experimental results.

7.3. *Analytical solution of drain current degradation*

We have shown that the drain current degradation for the a-Si TFTs with drain-bias under low-gate field can be solved numerically. However, an analytical solution is still appealing due to its simplicity. We will show below that an analytical solution for drain current degradation can be derived in closed form for the a-Si TFTs with drain-bias.

To obtain the analytical solution, we first make an assumption that the voltage at a position y in the channel $V_{ch}(y,t)$ does not change with time, i.e. $V_{ch}(y,t) = V_{ch}(y,t=0) = V_{ch}(y)$. The validation of this assumption will be discussed at the end of this section.

With the assumption $V_{ch}(y,t) = V_{ch}(y)$, the differential equation (7. 5) has a solution in a closed form

$$V_T(y,t) = V_{T0} + [V_{GS} - V_{T0} - V_{ch}(y)]\left\{1 - \exp\left[-\left(\frac{t}{t_0}\right)^{\beta}\right]\right\} \qquad (7.\ 16)$$

For TFTs operating in the linear region, substituting (7. 9) into (7. 8) and integrating along the channel from the source $y = 0$ (with $V_{ch}(y=0) = 0$) to the drain $y = L$ (with $V_{ch}(y=L) = V_{DS}$), we have

$$\int_0^L I_D(t)\, dy = \mu_n W C_{ins} \int_0^{V_{DS}} [V_{GS} - V_T(y,t) - V_{ch}(y)]\mathrm{d}V \qquad (7.\ 17)$$

Substituting (7. 16) into (7. 17)

$$I_D(t)L = \mu_n W C_{ins} \int_0^{V_{DS}} [V_{GS} - V_{T0} - V_{ch}(y)] \exp\left[-\left(\frac{t}{t_0}\right)^{\beta}\right] \mathrm{d}V$$

$$= \mu_n C_{ins} W \left[\left(V_{GS} - V_{T0} - \frac{1}{2}V_{DS}\right)V_{DS}\right] \exp\left[-\left(\frac{t}{t_0}\right)^{\beta}\right]$$

Thus,

$$I_{D,lin}(t) = \mu_n C_{ins} \frac{W}{L}\left[\left(V_{GS} - V_{T0} - \frac{1}{2}V_{DS}\right)V_{DS}\right] \exp\left[-\left(\frac{t}{t_0}\right)^{\beta}\right] \qquad (7.\ 18)$$

For TFTs operating in saturation, because there are no channel electrons at the drain, the threshold voltage at the drain will not shift with time, i.e. $V_T(y = L, t) = V_{T0}$. The drain current can be obtained by substituting $V_{DS} = V_{GS} - V_{T0}$ into (7. 18)

$$I_{D,sat}(t) = \mu_n C_{ins} \frac{W}{2L}[(V_{GS} - V_{T0})^2] \exp\left[-\left(\frac{t}{t_0}\right)^{\beta}\right] \qquad (7.\ 19)$$

It is interesting to note that the normalized drain current degradation $I_{D,nor}(t) = I_D(t)/I_D(t = 0)$ for TFTs operating in both linear region and saturation region has the expression

$$I_{D,nor}(t) = \exp\left[-\left(\frac{t}{t_0}\right)^{\beta}\right] \qquad (7.\ 20)$$

$t_0 = \nu^{-1}\exp(E_{act}/kT)$ as in (7. 6) and $\beta = T/T_0$ as in (7. 7).

Up to this point we have derived an analytical solution for drain current degradation without changing the channel voltage profile $V_{ch}(y, t)$. Therefore, the assumption of $V_{ch}(y, t) = V_{ch}(y)$ is valid.

7.4. *Experimental and modeling results*

The a-Si TFTs in our experiment are on the dry-etched sample #8 in Table 5-IV. We biased an a-Si TFT with a constant gate voltage of 5V (a gate field of ~1.5×10^5 V/cm) and a constant drain voltage of 0.1V in the linear regime. As a comparison, we biased another a-Si TFT with the same constant gate voltage of 5V and a drain voltage of 7.5V in saturation. Drain current was measured with a-Si TFTs maintained at 80°C and 120°C. The a-Si TFTs in stress measurements

have W/L = 150µm / 20µm. The experimental data of normalized drain current $I_{D,nor}(t)$ in function of stress time are shown in Fig. 7.2.

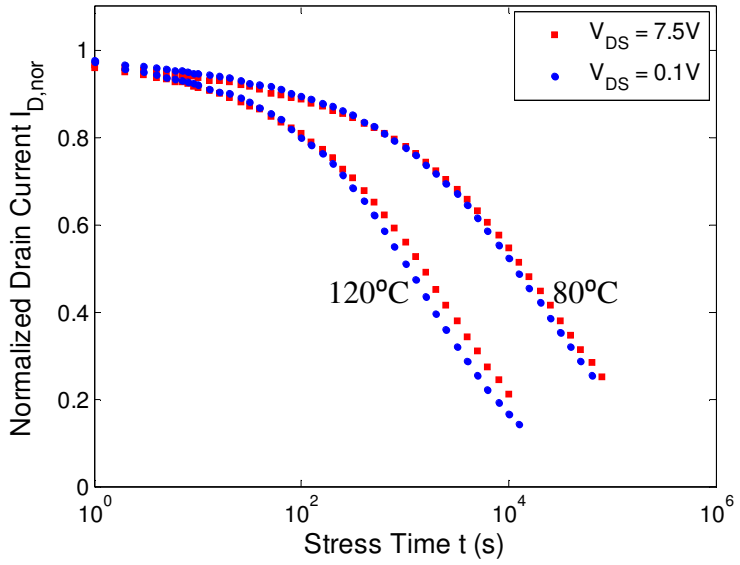


Fig. 7.2. The experimental data of normalized drain current as a function of stress time. Blue dots are measured in the linear regime and red dots are measured in saturation.

Blue dots are measured in the linear regime and red dots are measured in saturation. From Fig. 7.2, we can see that the normalized drain currents for TFTs operating both in the linear regime and in saturation degrade at the similar rate at 80°C and 120°C. This agrees with the analysis in Section 7.3.

Using (7. 20) to analytically fit the experimental data, we obtain the three fitting parameters ν = 5×10^5 Hz, T_0 = 964K, and E_{act} = 0.72 eV, i.e. the analytical fittings to experimental data are shown with blue curve in Fig. 7.3. The fitting parameters attempt-to-escape frequency ν and the characteristic temperature T_0 are the same as those for sample #14 in Table 5-IV in Chapter 5, but the activation energy E_{act} is different from 0.78 eV as in Table 5-IV. Further discussion will be made in Section 7.5.

Then we simulated the drain current degradation in saturation with the numerical method described in Section 7.2. Δy was chosen to be L/N and Δt was chosen to be non-uniform, with $t_{m+1} = t_m \times 10^{\Delta \log t}$. When N = 200 and $\Delta \log t$ = 0.001, the numerical results are plotted with

red curves in Fig. 7.3. The numerically results are very close to the analytical solutions. By decreasing the time step, the numerical results will further approach the analytical solutions.

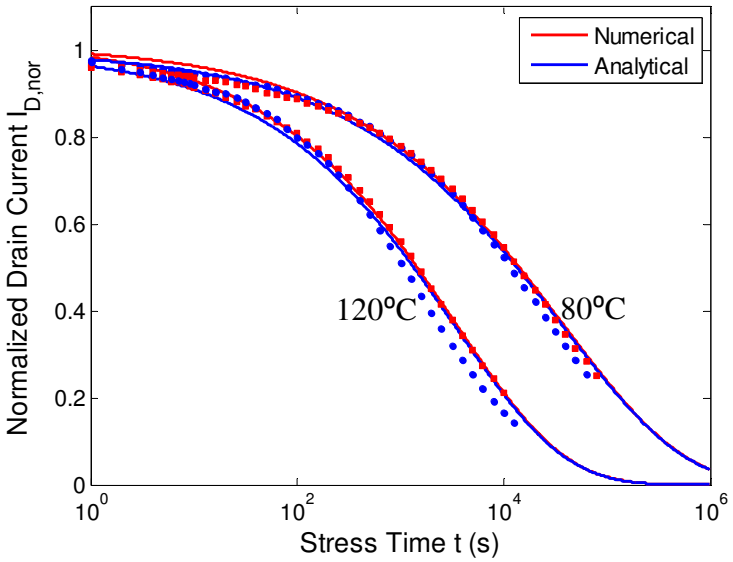


Fig. 7.3. Numerical and analytical solution to the normalized drain current degradation.

Fig. 7.4 illustrates the numerically calculated channel voltage profiles $V_{ch}(y,t)$ at $t = 0$ s, $t = 10^3$ s and $t = 10^4$ s for the a-Si TFT measured at 80°C.

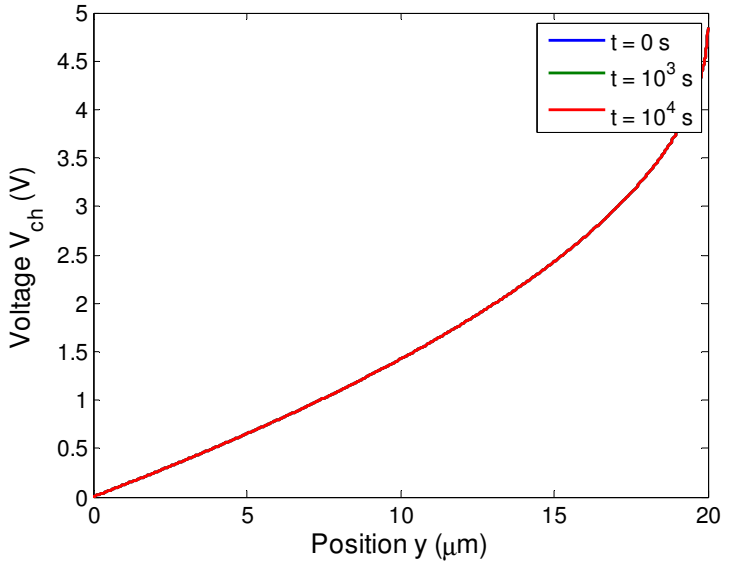


Fig. 7.4. Evolution of voltage at a position y in the channel $V_{ch}(y,t)$ with time for the a-Si TFT measured at 80°C.

The voltage profiles at three time points are the same and thus overlap each other. The results validate our assumption in Section 7.3 that voltage profile along the channel does not change with time, i.e. $V_{ch}(y,t) = V_{ch}(y)$.

When operating in saturation, the threshold voltage of a-Si TFTs is not uniform along the channel and the numerically solved non-uniform profiles of the threshold voltage at $t = 0$ s, $t = 10^3$ s and $t = 10^4$ s are shown in Fig. 7.5. The threshold voltage shift is fast near the source, and approaches zero near the drain.

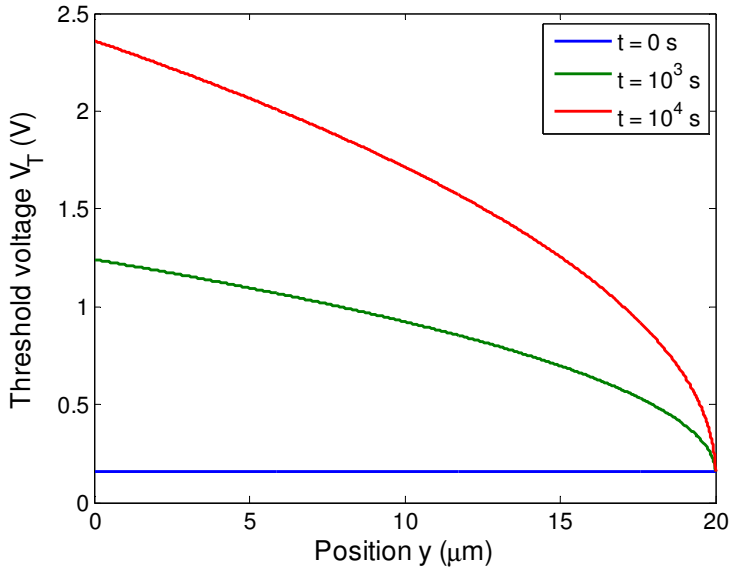


Fig. 7.5. Evolution of $V_T(y,t)$ with time for the a-Si TFT measured at 80^0C in saturation.

7.5. *Discussion*

In Chapter 4, for a-Si TFTs operating in saturation, the drain current degradation was modeled without the drain-bias effect by assuming a uniform channel condition. The drain current degradation also has a stretched exponential expression (4. 18). However, (7. 20) and (4. 18) are different in the exponent term by a factor of 2. The discrepancy in two models can be explained through comparisons made below.

7.5.1 *Very low drain-bias*

The threshold voltage shift is uniform along the channel. From the analysis in Section 7.3, we have

$$\Delta V_T(t) = (V_{GS} - V_{T0})\left\{1 - \exp\left[-\left(\frac{t}{t_0}\right)^{\beta}\right]\right\} \qquad (7.\ 21)$$

$$I_{D,nor}(t) = \exp\left[-\left(\frac{t}{t_0}\right)^{\beta}\right] \qquad (7.\ 22)$$

The threshold voltage shift vs time for the a-Si TFT stressed at 80^0C with $V_{GS} = 5$ V and $V_{DS} = 0.1$ V is shown in Fig. 7.6, with fitting parameters $t_0 = 3.7 \times 10^4$ s and $\beta = 0.37$.

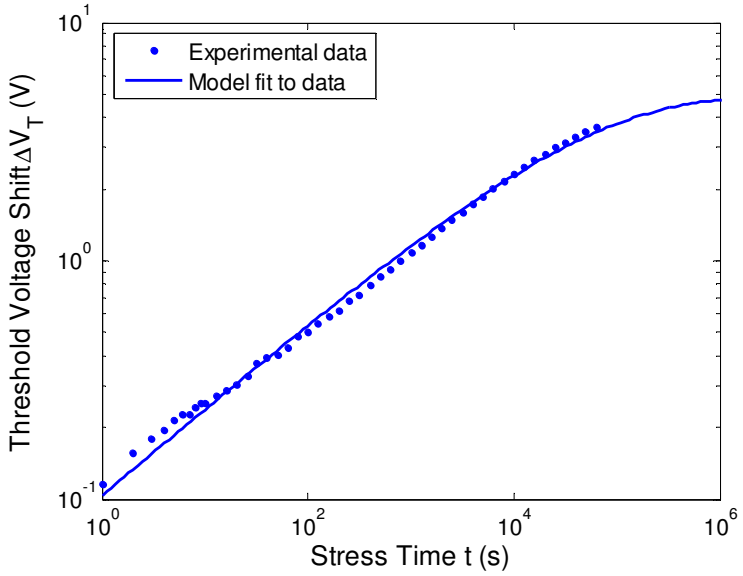


Fig. 7.6. Threshold voltage shift vs. time for the a-Si TFT stressed at 80^0C with $V_{GS} = 5$ V and $V_{DS} = 0.1$ V. Fitting parameters $t_0 = 3.7 \times 10^4$ s and $\beta = 0.37$.

7.5.2 *High drain-bias in saturation*

– **Non-uniform channel analysis**

The threshold voltage shift is not uniform along the channel. From the analysis in Section 7.3, we have

$$\Delta V_T(y,t) = [V_{GS} - V_{T0} - V_{ch}(y)]\left\{1 - \exp\left[-\left(\frac{t}{t_0}\right)^{\beta}\right]\right\} \quad (7.\ 23)$$

$$I_{D,nor}(t) = \exp\left[-\left(\frac{t}{t_0}\right)^{\beta}\right] \quad (7.\ 24)$$

The threshold voltage shifts at three positions along the channel are schematically shown in Fig. 7.7.

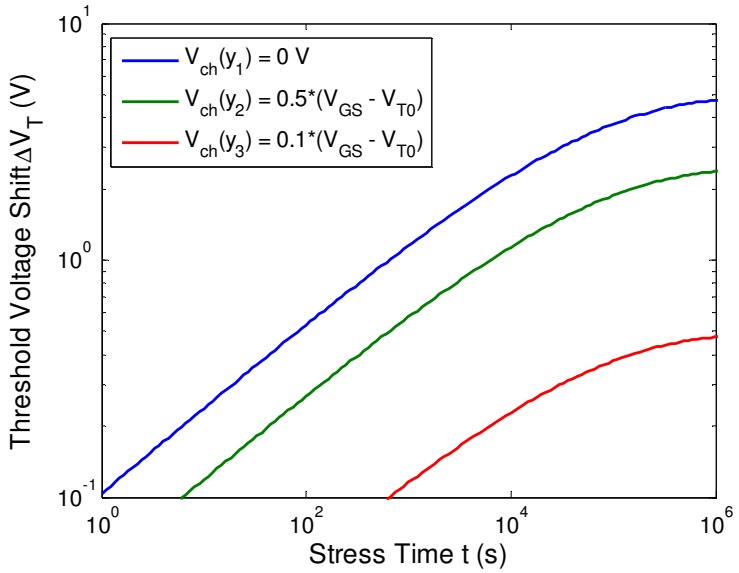


Fig. 7.7. Threshold voltage shifts vs. time in three positions along the channel for the a-Si TFT in saturation with $t_0 = 3.7 \times 10^4$ s and $\beta = 0.37$.

Position $y_1 = 0$ is at the source with $V_{ch}(y_1) = 0$ V, position y_2 is in the channel with $V_{ch}(y_2) = 0.5\ (V_{GS} - V_{T0})$, and position y_3 is close to the drain with $V_{ch}(y_3) = 0.1\ (V_{GS} - V_{T0})$. The threshold voltage shift saturates at a lower value along the channel from the source to drain, and it approaches zero near the drain, because there are few electrons there that induce defect creation.

– **Uniform channel analysis**

In Chapter 4, the drain-bias effects are ignored by assuming an effective uniform threshold voltage shift $\Delta V_{T,eff}$, which is related to the drain current with

$$I_D(t) = \frac{1}{2}\mu_n C_{ins}\frac{W}{L}[V_{GS} - (V_{T0} + \Delta V_{T,eff}(t))]^2 \quad (7.\ 25)$$

The effective threshold voltage shift $\Delta V_{T,eff}$ is modeled with the same stretched exponential expression as (7. 21)

$$\Delta V_{T,eff}(t) = (V_{GS} - V_{T0})\left\{1 - \exp\left[-\left(\frac{t}{t_{0,eff}}\right)^{\beta_{eff}}\right]\right\} \qquad (7.\ 26)$$

Combining (7. 25) and (7. 26), we obtain

$$I_{D,nor}(t) = \exp\left[-2\left(\frac{t}{t_{0,eff}}\right)^{\beta_{eff}}\right] \qquad (7.\ 27)$$

The threshold voltage shift for the a-Si TFT stressed at 80^{0}C with $V_{GS} = 5$ V and $V_{DS} = 7.5$ V is shown in Fig. 7.8, with fitting parameters $t_{0,eff} = 2.6 \times 10^5$ s and $\beta_{eff} = 0.37$.

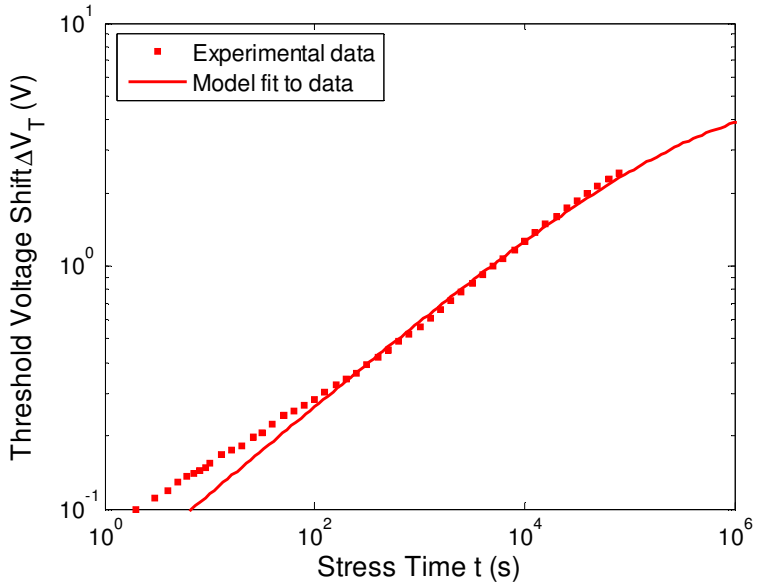


Fig. 7.8. Effective threshold voltage shift vs. time for the a-Si TFT stressed at 80^{0}C with $V_{GS} = 5$ V and $V_{DS} = 7.5$ V. Fitting parameters $t_{0,eff} = 2.6 \times 10^5$ s and $\beta_{eff} = 0.37$.

The effective threshold voltage shift is actually the averaged threshold voltage shifts along the channel in Fig. 7.7. By equating the right hands of (7. 24) and (7. 27), we find that

$$\beta_{eff} = \beta \qquad (7.\ 28)$$

$$t_{0,eff} = 2^{1/\beta} t_0 \qquad (7.\ 29)$$

The relations of (7. 28) and (7. 29) are verified in our experiments. For the a-Si TFT stressed at 80°C, results from the uniform and non-uniform analysis are summarized in Table 7-I. It shows that the extracted parameters $t_{0,eff}$ and β_{eff} from saturation region experiment in Fig. 7.8 are very close to those predicted with the relations (7. 28) and (7. 29).

Table 7-I. Relations between uniform and non-uniform analysis

Extraction of parameters from linear region experiment (Fig. 7.6)	Predicted parameters for $\Delta V_{T,eff}$ in saturation with (7. 28) and (7. 29)	Extraction of parameters from saturation region experiment (Fig. 7.8)
$t_0 = 3.7 \times 10^4$ s	$t_{0,eff} = 2.4 \times 10^5$ s	$t_{0,eff} = 2.6 \times 10^5$ s
$\beta = 0.37$	β_{eff} =0.37	β_{eff} =0.37

As discussed in Chapter 4 for the instability caused by defect creation in a-Si, the physical parameters are the characteristic temperature T_0, the attempt-to-escape frequency ν and the activation energy E_{act}. The characteristic temperature T_0 reflects the disorder of a-Si. The attempt-to-escape frequency ν is the prefactor for thermal activation process rate. Thus T_0 and ν are unrelated to the drain-bias. The effect of drain-bias is reflected in the activation energy E_{act}. In (4. 18), E_{act} is actually an effective activation energy (denote as $E_{act,eff}$), which is the activation energy E_{act} in (7. 20) scaled down by the non-uniform channel effect in saturation. The relation between E_{act} and E'_{act} can be found from (7. 29), and we have

$$E_{act,eff} = E_{act} + kT_0 \ln(2) \qquad (7.\ 30)$$

When $T_0 = 964$ K and $E_{act} = 0.72$ eV, $E_{act,eff} = 0.78$ eV, which is consistent with the result in Table 4-IV for sample #8. Thus, by neglecting the non-uniform channel condition in saturation, the stretched exponential drain current degradation in (4. 18) overestimates the activation energy, but it can be easily corrected with (7. 30). However, the unified stretched exponential model for defect creation in a-Si in Chapter 4 is still valid, because the attempt-to-escape frequency ν is independent of the drain-bias.

7.6. *Summary and conclusion*

We experimentally measured the drain current degradation of a-Si TFTs operating in the linear and saturation regions at 80°C and 120°C. Numerical simulation and analytical solution both agree well with the experimental data. It has been shown the normalized drain current degradation is independent of the drain-bias and can be modeled with a stretched exponential expression (7. 20) in a fairly simple closed form, which takes into the account that the local threshold voltage is changing at different rates in the channel at different places. The parameters extracted from experiment with very low drain-voltage can be used to predict the effective threshold voltage shift in saturation. This provides an easy method to characterize the stability of driver TFTs in AMOLED pixels.

References:

[1] B. Hekmatshoar, K. H. Cherenack, S. Wagner, and J. C. Sturm, "Amorphous silicon thin-film transistors with DC saturation current half-life of more than 100 years," in *Electron Devices Meeting, 2008. IEDM 2008. IEEE International*, 2008, pp. 1-4.

[2] B. Hekmatshoar, S. Wagner, and J. C. Sturm, "Tradeoff regimes of lifetime in amorphous silicon thin-film transistors and a universal lifetime comparison framework," *Applied Physics Letters,* vol. 95, Oct 5 2009.

[3] T. Liu, S. Wagner, and J. C. Sturm, "A new method for predicting the lifetime of highly stable amorphous-silicon thin-film transistors from accelerated tests," in *Reliability Physics Symposium (IRPS), 2011 IEEE International*, 2011, pp. 2E.3.1-2E.3.5.

[4] B. Hekmatshoar, K. H. Cherenack, A. Z. Kattamis, K. Long, S. Wagner, and J. C. Sturm, "Highly stable amorphous-silicon thin-film transistors on clear plastic," *Applied Physics Letters,* vol. 93, Jul 21 2008.

[5] C. C. Shih, Y. S. Lee, K. L. Fang, C. H. Chen, and F. Y. Gan, "A current estimation method for bias-temperature stress of a-Si TFT device," *Ieee Transactions on Device and Materials Reliability,* vol. 7, pp. 347-350, Jun 2007.

[6] K. S. Karim, A. Nathan, M. Hack, and W. I. Milne, "Drain-bias dependence of threshold voltage stability of amorphous silicon TFTs," *Ieee Electron Device Letters,* vol. 25, pp. 188-190, Apr 2004.

[7] Z. Tang, M. S. Park, S. H. Jin, and C. R. Wie, "Drain bias dependent bias temperature stress instability in a-Si:H TFT," *Solid-State Electronics,* vol. 53, pp. 225-233, Feb 2009.

[8] C. R. Wie and Z. Tang, "Non-uniform threshold voltage and non-saturating drain current in amorphous-Si TFT after saturation-mode bias temperature stress," in *Reliability Physics Symposium (IRPS), 2010 IEEE International*, 2010, pp. 347-353.

[9] C. R. Wie, Z. Tang, and M. S. Park, "Nonuniform threshold voltage profile in a-Si:H thin film transistor stressed under both gate and drain biases," *Journal of Applied Physics,* vol. 104, Dec 1 2008.

[10] M. J. Powell, C. Vanberkel, A. R. Franklin, S. C. Deane, and W. I. Milne, "Defect Pool in Amorphous-Silicon Thin-Film Transistors," *Physical Review B,* vol. 45, pp. 4160-4170, Feb 15 1992.

[11] R. S. Crandall, "Defect Relaxation in Amorphous-Silicon - Stretched Exponentials, the Meyer-Neldel Rule, and the Staebler-Wronski Effect," *Physical Review B,* vol. 43, pp. 4057-4070, Feb 15 1991.

[12] W. B. Jackson, J. M. Marshall, and M. D. Moyer, "Role of Hydrogen in the Formation of Metastable Defects in Hydrogenated Amorphous-Silicon," *Physical Review B,* vol. 39, pp. 1164-1179, Jan 15 1989.

[13] R. S. Muller, T. I. Kamins, and M. Chan, *Device electronics for integrated circuits*, 3rd ed. New York, NY: John Wiley & Sons, 2003.

3-TFT Highly Stable OLED Pixel Circuit with In-pixel Current Source

Active-matrix organic light-emitting diode (AMOLED) displays require highly-stable TFTs that operate in DC to provide constant current over time. The critical issue of stability limits the application of TFT technologies in AMOLEDs, such as the amorphous silicon (a-Si) TFTs [1]. In a traditional 2-TFT pixel circuit [2], the positive threshold voltage shift (ΔV_T) of the driving a-Si TFT under gate bias leads to reduced drain current and thereby reduced OLED brightness. Pixel circuits that can compensate for a threshold voltage shift have been introduced as an alternative method to overcome the instability issue of TFTs [3]. Current-programmed methods which use current input data are the one of major compensation methods [4, 5]. However, the current-programmed methods have the drawbacks of a long settling time at low data currents because of the parasitic capacitance of data lines and inconvenient constant current sources that control submicrometer ampere-level current in peripheral drivers [6]. Voltage-programmed methods proposed generally either require an excessive number of TFTs, or complex driving scheme.

This chapter presents a new 3-TFT voltage-programmed pixel circuit with an in-pixel current source. By using a TFT which operates at ~0.1% duty cycle to translate the programming voltage to a pixel current, the pixel current can be made largely insensitive to the threshold voltage shift of the driving TFT. Further, the new 3-TFT driving pixel with a-Si TFT technology is fabricated and characterized. Its dynamic range of driving current is greater than 100 under QVGA timing.

8.1. *Pixel circuit operation*

Fig. 8.1 illustrates the schematic circuit of the 3-TFT pixel circuit. This pixel circuit consists of a switching TFTs (T_1), a driving TFT (T_2), a programming TFT (T_3), a storage capacitor (C_s) and an OLED. The control signal lines are three row lines (V_{sel0}, V_{sel1} and V_{sel2}). The data line is the column line (V_{data}). The ground (GND) of the OLED is a blanket cathode shared by all the pixels.

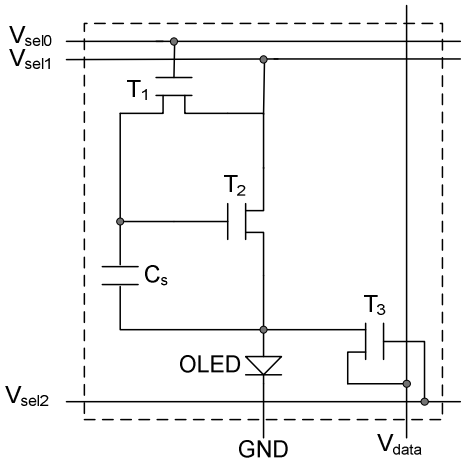
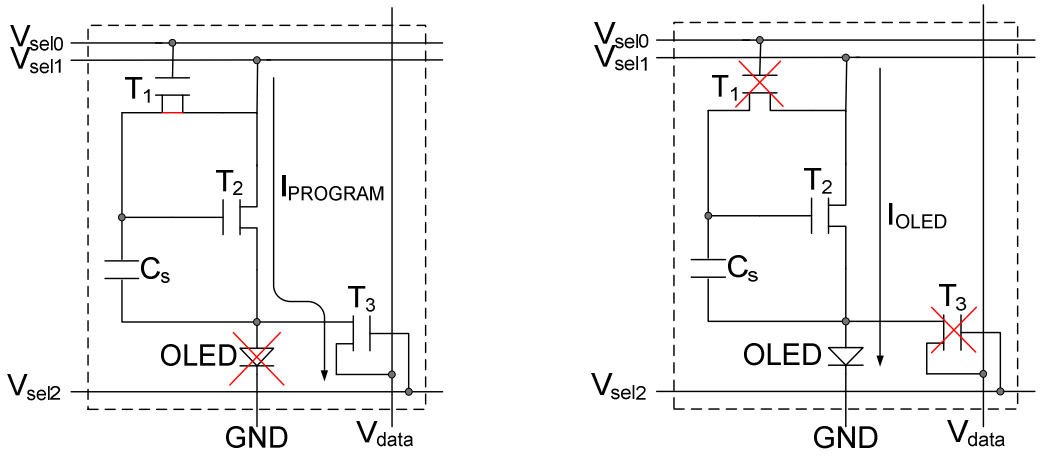


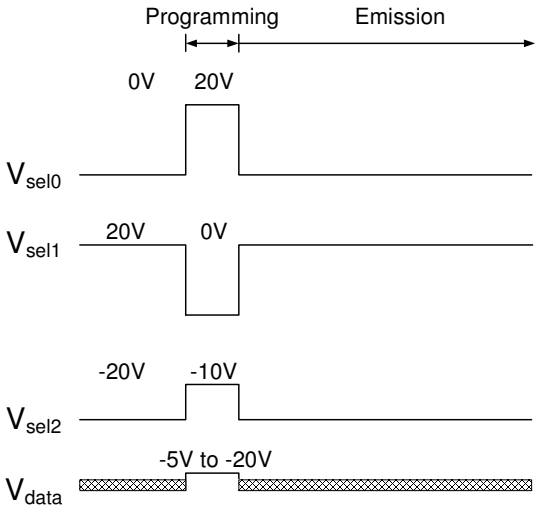
Fig. 8.1. Schematic pixel circuit.

During a frame time, the pixel operates in two modes – programming mode during the row time and emission mode otherwise. In the programming mode, V_{sel0} and V_{sel2} are set to high and V_{sel1} is set to low, so T_1 and T_3 are turned on. Since V_{sel0} is set to high, T_2 can be considered to be operating in diode mode with gate and drain connected through T_1. V_{sel1} is set to be low enough to ensure that OLED is reverse-biased and remains turned off during programming. The simplified circuit in programming mode can be shown as Fig. 8.2(a). T_3 is in saturation, acting as a local current source to set the pixel current in T_2 by its gate-source voltage, which is the voltage difference between V_{sel2} and V_{data}. The gate-source voltage V_{GS} of T_2 will adjust itself to mirror the current programmed into T_3, and the relevant V_{GS} of T_2 will be stored on capacitor C_s at the end of the programming cycle.

In the emission mode, V_{sel0} and V_{sel2} are set to low and V_{sel1} is set to high. T_1 is turned off to hold the gate-source voltage on OLED driver T_2. T_3 is also turned off so that the current supplied by T_2 flows through the OLED and controls its brightness. The simplified circuit in emission mode is shown as Fig. 8.2(b). Because the gate-source voltage V_{GS} of T_2 established during the programming mode can be held by C_s, the drain current passing through T_2 remains the same as that in the programming mode, if we ignore the channel length modulation effect. This effect is relevant because during programming the drain-source voltage of T_2 is equal to its gate-source voltage (at the onset of saturation), but during emission mode T_2 will be father into saturation with a higher drain voltage.



(a) programming mode (b) emission mode



(c) controlling signals

Fig. 8.2. Simplified circuits in programming mode and emission mode and controlling signals vs. time.

Note that T_2 is in DC operation providing current to the OLED during the emission mode, and hence prone to the threshold voltage shift. T_3, which converts the applied voltage ($V_{sel2} - V_{data}$) into the pixel current, is only positive-biased in programming mode at a low duty cycle (<0.1%), and its threshold voltage can recover during the emission mode. The threshold voltage of T_3 is expected to be far more stable than that of T_2. In the new 3-TFT pixel circuit, T_2 is effectively "current programmed" on each frame time, so that the pixel current is insensitive to the threshold

voltage shift of the driving TFT T_2. Thus the pixel should be highly stable compared to the conventional 2-TFT voltage-programmed pixel.

8.2. *Pixel circuit fabrication and characterization*

The pixel circuit was fabricated with standard back-channel passivated (BCP) a-Si TFT technology on a glass substrate in dry-etch process as described in Chapter 3. Typical isolated TFT transfer characteristics are demonstrated in Fig. 8.3. In the saturation regime, the threshold voltage is 0.4 V, the field-effect mobility is 0.9 $cm^2/V{\cdot}s$ and the subthreshold slope is 500 mV/dec.

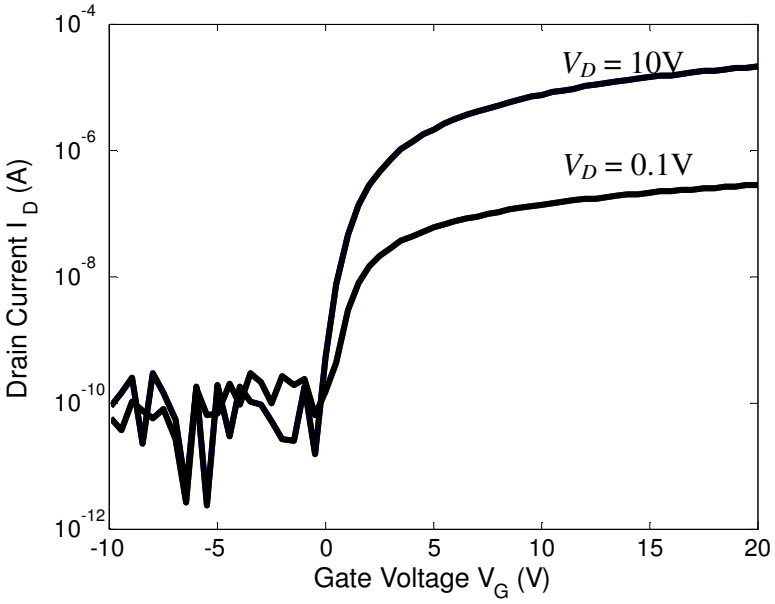
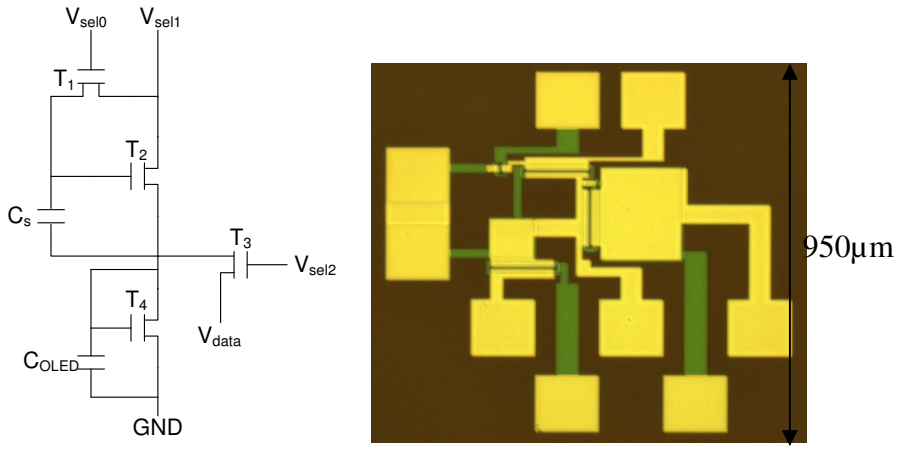


Fig. 8.3. Transfer characteristics of a typical isolated TFT with W/L = 150/15 µm.

For testing purposes, the OLED in the pixel circuit (Fig. 8.1) was replaced with a diode-connected TFT (T_4) in combination with a capacitor (C_{OLED}) in parallel as shown in Fig. 8.4.



(a) (b)

Fig. 8.4. (a) Schematic pixel circuit for fabrication; (b) micrograph of the fabricated 3-TFT pixel circuit.

The circuit design parameters are listed in Table 8-I. Large voltage swings (-10 V to 20 V) were used on the row lines to simplify testing – smaller swing would be used in practice.

Table 8-I. Circuit design and testing parameters

Name	**Value**
V_{sel0} (V)	0 to 20
V_{sel1} (V)	20 to 0
V_{sel2} (V)	-20 to -10
V_{data} (V)	-5 to -20
T_1 (W/L) (µm)	20/15
T_2 (W/L) (µm)	150/15
T_3 (W/L) (µm)	150/15
T_4 (W/L) (µm)	150/15
C_s (pF)	3.5
C_{OLED} (pF)	10

The DC operation of the pixel circuit in programming mode was confirmed by holding V_{sel0} = 0V, V_{sel1} = 20V, V_{sel2} = -10V. The programmed OLED current was measured as a function of V_{data} under DC and plotted with the blue curve in Fig. 8.5.

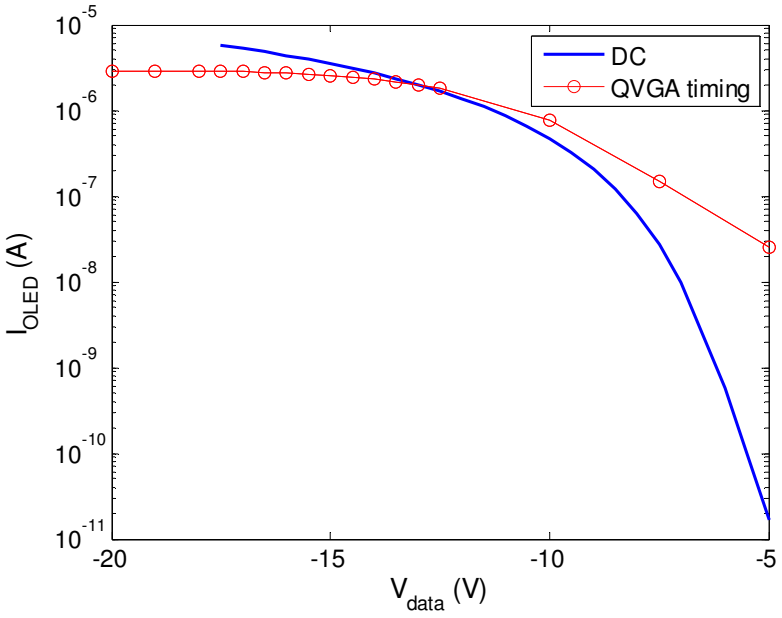


Fig. 8.5. OLED current vs. V_{data} in both DC and QVGA timing operation.

The exponential dependence of the programmed OLED current on V_{data} at high V_{data} range reflects the subthrehold operation of T_3. The slope of 600 mV/dec from Fig. 5 is in good qualitative agreement with that of the test TFT characteristics (500 mV/dec) shown in Fig. 8.3.

Under the typical display QVGA timing (50µs programming time and 16ms frame time) and V_{data} = -15 V, the OLED current was measured. The measured transient waveform is shown in Fig. 8.6. During the 16ms frame time, the OLED current holds at its programmed value 2.55 µA.

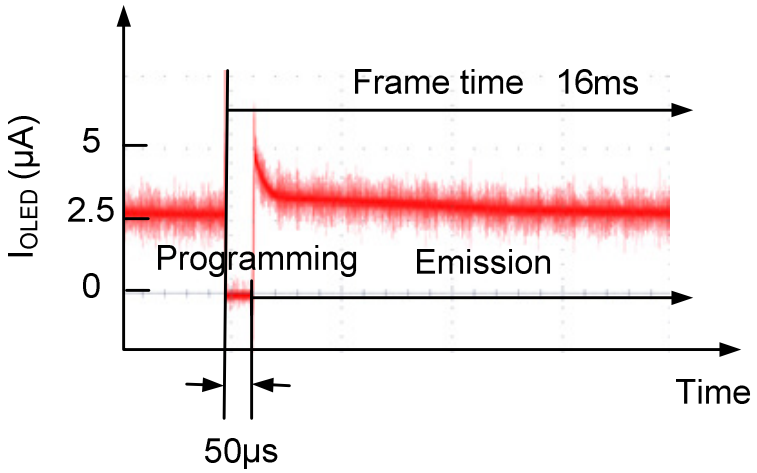


Fig. 8.6. Transient waveform of OLED current.

Under the same QVGA timing conditions, the OLED current in emission mode was also measured as a function of V_{data} (red circles in Fig. 8.5). Fig. 8.5 shows that the pixel circuit can provide OLED current ranging from 25 nA to 2.9 μA, which gives an on/off ratio of 116 at typical QVGA display timing. This is a very high dynamic range compared with typical current-programmed methods, which have limitations at low current level [6]. The settling time in conventional current-programmed pixel circuits, depends on the capacitance of the data line, which includes the gate-source/drain overlaps in all rows. In the new 3-TFT pixel circuit, the relevant capacitors are that of the OLED and the storage capacitor C_s, independent of the parasitic capacitance of data lines.

In Fig. 8.5, the current at QVGA timing is higher than that in DC for the low current range, in part because the gate-drain overlap capacitance of T_2 pulls up its gate voltage when V_{sel1} is set to high at the beginning of emission mode. Note that a high voltage supply range (0 V to 20 V) was used for V_{sel1} for simplified initial characterization of the circuit performance. With lower supply voltage range in practice in AMOLED displays, this effect should be reduced.

8.3. *Stability analysis and preliminary experimental results*

Ideally, without considering the channel length modulation and transient effect, any threshold voltage shift of T_2 does not affect the pixel current determined by the voltage difference between V_{sel2} and V_{data} in the programming mode. However, a-Si TFTs have a channel length

modulation effect, and the threshold voltage shift of T_2 affects the V_{DS} of T_2 and T_3, which leads to the programmed OLED current drop.

We modeled this effect with circuit simulator. The programmed OLED current drop was simulated as a function of the threshold voltage shift for T_2 with a channel length modulation coefficient of 0.01 for all the TFTs. In DC programming mode with $V_{sel0} = 0$V, $V_{sel1} = 20$ V, $V_{sel2} =$ -10 V and $V_{data} =$ -15 V, the programmed OLED current drop vs. ΔV_T of the driving TFT T_2 is demonstrated in Fig. 7, where the OLED current is normalized to the initial OLED current when ΔV_T is zero.

Fig. 8.7 suggests that the programmed OLED current drop is smaller than 5%, for a 5 V threshold voltage shift of the driving TFT T_2. Thus, the new 3-TFT voltage-programmed pixel circuit with in-pixel current source can be largely insensitive to the TFT threshold voltage shift.

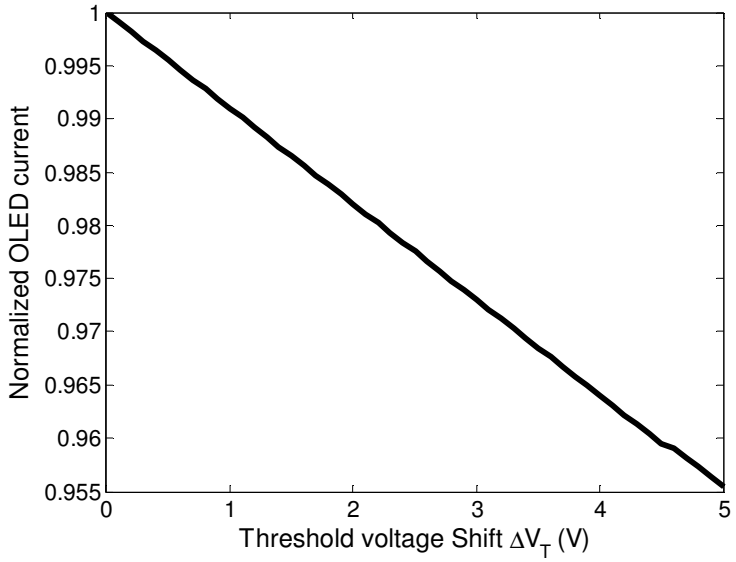


Fig. 8.7. Simulated OLED current drop vs. ΔV_T of driving TFT T_2.

We carried out preliminary lifetime tests on the 3-TFT pixel circuit with 16 ms frame time, 50 µs programming time and V_{data} = -15 V. The circuit was operating in air under room temperature. The drain current of T_2 in emission mode was monitored with time (red curve in Fig. 8.8). For comparison, the drain current degradation of an individual TFT on the same substrate was measured under constant V_{GS} = 5 V and V_{DS} = 7.5 V (blue curve in Fig. 8.8).

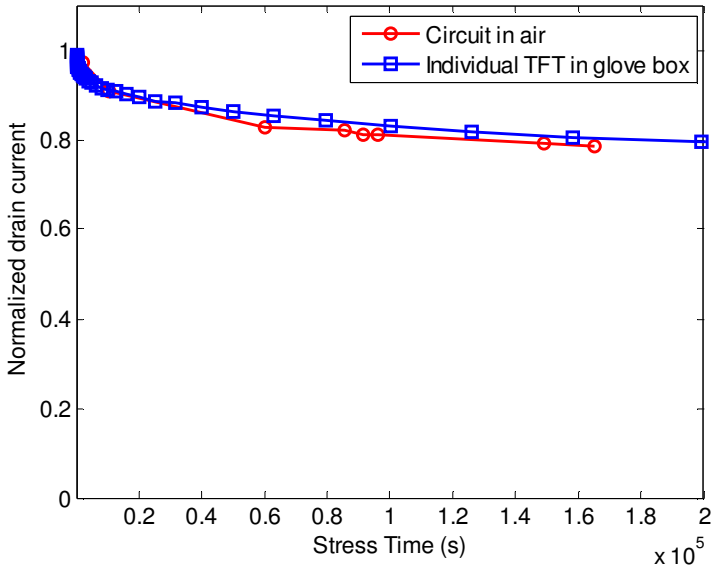


Fig. 8.8. Normalized drain current of T_2 in circuit and an individual TFT.

Preliminary lifetime tests of the new 3-TFT pixel circuit in air show a 20% drop of drain current in 46 hours, which is similar to drain current degradation of an individual TFT in glove box. This does not show the expected behavior for the circuit – we had expected the pixel current to degrade much slower than the individual TFT's. Besides the possible moisture effect, the faster drop of drain current in transient can be related to the time required to establish the voltage difference across C_s. When V_T increases, the required the voltage difference across C_s also increases, which makes the 50 µs programming time become insufficient. To overcome the transient effect, the storage capacitor of C_s needs to decrease.

8.4. *Summary and conclusion*

A new 3-TFT voltage-programmed pixel circuit with in-pixel current source was presented. The circuit combines the speed advantage of voltage-programming in large pixel arrays with the ability of current-programming to avoid OLED current drop due to the threshold voltage shift of driving TFTs. With 16ms frame time and 50 µs programming time, our experimental results show that the proposed pixel circuits can provide OLED current ranging from 25 nA to 2.9 µA, which gives an on/off ratio of 116 at typical QVGA display timing. Simulation suggests that the programmed OLED current drop should be smaller than 5%, for a 5 V threshold voltage shift of the driving TFT. Thus, the new pixel circuit can be largely insensitive to the TFT threshold

voltage shift. Improved design and fabrication of TFTs are required to optimize the performance of the new pixel circuit.

References:

[1] B. Hekmatshoar, K. H. Cherenack, A. Z. Kattamis, K. Long, S. Wagner, and J. C. Sturm, "Highly stable amorphous-silicon thin-film transistors on clear plastic," *Applied Physics Letters,* vol. 93, Jul 21 2008.

[2] R. M. A. Dawson, Z. Shen, D. A. Furst, S. Connor, J. Hsu, M. G. Kane, R. G. Stewart, A. Ipri, C. N. King, P. J. Green, R. T. Flegal, S. Pearson, W. A. Barrow, E. Dickey, K. Ping, S. Robinson, C. W. Tang, S. Van Slyke, F. Chen, J. Shi, M. H. Lu, and J. C. Sturm, "The impact of the transient response of organic light emitting diodes on the design of active matrix OLED displays," in *Electron Devices Meeting, 1998. IEDM '98. Technical Digest., International*, 1998, pp. 875-878.

[3] A. Nathan, G. R. Chaji, and S. J. Ashtiani, "Driving Schemes for a-Si and LTPS AMOLED Displays," *Journal of Display Technology,* vol. 1, pp. 267-277, Dec 2005.

[4] S. J. Ashtiani, P. Servati, D. Striakhilev, and A. Nathan, "A 3-TFT current-programmed pixel circuit for AMOLEDs," *Ieee Transactions on Electron Devices,* vol. 52, pp. 1514-1518, Jul 2005.

[5] Y. He, R. Hattori, and J. Kanicki, "Current-source a-Si : H thin-film transistor circuit for active-matrix organic light-emitting displays," *Ieee Electron Device Letters,* vol. 21, pp. 590-592, Dec 2000.

[6] C. L. Lin and T. T. Tsai, "A novel voltage driving method using 3-TFT pixel circuit for AMOLED," *Ieee Electron Device Letters,* vol. 28, pp. 489-491, Jun 2007.

Summary and Future Work

This chapter makes a summary and gives suggestions for future work.

9.1. *Summary*

While the a-Si TFT long been the workhorse in AMLCD industry, its stability issue questions its potential for further application in large area electronics, such as in AMOLED displays. The goal of this thesis is to comprehensively evaluate the stability of a-Si TFTs and their capability as current drivers in AMOLED pixels.

A two-stage model was developed to characterize the stability and predict the lifetime of a-Si TFTs under low-gate bias. Two stages of the threshold voltage shift were identified from the drain current degradation. Stage I can be measured in short time and modeled with the stretched exponential expression for charge trapping in the gate SiN_x. Long-term degradation in stage II can be greatly accelerated at high temperatures, and the unified stretched exponential fit for defect creation gives a good model to characterize stage II.

Then the two-stage model was applied to determine dependence of the a-Si TFT stability on the fabrication conditions. By optimizing the gate SiN_x and a-Si deposition conditions, the extrapolated 50% lifetime of the drain current under continuous operation has been raised from 3.3×10^4 sec (9.2 hours) to 4.4×10^7 sec (1.4 years). Etching is the most important post-deposition process that affects stability. A newly developed TFT fabrication process with four wet etch steps produces TFTs that are more stable than those processed with plasma etching.

Next, the two assumptions (1) defect creation in a-Si is the instability mechanism that dominates at low-gate field, and (2) the current degradation can be modeled without considering the drain bias effect, were proved to be valid when developing the two-stage model for lifetime prediction. The first assumption was investigated from the redistribution of the gap state density with the field effect technique. The second assumption was validated by analyzing the drain bias dependence both experimentally and theoretically.

Finally, a 3-TFT voltage-programmed pixel circuit for AMOLED displays with an in-pixel current source was presented. It can be largely insensitive to the TFT threshold voltage shift and promote the application of a-Si TFTs into the AMOLED displays.

9.2. *Future work*

The work in this thesis suggests the following areas that can be done in the future:

- Two-stage model applications

The two-stage model can be applied to TFTs fabricated with materials other than a-Si, such as organic materials and metal oxides, because the model was developed based on the physical properties of amorphous materials. Practically, the unified stretched exponential fit for degradation in Stage II can be easily adopted to characterize the thermally activated processes with distributed barrier energy / trapping parameters.

- Further fabrication condition optimization

It has been demonstrated that the extrapolated 50% lifetime of the TFT drain current at room temperature can be improved from 3.3×10^4 sec (9.2 hours) to 4.4×10^7 sec (1.4 years) by optimizing fabrication conditions. It makes the a-Si TFT a promising candidate in AMOLED display industry. However, there is still room for further improvement in stability. This can be achieved by matching the deposition conditions of SiN_x and a-Si, in terms of deposition temperature, gas flow rate, gas power, etc.

- Improving the deposition rate of thin films

Highly stable a-Si TFTs have relatively low growth rate in a-Si and SiN_x layer. The growth rate for good quality a-Si and SiN_x in this work is only about 3 – 5 nm / min. Because only the materials near the SiN_x / a-Si interface are important to the stability under low gate-field, the deposition rate can be accelerated simply by using a recipe with high growth rate for deposition more than ~20 nm away from the interface.

- Stability measurements on the 3-TFT voltage-programmed pixel circuit

Preliminary lifetime tests of the 3-TFT voltage-programmed pixel circuit show that the current provided by the circuit drops at a similar rate to that of the drain current degradation of an individual TFT in glove box. Further dynamic analysis and stability measurements are necessary for the real application of the proposed pixel circuit.

Publications and Presentations from Thesis Research

A.1. *Journal and conference publications*

[1] **T. Liu**, S. Wagner, and J. C. Sturm, “Highly stable amorphous-silicon thin-film transistors under low-gate field Stress – part I: two-Stage model for lifetime prediction,” IEEE Transactions on Electron Devices, to be submitted.

[2] **T. Liu**, S. Wagner, and J. C. Sturm, “Highly stable amorphous-silicon thin-film transistors under low-gate field Stress – part II: optimization of fabrication conditions,” IEEE Transactions on Electron Devices, to be submitted

[3] **T. Liu** and J. C. Sturm, “Drain-Bias dependence of drain current degradation of amorphous-silicon thin-film transistors under low-gate field”, under preparation

[4] **T. Liu**, S. Wagner, and J. C. Sturm, "Two-stage model for lifetime prediction of highly stable amorphous-silicon thin-film transistors under low-gate field," in Device Research Conference (DRC), 2012 70th Annual, 2012, pp. 245-246.

[5] **T. Liu** and J. C. Sturm, "3-TFT OLED Pixel Circuit for High Stability with In-pixel Current Source," SID Symposium Digest of Technical Papers, vol. 43, pp. 1101-1103, 2012.

[6] **T. Liu**, S. Wagner, and J. C. Sturm, "A new method for predicting the lifetime of highly stable amorphous-silicon thin-film transistors from accelerated tests," in Reliability Physics Symposium (IRPS), 2011 IEEE International, 2011, pp. 2E.3.1-2E.3.5.

[7] J. C. Sturm, Y. Huang, L. Han, **T. Liu**, B. Hekmatshoar, K. Cherenack, E. Lausecker, and S. Wagner, "Amorphous Silicon: The Other Silicon," in Ultimate Integration on Silicon (ULIS), 2011 12th International Conference on, 2011, pp. 1-4.

[8] N. Wook Jun, **T. Liu**, S. Wagner, and S. Fonash, "A study of lateral collection single junction A-SI:H solar cell devices using nano-scale columnar array," in Photovoltaic Specialists Conference (PVSC), 2010 35th IEEE, 2010, pp. 000923-000927.

[9] I. Chan, R. Cheng, H. C. Cheng, C. C Lee, **T. Liu**, B. Hekmatshoar, Y. Huang, S. Wagner, and J. C. Sturm, “Amorphous silicon thin-film transistors with low-stress silicon mitride for flexible display,” The International Conference on Flexible and Printed Electronics (ICFPE), 2010, S9-1-1

A.2. *Conference presentations*

[1] **T. Liu**, S. Wagner, J. C. Sturm, "Two-stage Model for Lifetime Prediction of Highly Stable Amorphous-Silicon Thin-Film Transistors under Low-Gate Field," IEEE Device Research Conference, University Park, PA, United States (2012).

[2] **T. Liu**, and J.C. Sturm, "3-TFT OLED Pixel Circuit for High Stability with In-pixel Current Source," the Society for Information Display, International Symp., Boston, MA, June (2012).

[3] **T. Liu**, S. Wagner, and J.C. Sturm, "Lifetime prediction of highly stable amorphous-silicon thin-film transistors by a unified stretched exponential model," Mat. Res. Soc. Spring Meeting, San Francisco, CA, April (2012).

[4] **T. Liu**, S. Wagner, J.C. Sturm, "A new method for predicting the lifetime of highly stable amorphous-silicon thin-film transistors from accelerated tests," IEEE International Reliability Phys. Symp., Monterey, CA, April (2011).

[5] **T. Liu**, S. Wagner, Isaac Chan, Ryan Cheng, Hua-Chi Cheng, Cheng-Chung Lee and J.C. Sturm, "Uniformity of highly stable wet-etched versus dry-etched amorphous silicon thin film transistors," Mat. Res. Soc. Spring Meeting, San Francisco, CA, April (2011).

[6] J. C. Sturm, Y. Huang, L. Han, **T. Liu**, B. Hekmatshoar, K. Cherenack, E. Lausecker, and S. Wagner, "Amorphous Silicon: The Other Silicon," Ultimate Integration on Silicon (ULIS) 2011, Cork, Ireland March (2011).

[7] **T. Liu**, W. J. Nam, S. J. Fonash, L. Han, J. Poirier, N. Yao, S. Wagner, "Growth morphology of two-phase silicon film on crystalline silicon nanowire substrates," Mat. Res. Soc. Spring Meeting, San Francisco, CA, April (2010).

[8] N. Wook Jun, **T. Liu**, S. Wagner, and S. Fonash, "A study of lateral collection single junction a-Si:H solar cell devices using nano-scale columnar array," 35th IEEE Photovoltaic Specialists Conference (PVSC), Honolulu, HI, June (2010).

[9] I. Chan, R. Cheng, H. C. Cheng, C. C Lee, **T. Liu**, B. Hekmatshoar, Y. Huang, S. Wagner, and J. C. Sturm, "Amorphous silicon thin-film transistors with low-stress silicon mitride for flexible display," The International Conference on Flexible and Printed Electronics (ICFPE), October (2010)

Appendix A: *Publications and Presentations*

Substrate temperature Calibration

The substrate temperature of a-Si TFTs deposited in Solarex / Innovative S900 plasma-enhanced chemical vapor deposition (PECVD) system was calibrated, with a thermal coupler clipped between two pieces of graphite in the position of substrate during deposition (Fig. B.1).

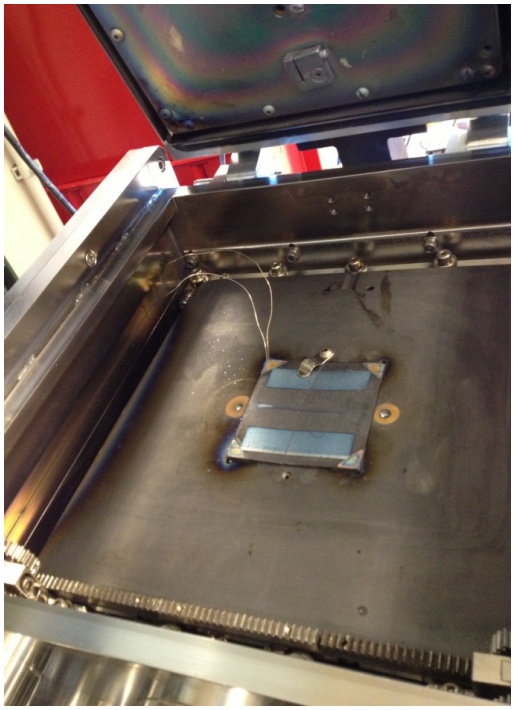


Fig. B.1. Substrate temperature calibration setup.

In each chamber, there are three heaters – two top heaters and one bottom heaters. Silicon nitride (SiN_x) was deposited in N-chamber and intrinsic amorphous silicon (a-Si) was deposited in I-chamber. The substrate temperature calibrations for N-chamber and I-chamber are shown in Table B-I and Table B-II, repectively. The actual substrate temperature is lower than the heater setting temperatures.

Table B-I. N-chamber substrate temperature calibration

Heater setting temperature (^{0}C)			Waiting time (min)	Substrate temperature (^{0}C)	Note: chamber condition
Left	**Right**	**Bottom**			
210	210	190	310	148.1	Vacuum
250	250	230	60	171.9	500 mTorr
280	280	250	40	190.3	500 mTorr
290	290	250	660	195.1	500 mTorr
290	290	260	220	214.3	Vacuum
350	350	325	710	272.8	Vacuum
			30	276.8	500 mTorr
400	400	350	70	318.7	500mTorr

Table B-II. I-chamber substrate temperature calibration

Heater setting temperature (^{0}C)			Waiting time (min)	Substrate temperature (^{0}C)	Note: chamber condition
Left	**Right**	**Bottom**			
200	200	200	140	160.8	Vacuum
250	250	230	60	200.7	500 mTorr
280	280	260	50	221.8	500 mTorr
350	350	320	60	278.8	500 mTorr
380	380	340	50	302.2	500 mTorr
			1010	311.7	Vacuum