BEAM PROCESSING OF SILICON WITH A SCANNING CW Hg LAMP

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ABSTRACT
A scanning arc lamp annealing system has been built using a 3" long mercury arc lamp with an elliptical reflector. The reflector focuses the light into a high intensity narrow line source. Silicon wafers implanted with 100 keV 75As+ to 1x10¹⁵ cm⁻² have been uniformly annealed with a single scan, resulting in complete activation and negligible redistribution of the implanted species. Using a scan rate of 1cm/s, entire 3" wafers have been annealed in less than 10 seconds with this system. The system has also been used to recrystallize thin films of polysilicon deposited on thermally grown silicon dioxide. The recrystallized films contain grains that are typically 0.5-1 mm in width and several centimeters long. Surface texture measurements show the crystallographic orientation, which is random in the plane of the film with the orthogonal <100> direction closely paralleling the scan direction. MOSFETs were fabricated in these films with surface mobilities 66% of ones fabricated in single crystal silicon. An epilayer on the same crystallographic features as the recrystallized film was grown on the film itself.

INTRODUCTION
Over the past few years a considerable amount of research has been directed towards developing alternative heat treatment techniques for application to semiconductor processing. The most thoroughly investigated of these has been the use of pulsed and CW laser and electron beams [1]. Work performed using these sources has provided new insights into the mechanisms of thermally induced processes such as solid phase and liquid phase epitaxial growth and thin film recrystallization. In particular, some of the earliest work demonstrated that ion implantation damaged silicon could be annealed with a scanned CW laser such that there was complete electrical activation of the implanted species and virtually no impurity redistribution [2]. In addition, laser recrystallization of fine grain or amorphous films on insulating substrates was found to significantly improve the electronic properties of the film itself [3]. Once these processes were observed and understood, work began to identify alternative beam sources for producing these effects. In this paper we describe the results of using a high pressure Hg arc lamp system for large area annealing of ion implanted crystalline silicon and zone recrystallization of silicon thin films on insulating substrates. We also present data obtained from MOSFETs fabricated in the zone recrystallized film as well as describe the crystallographic features of an epitaxial layer grown on the film itself.

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LING SYSTEM

have built an arc lamp annealing system which consists of a 3 inch long pressure mercury lamp, an elliptically shaped reflector and a variable translation hot stage. In previous work xenon and krypton lamps were
use. We chose to use a mercury lamp primarily for the following two reasons. Firstly, the spectral distribution of this lamp is most heavily weighted in the near ultraviolet region, the mean absorption depth for this source is much lower than that for the other lamps.

The second reason is that the mercury lamp was chosen over the other available lamps due to the narrow capillary used for containing the discharge. For example, a typical 3 inch krypton lamp has a 5 mm capillary whereas the mercury uses a 2 mm capillary. The tighter confinement results in a narrower beam, and thus yields a higher intensity at the sample surface for a given lamp power.

The light from the lamp is focused into a narrow (1 mm wide) ribbon by a parabolic reflector with an elliptical cross-section. By using this shape of reflector to collect and focus the light, we can create an intense linear source and still maintain a reasonable working distance between the lamp and the sample. The reflector in our system has major and minor axes of 0.5 and 1.0 cm respectively. This configuration gives a magnification of about 2.5 and a working distance of about 2.5 cm between the edge of the reflector and the focal plane.

These samples are placed on a heated sample stage, over which the lamp can translate at speeds up to 1 cm/s. A schematic representation of the arc lamp annealing system is shown in Fig. 1.

LAMP ANNEALING OF ION IMPLANTED CRYSTALLINE SILICON

Arc lamp annealing of ion implanted silicon has several distinct advantages over other techniques, in particular laser annealing. First, because the light is noncoherent, interference effects which result from the interaction of monochromatic light and the dielectric layers on the semiconductor material are eliminated. These effects can lead to nonuniform heating of the irradiated area if not eliminated. Second, the effective processing area for an arc lamp is orders of magnitude greater than that for a laser. For example, an arc lamp can be used in about 10 seconds, whereas a cw laser takes several minutes to process the same amount of material. Single scan-laser processing also eliminates the periodic nonuniformities observed in raster scanned laser annealed materials. Finally, an arc lamp is significantly less expensive than a laser and is much more efficient to use.

In the following section, we describe the results of using an arc lamp to anneal ion implanted silicon. We demonstrate that while it has the above advantages over conventional furnace annealing, it also provides the benefits of laser annealing, such as the high-quality, solid phase epitaxial regrowth with complete activation of the implant species and no dopant redistribution.

Annealing experiments were carried out using 2 and 3 inch 1-3 μm p-type (100) silicon wafers which were implanted with 75 keV at 100 keV to 1 x 10^15 cm^-2. It was found that several combinations of arc lamp power, scan rate and substrate temperature could be used to achieve a wafer temperature sufficient for good annealing, ~ 1000°C. In general, scan rates from 5 mm/s to 1 cm/s, substrate temperatures of 400°C to 600°C and arc lamp input power of 1 kW to 1.5 kW/inch gave good results.

Because of the length of the arc lamp, an entire wafer can be annealed in a single scan. Figure 2 is a photograph of a 3 inch wafer in which the scan was stopped at the center of the wafer. Because of the difference in reflectivities between single crystal and amorphous silicon, the demarcation between the annealed and unannealed regions is readily seen. Transmission electron microscope (TEM) diffraction patterns made from samples taken from the annealed and unannealed regions clearly indicate the amorphous and completely recrystallized nature of the regions, respectively. (The picture is somewhat distorted due to the angle at which the photo was taken.)

The recrystallized layer was also analyzed by Rutherford Backscattering Spectroscopy (RBS) and directly compared to a sample which was thermally annealed at 850°C for 30 minutes followed by a 10 second 1000°C anneal. Figure 3 shows the backscattering spectra from an as-implanted, arc lamp annealed and thermally annealed sample. As shown, there is no detectable difference between the quality of the regrown material annealed by the scanned arc lamp and the thermally processed sample.

Carrier concentration and mobility of the arc lamp annealed material as a function of depth were determined by means of differential sheet resistivity and Hall effect together with an anodic oxidation stripping technique. These
To assess the uniformity of the anneal, four point probe sheet resistivity measurements were made on a wafer which was completely annealed in a single scan. The variation across the wafer from side to side and top to bottom (with respect to the scanning beam) showed no significant variation in either direction, indicating a very uniform annealing of the implanted wafer. These data are shown in Fig. 5.

Fig. 5. Sheet resistivity profiles across an arc lamp annealed wafer.

High resolution transmission electron microscopy (TEM) was used to compare the residual dislocation density in arc lamp annealed material to material which was furnace annealed at 1000°C for 1 hour in N₂.

In Fig. 6 we compare the results of a sample which was annealed using 1 kW/inch lamp power, a scan rate of 7 mm/s and a substrate temperature of 450°C, to one which was thermally annealed. As shown the residual dislocation density is approximately the same in both cases.

Deep level transient spectroscopy has also been performed on these samples and compared to furnace annealed as well as other beam (e.g., laser and electron) annealed samples [4]. These results indicate that the arc lamp annealed material has approximately an order of magnitude lower defect density and does not contain the principle defect species identified in the other beam processed material.

Fig. 6. Bright field TEM micrographs of (a) furnace annealed (1000°C, 1 hr) and (b) arc lamp annealed samples.
CRYSTALLIZATION OF THIN POLYCRYSTALLINE Si ON SiO2

Fabrication of device-worthy silicon thin films on insulating substrates has been an area of research for many years. One approach for obtaining this material is by recrystallizing as-deposited thin films into large grain or single crystal material. Over 30 years ago, zone melting was shown to be an effective technique for obtaining single-crystal thin films [5]. In that work, a platinum wire was used to zone melt and recrystallize films of luminescent material on insulating substrates. By 1966, several researchers had grown large single-crystal germanium films using an electron beam for the zone melting process [6-9]. More recently, lasers [10,11] and graphite tip heaters have been used for zone annealing of silicon films [12-14].

In this section we show that a scanned, high pressure mercury lamp can be used for zone annealing and recrystallization of silicon thin films on insulating substrates. The samples used for these experiments were thermally oxidized silicon wafers on which polycrystalline films had been deposited from low pressure chemical vapor deposition (LPCVD). The thermal oxide was 200 nm thick and the deposited silicon film was 600 nm thick. Finally, the substrates were encapsulated with 1 um of CVD SiO2.

To control the zone melting process, parameters such as power and temperature were varied. The general observations were made. If the scan rate was too fast and/or the lamp power was too low, partial melting of the film and/or severe agglomeration occurred. If the scan rate was too slow and/or the lamp power was too high, melting of the underlying single-crystal substrate occurred. Finally, within the operating region of a stable molten zone, an increase in the scan rate was found to increase the spacing between the subgrain boundaries.

Our best results to date were obtained using a lamp power of 1 kW/inch, a substrate temperature of 1150°C and a scan rate of 3 mm/s. The following results were obtained under these experimental conditions.

The zone recrystallized films using our system exhibited features similar to those found in zone recrystallized films using other techniques. The films consisted of very large grains, typically 0.5 mm to 1 mm in width and up to several centimeters long. These large grains were obtained using any intentional seeding techniques. Such techniques have been shown to eliminate the angle grain boundaries and yield a film composed entirely of low angle grain boundaries [12].

The individual grains were composed of many subgrains, each having boundaries typically from 50 nm to 100 nm wide. The boundaries are generally straight and parallel to the original substrate surface. Figure 7 is a photomicrograph of a section of the recrystallized film which has been etched to delineate the subgrain boundaries. Figure 8 is a scanning electron micrograph of the film taken under channeling contrast conditions.

DEFECTS IN ZONE RECRYSTALLIZED FILM

The principal defects we have observed in the zone recrystallized film and/or substrates are: (1) slip and warpage, (2) substrate melt-through, (3) protrusions, (4) voids and (5) agglomeration or dewetting.
Slip and warpage damage to the single crystal silicon substrate are a result of the large thermal stresses the substrate sees during the processing. In general, higher substrate temperatures and very uniform substrate heating reduce stresses and eliminate these problems.

When the molten zone (or an area of it) becomes too hot, melting of the crystalline substrate beneath it can occur. Under these conditions the thermal oxide can rupture resulting in a large 'melt through' pit, where the surface film and substrate have fused together. This is shown in Fig. 10[d].

If the film to be recrystallized contains impurities, they can segregate to the sub-boundaries during the solidification process. This segregation will depress the melting temperature of the film in that region. Consequently, it will solidify after the zone front has passed that region and the neighboring film has solidified. Since silicon has a positive expansion coefficient upon solidification, these small molten areas which are constrained by the surrounding solid silicon must expand upward, resulting in small protrusions at the surface of the film. Figure 10(b) illustrates this case. Note how the protrusions all lie along the low angle grain boundaries. In general, clean material, reduced scan speeds and steep thermal gradients will prevent this defect.

We have also observed small areas in the zone recrystallized film where the film has thinned out and exposed the underlying thermal oxide. These 'voids' are believed to be a result of some local contamination at the interface between the oxide and the deposited film. Figure 10(c) is a photomicrograph of this defect. The last defect, agglomeration and dewetting is a gross feature which generally renders the film useless. This is the case when the film balls up or spheroids into separate unattached regions, as shown in Fig. 10(a). The driving force for this reaction is the minimizing of free energy by reducing the surface volume ratio of the film. The encapsulation layer is intended to minimize this effect. Some investigators have found that two layer encapsulants (18) are more effective than the single layer SiO₂. We have observed, however, that some deposited films are less prone to agglomeration than others and can be relatively insensitive to the encapsulant. In either case, this problem is perhaps the most demanding and the solution must be understood and universally reproducible if this process is to become a useful technique.

**Fig. 9.** Photomicrograph of zone recrystallized film illustrating misalignment of etch pits due to the presence of a grain boundary.

**Fig. 10.** Defects in zone recrystallized films (a) agglomeration, (b) protrusions, (c) voids, and (d) substrate melt through.

**MOSFETS IN ZONE RECRYSTALLIZED FILM**

In order to investigate the electronic properties of the zone recrystallized films, n-channel metal-oxide-semiconductor field-effect transistors were fabricated using an aluminum gate process. The transistors had channel lengths of 10 μm, 20 μm and 50 μm with all channel widths being 200 μm. The transistors were fabricated such that there were channels running both parallel and perpendicular to the low angle grain boundaries. In this way the effect of the low angle boundary orientation on the channel mobility could be assessed.

Channel implants of 1.5x10¹¹ cm⁻² boron and phosphorus were used for the enhancement and depletion mode devices, respectively. The implants were thermally annealed under such conditions as to insure a uniform dopant distribution through the film thickness, yielding a net impurity concentration of 2x10¹⁵ cm⁻³. The gate oxide thickness was 1000 Å and all devices were isolated by an island etch.

A circular bulk resistor pattern was also included to evaluate bulk properties of the film. Resistivity data obtained from these devices indicate that there was complete activation of the phosphorus implant and single crystal bulk mobilities in the film. Surface mobility data were obtained by analyzing transistor IV characteristics from a curve tracer. In Table I we summarize the surface mobility data obtained from the MOSFETS. As shown, the average
Table I

<table>
<thead>
<tr>
<th>Channel Length Direction</th>
<th>Enhancement</th>
<th>Depletion</th>
</tr>
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<tbody>
<tr>
<td>0 μm parallel</td>
<td>436</td>
<td>334</td>
</tr>
<tr>
<td>0 μm perpendicular</td>
<td>418</td>
<td>399</td>
</tr>
<tr>
<td>0 μm parallel</td>
<td>382</td>
<td>415</td>
</tr>
<tr>
<td>0 μm parallel</td>
<td>345</td>
<td>332</td>
</tr>
<tr>
<td>0 μm perpendicular</td>
<td>335</td>
<td>357</td>
</tr>
</tbody>
</table>

Inclusions: no sub-boundary orientation effects on surface mobility.

Surface mobilities for the enhancement and depletion mode devices in the zone recrystallized film ranged from 335 cm²/V-s to 436 cm²/V-s. No systematic variation due to low angle grain boundary orientation or channel length was observed. Included in Table I are the surface mobilities of enhancement mode devices simultaneously fabricated in single crystal material. The average mobility for these devices is 567 cm²/V-s. Thus the transistors fabricated in the recrystallized film had surface mobilities approximately 6% of those fabricated in single crystal material.

Fig. 11. Nomarski photomicrograph of surface of epitaxial layer grown on zone recrystallized film.

Fig. 12. 200 μm

Fig. 12. Recrystallized film from (a) epi on as-deposited film, (b) epi on zone recrystallized film.

Fig. 12. Recrystallized film from (a) epi on as-deposited film, (b) epi on zone recrystallized film.

Although 0.5 μm silicon films can be used for MOSFET devices, thicker films are desirable for bipolar applications. In light of this need, a 14 μm epitaxial layer was grown on a 0.5 μm zone recrystallized film. The sample separation and zone recrystallization were performed as described in the previous section. After processing, the 2 μm SiO₂ encapsulation layer was removed from the sample. The sample was then cleaned and placed in a standard conventional epitaxial reactor.

It was found that the epitaxial layer replicated and enhanced the surface features of the zone recrystallized film. In particular, the low single grain boundaries were clearly evident in the topography of the epitaxial layer. Fig. 11 is a Nomarski photomicrograph of the surface of the film illustrating these features. Diffraction patterns of epitaxial layers grown on as-deposited as well as zone recrystallized material were taken using a Recrystallized camera. These patterns, shown in Fig. 12, clearly indicate that while the layer grown on the as-deposited film is fine grained with no preferred orientation, the layer grown on the recrystallized film is large grained and highly oriented. In the latter to evaluate the macroscopic crystallographic features of the epitaxial layer, the preferential etch pit method previously described was used. These results are presented in Fig. 13. As shown, there are no facets in the etched pattern in the layer grown on the as-deposited film. However the etch pit pattern in the layer grown on the recrystallized film clearly indicates a 30° film orientation. The photomicrograph shown in the lower portion of Fig. 13 was taken using light scattered off the sample surface. All the etch pits within a single grain will have their facets aligned. This alignment never will vary from grain to grain. Thus this technique can be used to...
The recrystallized film had a (100) in plane orientation and exhibited a <100> texture in the direction of the zone scan. Enhancement and depletion m
MOSFETs were fabricated in the zone recrystallized film. The electron surfac
mobilities were greater than 65% of those measured in devices fabricated in
single crystal silicon, demonstrating that the electronic properties of the
film are suitable for device applications. Finally, a 14 mm epitaxial layer
was grown on a zone recrystallized film. This layer contained the same
crystallographic features as the zone recrystallized film used as a substrat
and has potential for bipolar device applications.

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ZONE-MELTING RECRYSTALLIZATION OF SEMICONDUCTOR FILMS

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ABSTRACT

The use of zone melting recrystallization (ZMR) to prepare large-grain (and in some cases single-crystal) semiconductor films is reviewed, with emphasis on recent work on Si on SiO.

Encapsulants are generally required to minimize contamination and decomposition, induce a crystalline texture, improve surface morphology and prevent agglomeration. In the case of Si, the solid-liquid interface is faceted, which gives rise to subboundaries. These can be entrained by laterally modulating the temperature through the use of an optical absorber on top of the encapsulant. Control of thermal gradients and in-plane crystallographic orientation are important for reliable entrainment.

Preparation of high-quality semiconductor films on insulating substrates has been the subject of numerous investigations. One of the more promising techniques for producing such films is zone-melting recrystallization (ZMR) which is accomplished by scanning a molten zone through the semiconductor film. The resulting film usually consists of large grains with a specific crystallographic texture, and has electrical properties approaching those of bulk single crystal material. In this article we review briefly the development of ZMR and discuss its application to Si on SiO.

The concept of ZMR was first discussed by Leff9 as a possible method for obtaining single-crystal films of ZnS. Mitchell9 et al. used a zone melting technique to produce single-crystal films of AgCl and AgBr. Later, ZMR was used to produce crystalline films of Ge, InSb and, in recent years, Si on SiO. Various methods have been used to produce the molten zone. For relatively low-melting-temperature materials, such as AgCl, AgBr and certain organics, a small hot plate, which was moved with respect to the substrate, was sufficient. Materials with higher melting temperatures, such as Si and Ge, require higher power densities, which can be obtained with electron or laser beams. If the substrate is heated to near the melting temperature of the semiconductor by some auxiliary means, a resistively heated wire or carbon rod, or a focused lamp, can be used to supply the additional heat necessary to melt a narrow zone in the semiconductor.10-18

Most investigators have found it necessary to use an encapsulant layer on top of the film to be recrystallized by zone melting. These encapsulants serve the obvious purposes of minimizing contamination and decomposition of the film during ZMR. However, they also induce a crystalline texture, improve the surface morphology of the film, and reduce or prevent agglomeration. For example, an SiO encapsulant was found necessary to obtain a (100) texture in ZMR of Si films on SiO.9 As shown in Fig. 1, the surface morphology of a Si film improves with the SiO encapsulant thickness.19 In the case of ZMR of InSb, the natural oxide, InO, was used as an encapsulant.6

Often, a molten semiconductor will not wet a substrate and will "bead up" or agglomerate during ZMR. Hasegawa2 found that agglomeration could be avoided by keeping the molten zone very narrow, a few 100 µm wide. However, such narrow molten zones usually require highly focused energy sources such as