Self-alignment techniques for fabricating a-Si:H TFTs at 300°C on clear plastic

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Abstract

We previously demonstrated highly stable back-channel cut and back-channel passivated amorphous silicon thin-film transistors (a-Si:H TFTs) made at 300°C on 2.9-inch x 2.9-inch clear plastic substrates [1]. Mechanical stress in the TFT stack causes the substrate to expand or contract, which easily results in misalignment between consecutive device layers [2,3]. Therefore we developed three self-alignment processes to resolve this issue. To process (1) we self-aligned the channel passivation in back-channel passivated TFTs to the gate. To process (2) we self-aligned the source-drain terminals, and the a-Si:H island layer in back-channel cut TFTs to the gate. To process (3) we combined processes (1) and (2), which enabled us to fabricate back-channel passivated TFTs with the channel passivation, the source-drain terminals and the a-Si:H layer self-aligned to the gate. Using these processes we were able to reduce the TFT channel length to 5µm with a 1 µm source/drain (S/D) overlap, and obtained functional devices over the entire surface area of the plastic workpiece.

1. Introduction

The mechanical stress in a plastic workpiece needs to be designed carefully [1-3] to obtain functional devices on free-standing plastic substrates. Even if the deposited device layers are crack-free, the stress in the TFT stack causes the substrate to expand or contract (depending on the sign of the strain of the total structure), resulting in misalignment between consecutive mask layers. Misalignment is defined by $\Delta \equiv 10^6 \times d/\lambda$ [ppm]. In this equation d is the local misalignment between the alignment mark in the bottom layer (patterned before device layer deposition) and the alignment mark in the top layer (patterned after device layer deposition). λ is the distance from the center of the substrate to the center of the alignment mark where the misalignment is calculated.

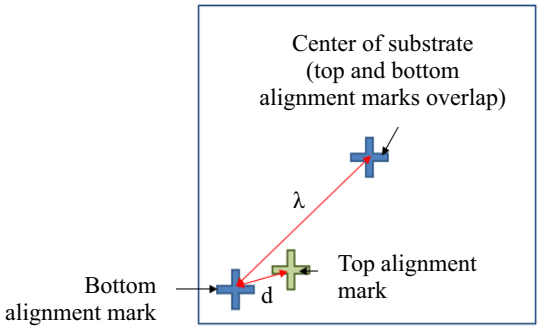

Figure 1 Schematic indicating where d and λ are measured to calculate the degree of misalignment between mask layers (not to scale)

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alignment processes for TFT fabrication on clear plastic. We refer to them as SA-1, SA-2 and SA-3 for easy reference. For SA-1 we use a back-channel passivated TFT process to self-align the gate (mask 1) and the channel passivation (mask 2). This approach is similar to that published by Cheng [4]. For SA-2 we use a back-channel cut TFT process to align the gate (mask 1) to the S/D terminals (mask 2) and the a-Si:H islands (mask 3); finally SA-3 is a combination of SA-1 and SA-2. The numbers indicated in the definitions of SA-1, SA-2 and SA-3 are the numbers of the masks that would be used to pattern these layers if we were using standard photolithography. The distinguishing feature common to all of these self-alignment methods is that they rely on a previously patterned device layer as a mask to pattern a subsequent device layer. This is in contrast to a standard photolithographic process where patterns are transferred from a rigid glass mask to the top device layer on the substrate. Device layers (such as metal layers) that block UV light act as 'masks' in self-alignment processes. In our process we always align all mask layers at the center of the substrate, and measure misalignment at the edge. Figure 1 shows a schematic of a substrate after patterning the second mask layer using photolithography, indicating where d and λ are measured. For TFTs this misalignment has the following implication: if the device layers delineating the TFT channel do not overlap the TFT will not turn on.

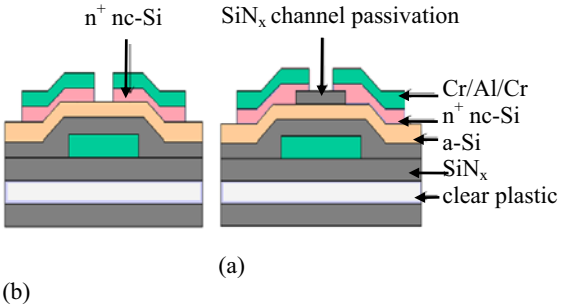

Figure 2 a-Si:H TFT structures: (a) back-channel cut, bottom-gate staggered source-drain, (b) back-channel passivated

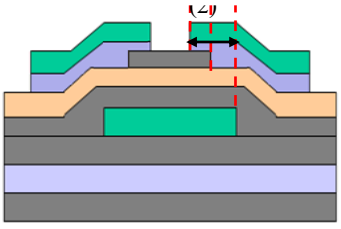

Figure 3 Schematic cross section indicating the critical overlaps (1) and (2) for bottom-gate back-channel passivated a-Si:H TFTs

A schematic showing the back-channel cut and back-channel passivated TFT structures that we fabricated in our work is shown in Figure 2. The position of the critical alignment gaps/overlaps between (1) the gate and the channel passivation and (2) between the gate and the S/D terminals for a back-channel passivated TFT are shown in Figure 3. Another issue to be considered is the impact of misalignment on the minimum TFT channel dimensions that can be designed in a mask set for device fabrication on plastic. To counteract misalignment it is customary to fabricate TFTs with large S/D overlaps with the gate (≥10μm), and that have relatively long channels (our usual TFT channel length is 40μm). A reduction in the misalignment between device layers will allow us to reduce the TFT channel dimensions.

2. Device Fabrication

2.1 Substrate Preparation

Our 75-μm-thick optically clear-plastic substrates are cut into 7.4 × 7.4 cm^2 workpieces. These substrates have a working temperature ≥ 300^0C. Their in-plane coefficient of thermal expansion $\alpha_{SUBSTRATE}$ is ≤ 10 ppm/◦C, which is sufficiently low to obtain intact device layers in a 300^0C process [1]. We prepare our clear plastic substrate as described in [1]. Following the plasma treatments the front and back of the substrate are coated with a SiN_x barrier layer. In each case, the barrier layer deposition was preceded by the deposition of 30nm of SiN_x at 213mW/cm^2 (ultra-high power) and 280^0C to promote adhesion. The 200nm thick front barrier layer was deposited at a power density of 18mW/cm^2 at 280^0C and the 300nm thick back barrier layer was deposited at a power density of 18mW/cm^2 at 280^0C.

2.2 TFT Device Structure

The SiN_x gate dielectric is 300nm thick. We chose an a-Si:H thickness of 25nm to make the layers sufficiently transparent for self-alignment [4]. The n^+ doped layer is 50nm thick and the SiN_x back-channel passivation layer is 150nm thick. The SiN_x, a-Si:H and n^+ a-Si:H layer deposition recipes are listed in Table 1. The gate electrodes, as well as the source/drain electrodes are patterned from tri-layers of Cr/Al/Cr, which are 15/40/15nm thick.

2.3 SA-1 Back-channel Passivated

The fabrication of back-channel passivated TFTs using SA-1 self-alignment is used to self-align the channel passivation in our back-channel passivated TFTs to the gate electrode [4]. It proceeds as follows: first we deposit a tri-layer of Cr/Al/Cr using thermal evaporation; then we pattern the metal to form the gate electrodes using standard photolithography. During all photolithography steps, the plastic substrate is temporarily mounted to a carrier glass to keep it flat. Next, we deposit the TFT stack (SiN_x, a-Si:H, and SiN_x) and carry out SA-1 self-alignment between the channel passivation layer and the gate. This is done as follows: we coat the top SiN_x channel passivation layer with hexamethyldisilazane (HMDS) and AZ5214 photoresist and prebake it for 30 seconds (soft-bake). Then we load the substrate facing downwards into a MJB3 mask aligner. Therefore the back of the substrate is facing the UV light source. In this situation the gate metal will act as a mask, blocking UV light from reaching the photoresist. We expose the photoresist through the back of the substrate for 15 minutes using a light intensity of 3.5mW/cm^2 at a wavelength of 405nm. Following back-exposure, we develop the photoresist for 50 seconds using AZ300 developer, removing all areas of the photoresist that were exposed to UV radiation. Next, the SiN_x layer is over-etched in buffered oxide etch (BOE = $HF:NH_4F:H_2O$) for 90 seconds to create a gap between the edge of the gate and the edge of channel passivation. Now we clean the surface using a piranha etch (H_2O_2:H_2SO_4) followed by a short dip in BOE diluted 1:100 with DI to ensure clean interfaces between the exposed a-Si:H channel layer and the subsequently deposited n^+ a-Si:H. Next, the n^+ a-Si:H and a tri-layer of Cr/Al/Cr film are deposited and patterned to form the S/D electrodes using mask 2, by wet-etching of the Cr/Al/Cr tri-layer and RIE etching of the n^+ layer. Next, we use mask 3 and RIE etching to pattern the a-Si:H islands. Finally, via holes are opened over the gates using RIE and mask 4.

Table 1 TFT stack deposition conditions

	SiN_x gate dielectric	i a-Si:H	SiN_x channel passivation	n^+ a-Si:H
Substrate temperature (°C)	300	250	240	250
Pressure (mTorr)	500	500	500	500
Power density (mW/cm^2)	22	17	22	22
Gas flow rate (sccm)	SiH_4 = 15 NH_3 = 130	SiH_4 = 50	SiH_4 = 15 NH_3 = 130	SiH_4 = 44 PH_3* = 6
Approximate growth rate (Å/s)	1.8– 4.5	1.6	1.5	1.1
Usual thickness deposited (nm)	300-400	25	150	30

*1% diluted in hydrogen

2.4 SA-2 Back-channel Cut

We developed SA-2 self-alignment to fabricate back-channel cut a-Si:H TFTs where the a-Si:H island layer and the S/D electrodes are self-aligned to the gate. In this process we first pattern the gate electrodes using mask 1 as described in section 2.3, followed by TFT stack deposition (SiN_x, a-Si:H, and n^+ a-Si:H). Then the sample is removed from the PE-CVD system and the S/D interconnects are self-aligned to the gates as follows: we coat the top of the sample with HMDS and AZ5214 photoresist and prebake it, as described in section 2.3. Now we first use standard photolithography and mask 2 to create large patches of photoresist over the channel regions. Next, we use SA-2 self-alignment to pattern these patches into thin stripes of photoresist centered over the channel region. The edge of the photoresist stripe is moved to the inside of the edge of the gate by loading the substrate into the mask aligner front-side facing downwards, and at an angle as illustrated in Figure 4. The substrate then is exposed for 12 minutes at a power density of 3.5mW/cm^2 and a wavelength of 405nm. Then the substrate is rotated by 90^o (still facing downwards) and is again exposed for 12 minutes. The exposure and rotation steps are repeated a total of 4 times, giving a total exposure time of 48 min. Finally the substrate is developed in AZ300 for 40 to 60 seconds. Figure 5 shows an optical micrograph of such a photoresist stripe patterned on top of a TFT gate. For the conditions stated above we routinely achieved a gap ~1μm between the edge of the gate pattern and

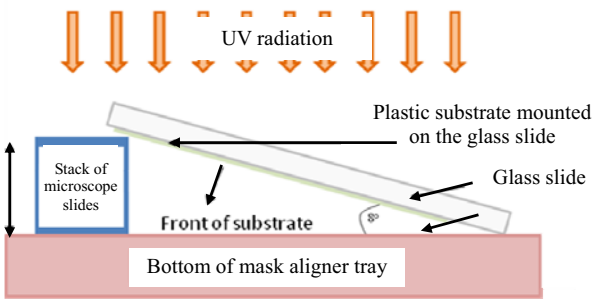

Figure 4 Schematic indicating the loading sequence in SA-2 and SA-3

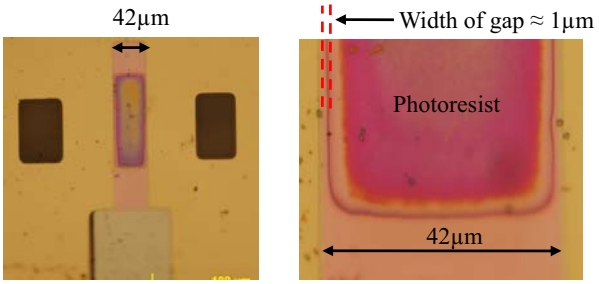

Figure 5 A TFT after the source-drain self-alignment step (a) whole TFT (b) close-up of channel region, showing the 1µm gap between the edge of the gate and the photoresist created using SA-2. The W/L of this TFT is designed to be 80µm/40µm

the photoresist. After the self-alignment step, the substrate surface is dipped in buffered oxide etch mixed 1:100 with DI water for 2-4 seconds and loaded directly into the thermal evaporator. A tri-layer of Cr/Al/Cr is thermally evaporated for S/D electrodes. Next we carry out a lift-off process by placing the sample in a sonicator bath with isopropanol for about 20 minutes. This is followed by soaking the substrate in AZ400 for about 10 seconds while rubbing the surface gently with two q-tips, in succession followed by an oxygen descum (the conditions in our Plasmatherm 790 are set at O_2 flow rate = 40sccm, pressure = 115mTorr, RF power = 80W and time = 600s). This lift-off step removes the source-drain metal from the channel region, opening up the gap in the metal between the S/D electrodes. We now use standard photolithography and mask 3 to define the rest of the S/D electrodes. The pattern in mask 3 shows the shape of the S/D electrodes, except that the gap between the S/D electrodes is omitted since the metal in this region was already removed by the lift-off process. At this point we have self-aligned the S/D terminals to the gate. After wet-etching the S/D metal layer in the pattern defined by mask 3 we plasma-etch the n^+ layer and the a-Si:H layer. In doing so, we remove all of the a-Si:H on the surface, except for the a-Si:H in the channel region that was protected by the photoresist pattern of mask 3. This means that we have effectively self-aligned the a-Si:H layer to the S/D layer in this step. Next, we strip the photoresist, plasma-etch the n^+ nc a-Si left in the channel region and etch via holes in the SiN_x gate dielectric over the gate contact pad (mask 4). This completes the back-channel passivated TFTs. In this process we self-aligned the S/D electrodes, the a-Si:H island and the gate electrode.

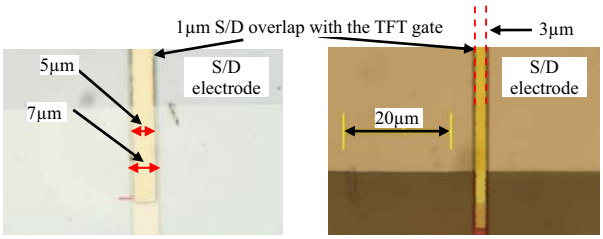

Figure 6 Optical micrograph of the channel region of back-channel passivated TFTs fabricated using SA-3, on clear plastic, with channel lengths of (a) L = 5µm and (b) L = 3µm. The maximum process temperature was 300°C

2.5 SA-1 and SA-2 combined to SA-3

For SA-3self-alignment we combined SA-1 and SA-2 self-alignment methods described in Sections 2.3 and 2.4 to fabricate back-channel passivated a-Si:H TFTs in which the channel passivation, the S/D terminals and the a-Si:H layer are self-aligned to the gate. A completed TFT fabricated using SA-3 is shown in Figure 6. Using this self-alignment approach we were able to achieve a minimum channel length of 3µm.

3. Results and Discussion

3.1 Self-alignment

SA-1 self-alignment does not allow us to achieve functional devices over the entire 7.4 × 7.4 cm^2 substrate surface since we are not able to align the S/D terminals to the gate. In contrast, SA-2 and SA-3 self-alignments allow us to align all critical device layers over the entire surface area, as well as drastically reduce the TFT channel length. This is illustrated in Figure 7 which shows a section of the finished work-piece, at a distance of ~5 cm away from the center of the substrate. The TFT on the right hand side of the figure is patterned using SA-3 self-alignment and is fully functional. The TFT has a W/L = 360µm/3µm, and a 1µm S/D overlap with the gate. In contrast, the alignment mark on the left hand side of Figure 7 is patterned without self-alignment. The gate layer (patterned with mask 1) and the S/D layer (patterned with mask 2) of the alignment mark are displaced by ≈ 15µm. This gives a misaligment error of $\Delta \equiv 10^6$ x 15/50,000 = 300ppm when the bottom (gate) and the S/D layers are patterned using standard photo-lithography.

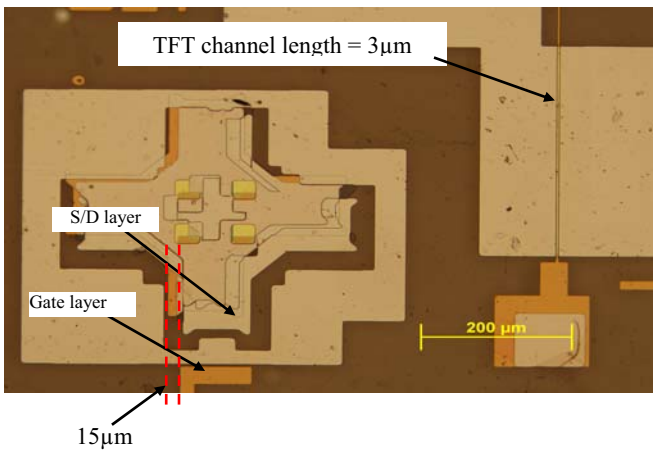

Figure 7 Optical micrograph of a back-channel passivated TFT fabricated using SA-3 at 300°C on clear plastic. The TFT W/L is 360 µm / 3 µm.

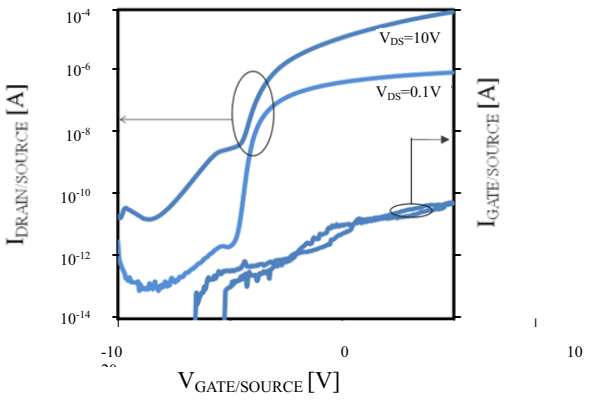

Figure 8 Transfer characteristics of an a-Si:H TFT fabricated at 300°C using a back-channel passivated geometry and SA-3 self-alignment

3.2 Electrical Performance

We evaluated the electrical performance of our TFTs by measuring the transfer characteristic using an HP4155A parameter analyzer. We measure I_{DS} and I_{GS} while sweeping V_{GS} from -10 to 20V, at V_{DS} = 0.1V or 10V. The measured transfer characteristic of a TFT with W/L = 360 µm / 5 µm is plotted in Figure 8 and the performance parameters extracted from this figure are listed in Table 2. The TFT clearly works and has acceptable effective mobility values (for a short-channel length TFT). The undesirably high OFF-current for the V_{DS}=10V plot is attributed to remnants of photoresist in the channel region after the lift-off process.

4. Conclusion

We have demonstrated self-alignment of the channel passivation, the S/D electrodes and the a-Si:H layer to the gate electrode of a-Si:H TFTs fabricated on clear plastic, and reliably achieved a 1-µm S/D overlap with the gate. We were able to fabricate functional TFTs with a channel length as small as 3µm over the entire 7.4 × 7.4 cm^2 substrate surface. In contrast, a process without self-alignment results in a misalignment as large as 300ppm between the bottom (gate) and the S/D layer at the edge of the substrate. Therefore it would have been impossible for us to fabricate functional TFT arrays with such small channel lengths over the entire surface area using standard photolithography. Our self-alignment process therefore improves on our standard 300°C fabrication process in three ways. (1) It allows us to implement our 300°C process over a large surface area. (2) It enables us to fabricate TFTs with very small channel lengths. (3) It allows us to reduce the S/D overlap with the gate from 10µm down to 1 µm.