

# High Breakdown Voltage Schottky Gating of Doped Si/SiGe 2DEG Systems Enabled by Suppression of Phosphorus Surface Segregation

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## I. INTRODUCTION

Quantum dot devices in the Si/SiGe material system are a promising candidate to implement quantum computation due to the weak nature of its nuclear spin. A Schottky split-gate on a Si/SiGe modulation-doped two-dimensional electron gas (2DEG) with negative biases has become a common way to define lateral quantum dot arrays [1]. However, the severe leakage through the Schottky gate caused by the phosphorus surface segregation from the intentionally doped electron supply layer degrades the reliability of split gate technique. In this study, we demonstrate a large reduction in gate leakage by the suppression of phosphorus surface segregation during sample growth.

## II. SAMPLE PREPARATION

2DEGs were first epitaxially grown by rapid thermal chemical vapor deposition (RTCVD) (Fig.1). Samples were then etched as Hall bars and AuSb was deposited as contacts followed by 450°C annealing for 10 minutes. Pd was finally deposited across the Hall bar to form a Schottky gate. The mobility of 2DEG samples used in this study is above 200,000 cm<sup>2</sup>/Vs and 2D electron densities are in the range of 5~9x10<sup>11</sup> cm<sup>-2</sup>.

## III. DISCUSSIONS

A negative bias on the gate should fully deplete the 2DEG to pattern it. However, the well-known surface segregation of phosphorus from the doped electron supply layer into the following SiGe/Si capping layers during growth causes a high electric field at the sample surface when a reverse bias is applied. This high field leads to tunneling of electrons from the metal to the semiconductor, resulting in undesirable gate leakage. For example, growing capping layers at 575°C results in extensive phosphorous surface segregation, giving a phosphorous surface concentration about 1x10<sup>18</sup> cm<sup>-3</sup> (Fig.2a). There is a small breakdown voltage ~-2V and the channel between drain and source can't be shut off before leakage starts (Fig.3).

The phosphorous segregation can be greatly suppressed by lowering cap layer growth temperature from 575°C to 525°C [2]. Therefore, the phosphorous surface concentration can be reduced as low as 2x10<sup>16</sup> cm<sup>-3</sup> (Fig.2b), and the breakdown voltage is dramatically increased to over -7V (Fig.3). Simulations based on [3] with an effective E<sub>max</sub>

calculated from phosphorus profiles (Fig.2) fit data fairly well. In addition, the 2DEG channel can be shut off when the gate voltage is around -0.53V with negligible leakage current (Fig.4).

With low leakage, a quantum point contact (QPC) structure was fabricated. By measuring the conductance through five different sets of gates with various spacing (inset of fig.5), the best gap width to sense remote charges for external use as a charge detector from a nearby quantum dots can be observed (Fig.5) [4]. For the gap width~280nm (between G0 and G1), the current flowing in the gap could not be closed for any voltages. The high sensitivity occurs with the narrowest gap width ~ 80nm (between G0 and G5) where the current in the gap could be turned completely on and off within small gate voltages (Fig.6).

## IV. CONCLUSION

In this study, the suppression of phosphorus segregation by low temperature (525°C) cap layer growth results in high breakdown voltage of Schottky gates on modulation-doped Si/SiGe heterostructures. The wide window to deplete 2DEGs via negative bias with very low leakage thus enables Schottky split-gate quantum devices.

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## References

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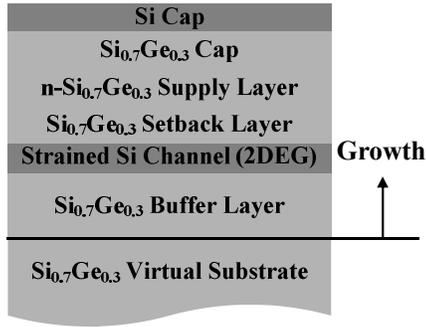


Fig.1: Typical modulation-doped Si/SiGe 2DEG layer structure grown by RTCVD.

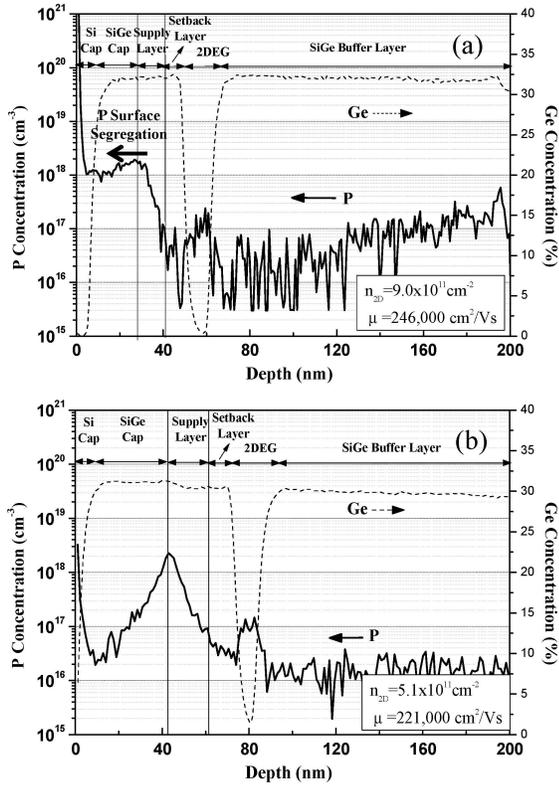


Fig.2: SIMS profiles for the samples with cap layers grown at (a) 575°C and (b) 525°C. The phosphorous “bump” in the Si 2DEG is a SIMS artifact.

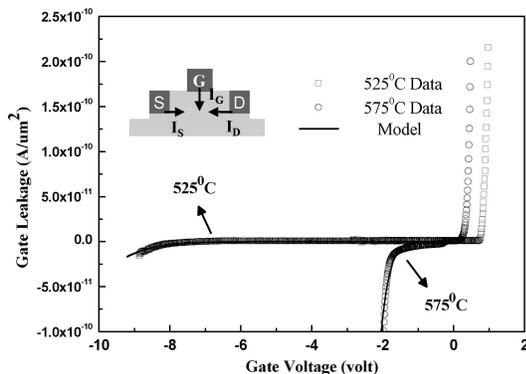


Fig.3: Schottky leakage test at 4K and simulation.

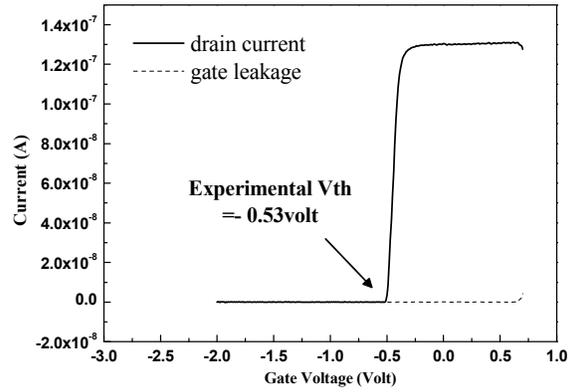


Fig.4: Depletion test of the sample with caps grown at 525°C (temp = 4K).

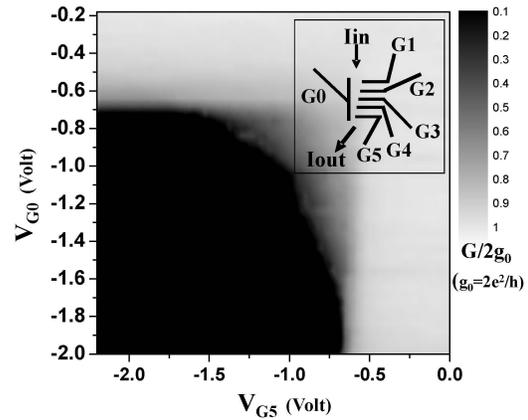


Fig.5: Successful QPC test without any leakage (temp = 4K). A wide transient region is observed. The inset shows the schematic of the QPC test structure.

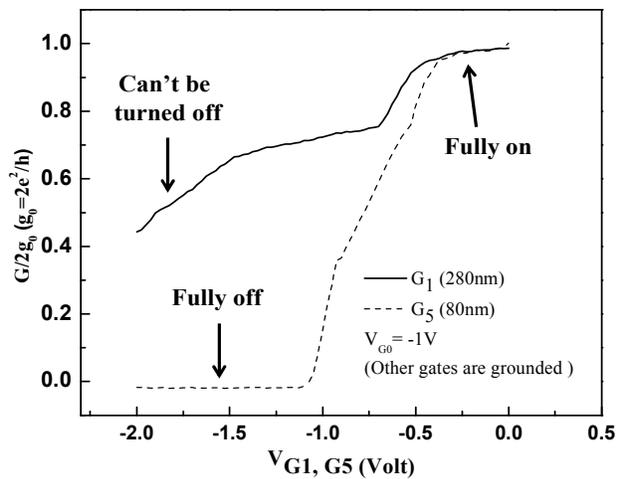


Fig.6: The channel between  $G_0$  and  $G_1$  remains on at -2V but the channel between  $G_0$  and  $G_5$  can be fully shut off.