

## Thin-Film Circuits for Scalable Interfacing Between Large-Area Electronics and CMOS ICs

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Hybrid systems based on large-area electronics (LAE) and CMOS ICs aim to exploit the complementary strengths of the two technologies: the scalability of LAE for forming interconnects and transducers (for sensing and energy harvesting), and the energy efficiency of CMOS for instrumentation and computation. The viability of large-scale systems depends on maximizing the robustness and minimizing the number of interfaces between the LAE and CMOS domains. To maximize robustness, inductive and capacitive coupling has been explored, avoiding the need for metallurgical bonding [1]. To minimize the number of interfaces, a method to access and readout individual sensors via minimal coupling channels, is crucial. In this abstract, we present a thin-film transistor (TFT) based scanning circuit that requires only three capacitively-coupled control signals from the IC to sequentially access an arbitrarily large number of LAE sensors, enabling a single readout interface (Fig. 1). A key attribute of the presented circuit is the low power consumption, which remains nearly constant even as the number of sensors scales.

Previously, an LAE-CMOS interface using a fully-passive TFT and thin-film diode scanning circuit was demonstrated, requiring four control signals transmitted inductively from the CMOS IC [1]. With the IC providing power for the circuit, inductors were required to step up the voltage of the IC signals (from 1.2V to 6.5V) to ensure adequate TFT drive current. Due to inductor losses, this imposed substantial power consumption, limited voltage swings, and correspondingly degraded operating frequency. In this work, an on-sheet LAE power supply based on solar energy harvesting [2], is incorporated to demonstrate a novel active NMOS TFT-based scanning circuit (Fig. 1). The new design is not only amenable to standard TFT processing techniques, but also enables larger voltage swings, higher operating frequencies, lower power consumption, and a reduced number of IC control signals.

Fig. 2 shows the TFT-based scanning circuits that generate individual sensor-accessing signals ( $EN_{<i>N</i>}$ ) using only 3 control signals: a two-phase clock (CLK and CLK\_BAR) and global reset (GRST). The  $N^{\text{th}}$  scan block receives the charge signal, CIN, from the  $N-1$  element, except for the first block wherein GRST is used instead. The CIN signal turns on TFTs on both sides of the capacitor, causing both plates to discharge. Next, when CIN is de-asserted the bottom plate is driven back to the supply level. Since the capacitor maintains its voltage, the top plate,  $EN$ , also rises to the supply level. Thus,  $EN_{<N>}$  is asserted, and the information of the corresponding sensor is accessed through the output channel. Simultaneously, when  $EN$  is high, the clock signal, CLK, is passed as the charge signal for the  $N+1$  element (COUT). With the 2-phase clock, the scanning system generates  $EN$  signals at twice the frequency of the clock signal. Finally,  $EN_{<N>}$  is permanently de-asserted when a reset signal (RST) from the  $N+1$  block discharges the bottom plate of the capacitor. Importantly, this design ensures that voltage of  $EN$ , though dynamically held, will robustly remain low due to the circuit's leakage currents. Consequently, a large number of scan blocks can be safely employed.

Many sensors, such as the LC oscillator-based cells in [3], require an enable signal with a high voltage swing ( $\sim 15-20V$ ). To produce such a voltage swing, the TFTs in the scanning blocks require a large transconductance, and thus large gate voltages (CIN, RST, GRST  $\sim 12-15V$ ). However, since ICs typically have lower I/O voltages ( $\sim 3.6V$ ), level converter circuits are used to convert the CMOS input signals (CLK\_IC, CLK\_IC\_BAR, GRST\_BAR) to the required levels (CLK, CLK\_IC\_GRST\_BAR). The level-converter circuits (Fig. 2) work in a similar fashion to the scanning circuits (by discharging the capacitor).

Although the level converters consume static power, only the scan block whose enable signal is asserted will consume static power. Thus, with this design, the number of scan blocks and sensors can be scaled with no additional static power consumption.

The level converter and scanning circuits were fabricated in a flex-compatible a-Si TFT technology (Fig. 3). The TFTs have a channel length of 10  $\mu\text{m}$  and electron mobility of  $\sim 0.7 \text{ cm}^2/(\text{V}\cdot\text{s})$  (Fig. 4). The samples tested in this work were fabricated on glass substrates (Fig. 5). Fig. 6 shows the output of the level converter circuit, CLKH, having a voltage swing of  $\sim 15V$ , when driven by a 500 Hz, 3.6 V swing input clock signal CLKL, at  $V_{\text{DD}} = 20V$ . Fig. 7 shows the GRST, CLK,  $EN_{<1>}$ , and RST signals for the first scan block at a frequency of 1 kHz (clock frequency of 500 Hz) and  $V_{\text{DD}} = 20V$ . Finally, Fig. 8 shows four enable signals ( $EN_{<1-4>}$ ) with a voltage swing of  $\sim 15V$  at a frequency of 1 kHz (clock frequency of 500 Hz) and  $V_{\text{DD}} = 20V$ . The circuits have been tested up to a 2kHz clock frequency, and integration in a preliminary hybrid system for multi-sensor accessing has been achieved [3].

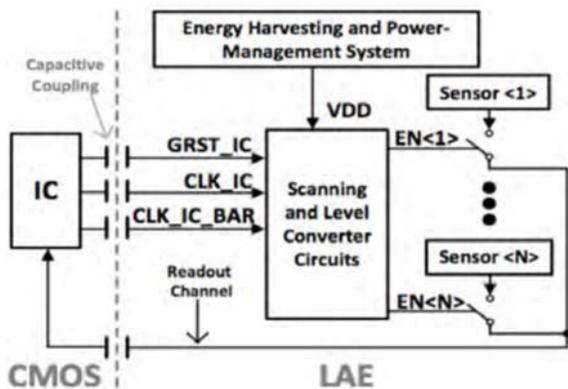
In conclusion, a new TFT-based circuit with large voltage swings, high operation frequencies, and low power consumption, for accessing a large array of sensors using only three IC control signals has been demonstrated.

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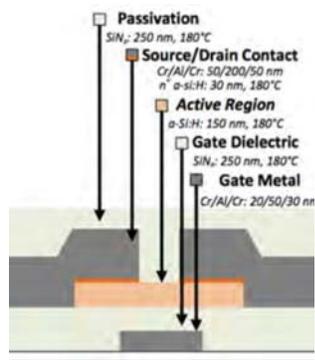
[1] Yingzhe Hu et al., 2012 Symposium on VLSI Circuits.

[2] Warren Rieutort-Louis et al., IEEE Journal of Photovoltaics, Vol. 4, No. 1, January 2014, pp 432-439

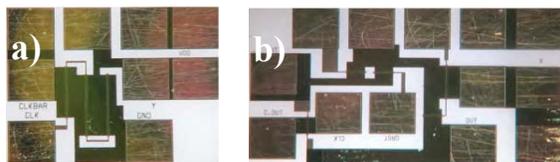
[3] Yingzhe Hu et al., 2014 Symposium on VLSI Circuits (submitted)



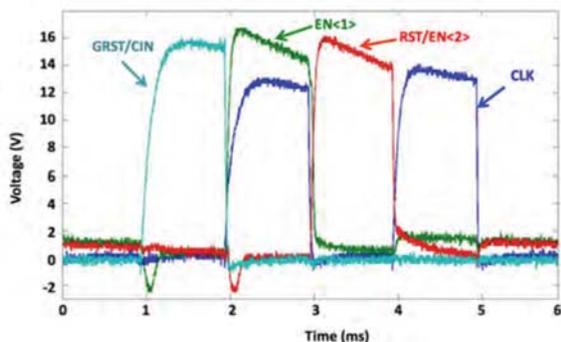
**Fig. 1:** Overall CMOS-LAE hybrid system architecture. Enable signals, EN, are used to sequentially access an arbitrarily large number of sensors through one output channel.



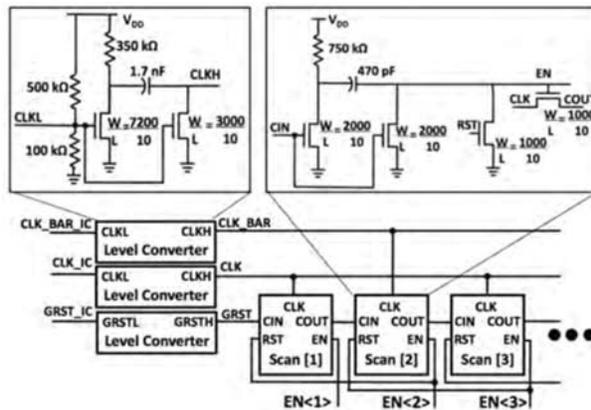
**Fig. 3:** Cross-sectional diagram of a-Si TFTs.



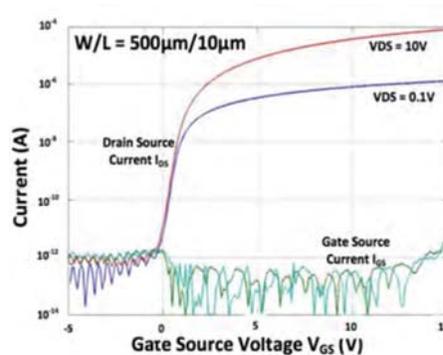
**Fig. 5:** a) Level converter test sample on glass. b) Scan circuit test sample on glass.



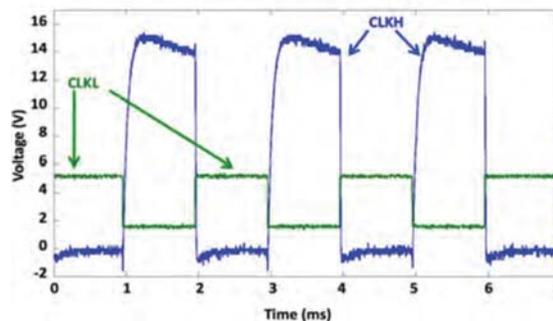
**Fig. 7:** CIN (GRST), EN<1>, RST (EN<2>), and CLK signals for the first scan block at an operation frequency of 1 kHz (clock frequency of 500 Hz).



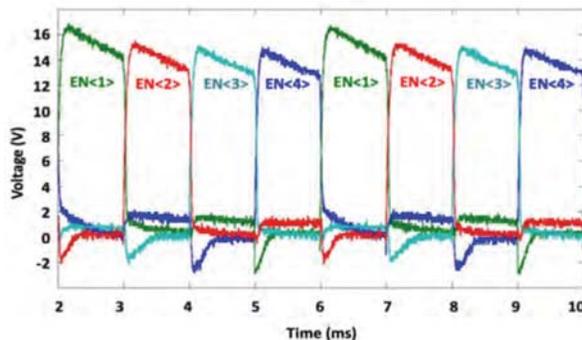
**Fig. 2:** NMOS TFT-based scanning and level converter circuits to generate enable signals, EN. TFT widths and lengths are in  $\mu\text{m}$ .



**Fig. 4:** I-V characteristic of an a-Si TFT on glass.



**Fig. 6:** The output, CLKH (CLK\_BAR), of a level converter circuit with input CLKL (CLK\_BAR\_IC) at a frequency of 500 Hz.



**Fig. 8:** The enable signals, EN<1-4>, from an array of four scan blocks, to continuously sample a four-sensor array at an operation frequency of 1 kHz (clock frequency of 500 Hz).