

Amit Kumar

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INTERESTS

Interconnection networks, on-chip networks, multicore architectures, system-level power/thermal modeling and management.

EDUCATION

Princeton University, Princeton, NJ

Ph.D. in Electrical Engineering Aug. 2008 (expected)
Advisors: Prof. Li-Shiuan Peh
Prof. Niraj Jha

Princeton University, Princeton, NJ

M.A. in Electrical Engineering May 2005
GPA: 3.8/4

Indian Institute of Technology, Kharagpur, India

B.Tech. (Honors) in Electrical Engineering June 2003
GPA: 9/10

WORK EXPERIENCE

Graduate Research Intern – Intel Corp., Santa Clara June-Sept. 2006

- Proposed and evaluated a novel performance- and energy-efficient network flow-control and router micro-architecture design for on-chip interconnection networks.

Graduate Research Intern – Intel Corp., Santa Clara June-Sept. 2005

- Worked on micro-architecture level modeling and infrastructure development for power and performance studies of on-chip interconnection networks.

Summer Intern – National Semiconductor, Bangalore, India May-July 2002

- Worked on verification and testing of the memory and bus interface units of an ARM processor using Verilog HDL and verification tools.

Summer Intern – Advanced VLSI Lab, I.I.T., Kharagpur, India May 2001

- Gained hands-on experience designing several analog and digital VLSI circuits using CAD tools.

Teaching Assistant – Princeton University Feb.-May 2005

- Conducted precepts and designed/graded exams and assignments for a sophomore-level course “Introduction to Logic Design”.

RESEARCH

- Designing close to ideal on-chip networks** – The ideal interconnection mechanism to connect different communicating nodes on a chip is to have dedicated links between all possible pairs

of communicating nodes. Unfortunately, this approach does not scale beyond a few nodes. Hence, driven by technology limitations to scaling and increasing bandwidth demands, state-of-the-art on-chip networks in both general-purpose chip multi-processors (CMPs) and application-specific systems-on-a-chip (SoCs), use a packet-switched design in which network links are multiplexed over several communication flows. This, however, comes with a significant latency, area and energy cost in the form of a complex router needed at every node for orchestrating communication. I have proposed and developed Express Virtual Channels (EVCs), a novel flow-control mechanism which supports virtual express lanes in the network using which packets can bypass routers along their path, thereby approaching the ideal communication of dedicated links with almost no router overhead. EVCs have been shown to exhibit excellent scalability with a very low implementation complexity.

- **High-performance router design for on-chip networks** – On-chip networks in multicore designs are required to provide ultra-low latency and scalable, high-bandwidth communication to support a wide range of applications with diverse traffic characteristics, while adhering to tight area and power budgets with tractable hardware complexity. In this project, I worked on designing a high-speed on-chip router targeted at a 36-core shared memory CMP system in 65nm technology. This design targeted an aggressive clock frequency of 3.6GHz and a peak data rate in excess of 4.6Tbits/s per node, thus posing tough design challenges that led to several unique circuit and microarchitectural innovations and design choices, including a novel high throughput and low latency switch allocation mechanism, a single-cycle router pipeline, a low overhead virtual channel allocator and a dynamically-managed shared buffer design which uses prefetching to minimize critical path delay. Detailed performance, power and area evaluations were carried out both at the microarchitecture- and circuit-level.
- **Thermal modeling and management of multi-core chips** – This problem deals with developing thermal models for multicore chips and exploring distributed, collaborative ways to manage thermal emergencies across the chip. I have worked on implementing and evaluating run-time thermal management techniques for the on-chip network of the MIT Raw CMP.
- **System-level hybrid thermal management** – This project deals with system-level thermal issues, as opposed to chip-level and uses the global knowledge of the operating system in order to manage overall power and temperature. I have developed a framework to manage the run-time temperature of different system components, like the processor and memory, using a hybrid of hardware and software techniques in a coordinated fashion, with a very low performance impact. This involved modifying the Linux operating system to add performance-monitoring features and to make the scheduling policy thermal-aware.

PUBLICATIONS

- A. Kumar, L.-S. Peh and N. K. Jha, “Token flow control”, *41st International Symposium on Microarchitecture*, Lake Como, Italy, Nov. 2008 (to appear).
- T. Krishna, A. Kumar, P. Chiang, M. Erez and L.-S. Peh, “NoC with near-ideal express virtual channels using global-line communication,” *IEEE International Symposium on High-Performance Interconnects (HotI)*, Stanford, Aug. 2008 (to appear).

- A. Kumar, L.-S. Peh, P. Kundu and N. K. Jha, “Towards ideal on-chip communication using express virtual channels,” **IEEE Micro Top Picks from 2007 Computer Architecture Conferences, Jan./Feb. 2008 (paper selected among the top 10 papers from premiere computer architecture conferences).**
- A. Kumar, L. Shang, L.-S. Peh and N. K. Jha, “System-level dynamic thermal management for high performance microprocessors,” *IEEE Transactions on Computer-Aided Design (TCAD)*, Jan. 2008.
- A. Kumar, P. Kundu, A. P. Singh, L.-S. Peh and N. K. Jha, “A 4.6Tbits/s 3.6 GHz single-cycle NoC router with a novel switch allocator in 65nm CMOS,” *25th International Conference on Computer Design (ICCD)*, Lake Tahoe, Oct. 2007.
- A. Kumar, L.-S. Peh, P. Kundu and N. K. Jha, “Express virtual channels: Towards the ideal interconnection fabric,” *34th International Symposium on Computer Architecture (ISCA)*, San Diego, June 2007.
- A. Kumar, L. Shang, L.-S. Peh, and N. K. Jha, “HybDTM: A coordinated hardware-software approach for dynamic thermal management,” *43rd IEEE Design Automation Conference (DAC)*, San Francisco, July 2006.
- L. Shang, L.-S. Peh, A. Kumar, and N. K. Jha, “Temperature-aware on-chip networks,” **IEEE Micro Top Picks from 2005 Computer Architecture Conferences, Jan./ Feb. 2006 (paper selected among the top 13 papers from premiere computer architecture conferences).**
- L. Shang, L.-S. Peh, A. Kumar, and N. K. Jha, “Thermal modeling, characterization and management of on-chip networks,” *37th IEEE/ACM International Symposium on Microarchitecture (MICRO)*, Portland, Dec. 2004.

PATENTS

- A. Kumar and P. Kundu, “Express virtual channels: A method to improve energy and latency characteristics of a packet switched on-chip interconnection network,” U.S. patent filed, Assignee Intel Corp.
- A. Kumar and P. Kundu, “A novel low-latency, high-throughput switch allocator for on-chip 2D interconnection networks,” U.S. patent filed, Assignee Intel Corp.

HONORS

- Recipient of the **Intel Foundation Ph.D. Fellowship 2006-08.**
- **IEEE Micro Top Picks from Premiere Computer Architecture Conferences paper, 2007.**
- **IEEE Micro Top Picks from Premiere Computer Architecture Conferences paper, 2005.**
- Recipient of **Princeton Graduate Fellowship**, 2003.
- Ranked **among top 3 students** in the Department of Electrical Engineering, Indian Institute of Technology, Kharagpur, class of 2003.
- Ranked among **top 1% in Indian National Physics Olympiad**, 1999.
- Ranked among **top 0.5% out of around 150,000** candidates in the All India IIT joint entrance exam, 1999.

SKILLS

- **Programming languages:** C, C++, x86 assembly, Verilog HDL.
- **Operating systems:** Unix/Linux, Windows 95/98/NT, Solaris.
- **Architectural simulators/tools worked with:** MIT Raw, Rice Simulator for ILP Multiprocessors (RSIM), Wisconsin GEMS, SimpleScalar, Cacti, Wattch, HotSpot, Orion.

SELECTED TALKS

- “Performance- and power-efficient on-chip communication” at *Advanced Architecture and Technology Lab., AMD, Bellevue, WA*, March 2008.
- “A 4.6Tbits/s 3.6GHz single-cycle NoC router with a novel switch allocator in 65nm CMOS” at *International Conference on Computer Design (ICCD)*, Oct. 2007.
- “Express virtual channels” at *International Symposium on Computer Architecture (ISCA)*, June 2007.
- “Performance- and energy-efficient on-chip network microarchitecture” at *Platform Architecture Research (under Microprocessor Technology Lab.), Intel Corp., Santa Clara*, Sept. 2006.
- “HybDTM: A coordinated hardware-software approach for dynamic thermal management” at *Design Automation Conference (DAC)*, July 2006.
- “Power/performance studies in on-chip interconnection networks” at *Platform Architecture Research (under Microprocessor Technology Lab.), Intel Corp., Santa Clara*, Sept. 2005.

RELEVANT COURSEWORK

Interconnection Networks, Advanced Computer Architecture, Low Power IC and System Design, Scalable Systems and Applications, Advanced Operating Systems, Compiling Techniques, Processor Architectures for New Paradigms, Operating Systems, Computer Organization, Computer Networks, Switching and Sequential Systems, Digital System Testing, Pulse and Digital Circuits, Linear Electronic Circuits, Introduction to Computing, Basic Electronics, Multiprocessors and Microcomputers, Electronic Systems Design.

PROFESSIONAL ACTIVITIES

- External reviewer for the International Symposium on Computer Architecture.
- Reviewer for Computer Architecture Letters, IEEE Transactions on VLSI Systems, IEEE Transactions on Circuits and Systems and IEEE Potentials.
- Web Chair, International Symposium on Networks-on-chip, 2007.
- Student member IEEE, ACM, SIGARCH.
- Served on several committees of the School of Engineering and Applied Sciences and the Department of Electrical Engineering at Princeton University.

References:

Available upon request.