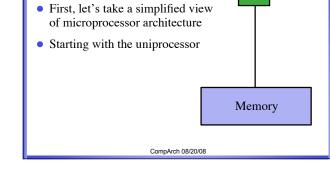
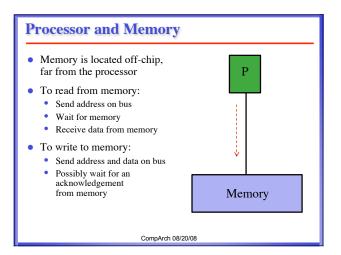
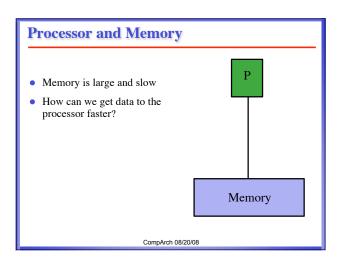


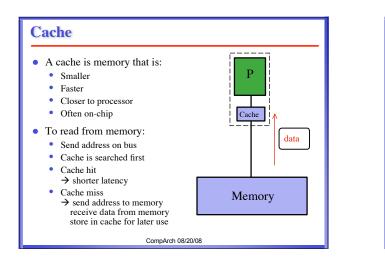
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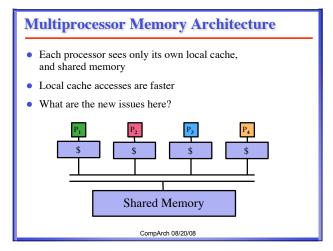
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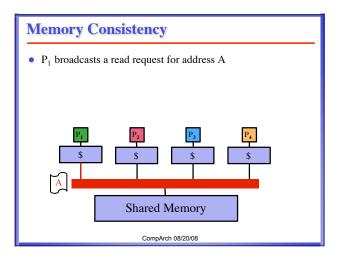


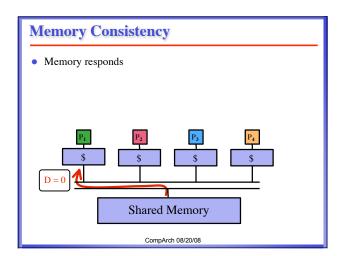


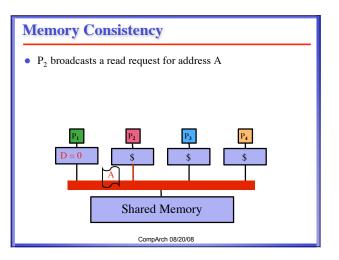


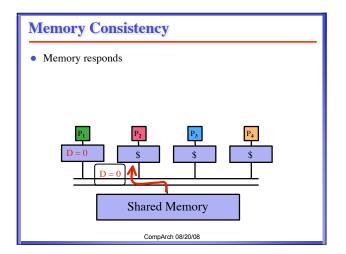
Multiprocessor Memory Architecture Processors connected to shared memory via a shared bus All processors see all memory activity Memory is large and slow How can we get data to the processor faster? Pa Pa Pa Pa Pa Memory Shared Memory Comparch 08/20/08

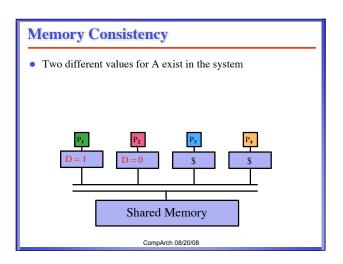


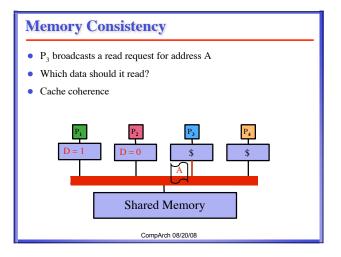


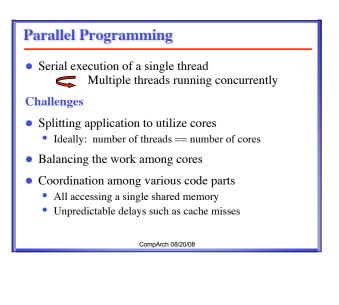


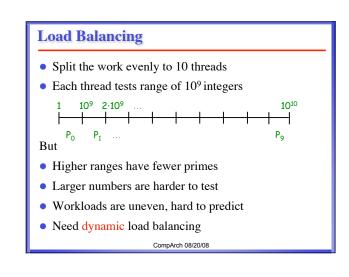








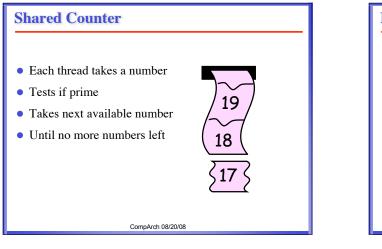


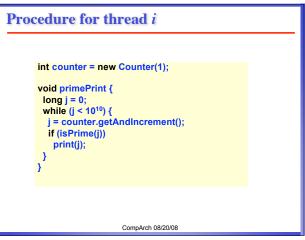


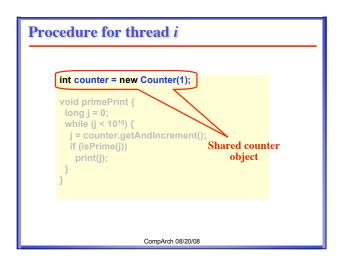
Prime Number Example

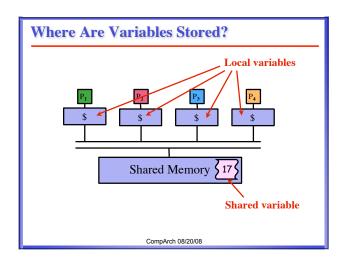
- <u>Task</u>: Print primes from 1 to 10¹⁰
 <u>Hardware</u>:
- Ten-processor CMP One thread per processor
- <u>Goal</u>: Close to maximum possible speedup Ten fold speedup over uniprocessor (?)

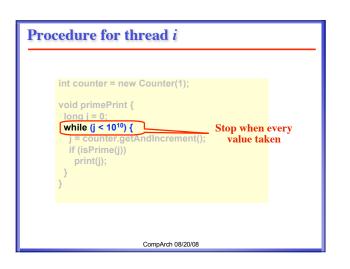
Example adopted from "Art of Multiprocessor Programmin CompArch 08/20/08 Herlihy-Shavit





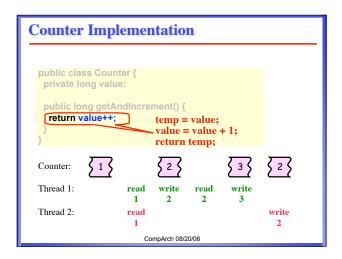


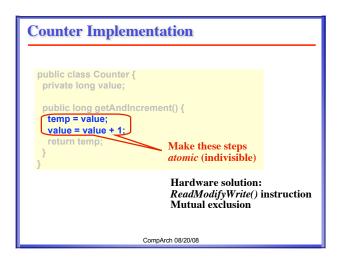


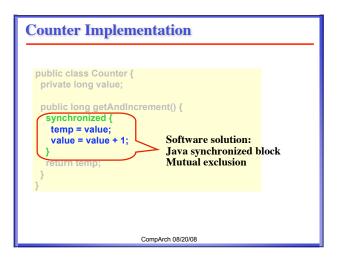


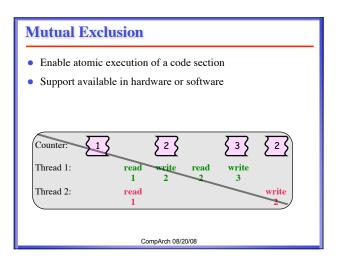


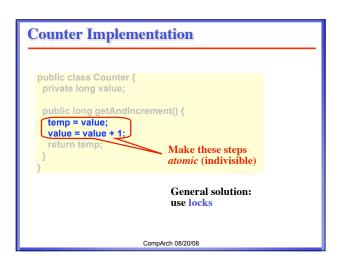


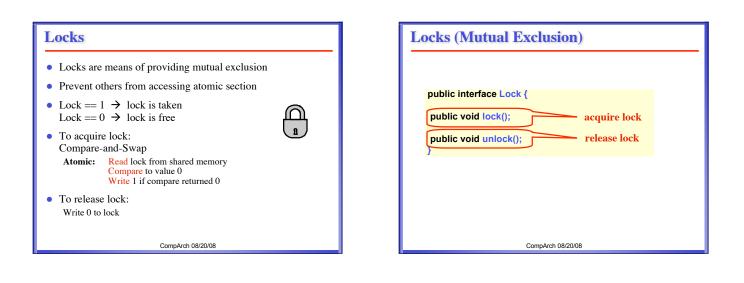




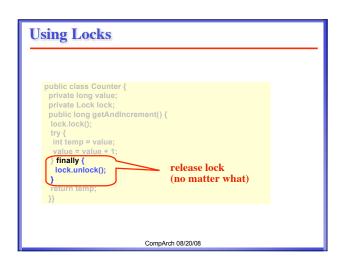


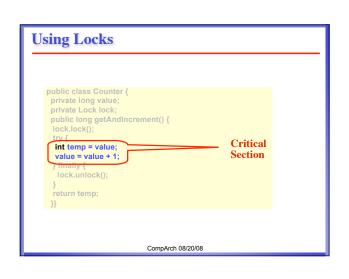












Parallel Programming for Performance

- Load balancing
- Reduce idle time when threads wait
- Maximize parallel portion of code
- Minimize sequential parts
- Small critical sections
 - Fine-grained synchronization

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Disadvantages of Locks

• Coarse-grain

- High contention (on the lock)
- Low throughput
- Fine-grain
- Difficult to program and debug
 - Deadlock, interrupt
- Spin-locks repetitive accesses until free
 - Many memory accesses
 - Useless work
- Alternatives: blocking, queue locks

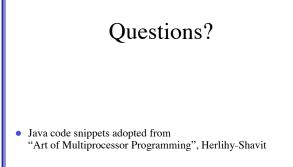
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Fransactional Memory
Lock-free synchronization
Transaction: Atomic section $lock() \rightarrow unlock()$
 Speculative execution – optimistic No conflicts → commit Conflicts detected → roll back, reissue
 Hardware requirements Additional memory or dedicated cache Changes to cache coherence protocol
• May also be implemented in software
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Parallel Programming

- Parallelize as much of the code as possible
- Minimize sequential parts
- Be careful with mutual exclusion
 - Requires waiting
 - Different approaches
 - Each has its advantages

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