



Power in Microprocessor Designs



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First....

Who Am I ?



Until a few years ago ..

Emphasis had been solely on improving performance



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Times have changed

No longer sole emphasis on performance

Power & reliability concerns have become huge !!

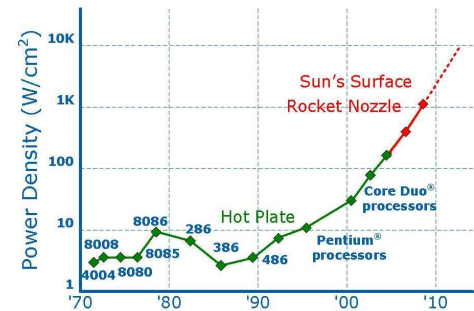
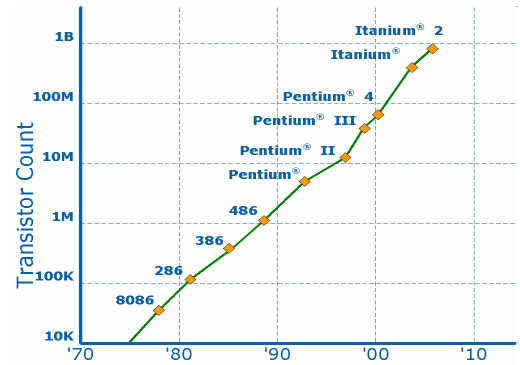
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Technology Trends: Moore's Law

- More and faster transistors with higher power demands
 - Gate delay ↓30% every process generation (2 years)
- Area of a transistor roughly scales by 50% per generation
 - Transistor density doubling
 - Power density increasing



Technology Trends

Traditional cooling solutions reaching physical limits

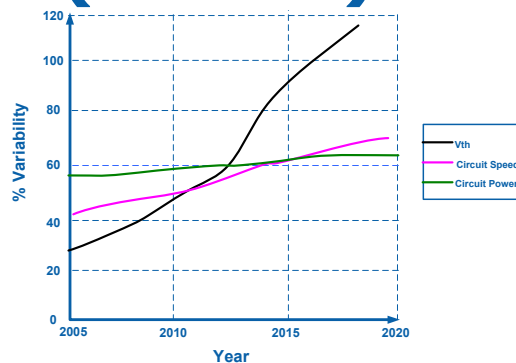


http://www.phys.ncku.edu.tw/~htsu/humor/fry_egg.html

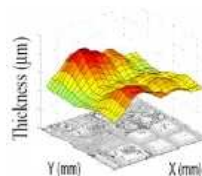


Technology Trends (contd.)

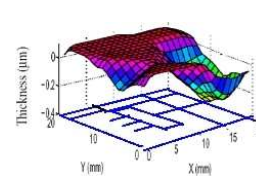
- In-die process variations
 - V_{th} variation
 - Variation in parasitics
 - Variations in die ageing
- **Impact:** Alters impedance, current demand, hurts reliability



Data extracted from ITRS 2005



Cu Thickness Variation

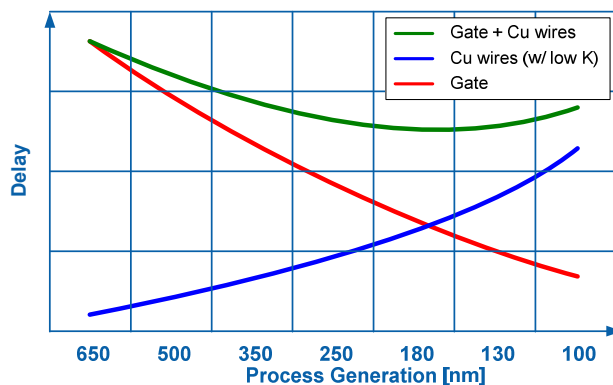


ILD Thickness Variation



Technology Trends (contd.)

- Delay Trends
 - ↓ Gate delay, ↑ Wire delay
 - ↑ Cross-chip communication
- Performance demands continue

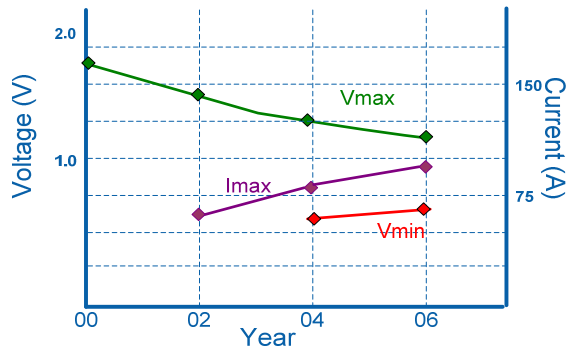


Wire & gate delay trends

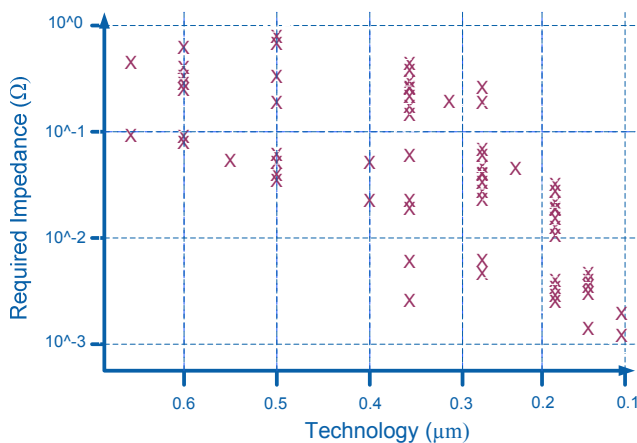


Technology Trends (contd.)

- Intel's "Right Hand Turn"
 - Power is \$\$
 - "Power Wall" driving reduction in voltage
 - Dynamic power = $\alpha C V^2 F$
- V_{MIN} relatively constant
 - \downarrow Operating range
 - \downarrow Noise margins



Technology Trends (contd.)



Impedance Rqmts. For High Performance MicroProcessors

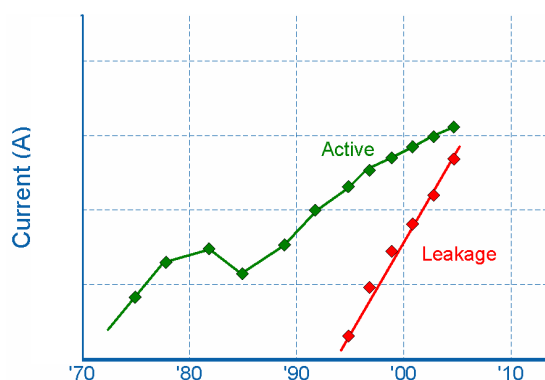
ISTR RoadMap
July 31st 2007

- Impedance scaling:
 - Drastic drop in supply impedance
 - Even at constant power
 - $V_{dd} \downarrow$, $I_{max} \uparrow$
 - $|Z_{required}| \downarrow \downarrow$
 - Today's chips: $|Z_{required}| \approx 1 \text{ m}\Omega$
 - Supply voltage becoming noisy as result



Technology Trends (contd.)

- Leakage power
 - Increasing
 - Constant demand on power delivery system
 - Reliability impact



Leakage & Active Current Trends

Challenge: Efficient power delivery while:

- Minimizing power consumption
- Optimizing heat dissipation



Some Other Trends

Economy

- Electronic device presence multiplying
- Energy consumption increasing
- Energy costs rising
 - We all have an electricity bill to pay at the end of the month



Sociology & environment

- Global warming awareness



What exactly is Power & Energy ?

Power

- Rate at which work is done, expressed as amount of work per unit of time in Watts
- In a microprocessor:
 - Power consumed = dynamic power + leakage power
 - $P = (P_{\text{switch}} + P_{\text{sc}} + P_{\text{cont}} + P_{\text{glitch}}) + P_{\text{leak}}$
 - $P = (\alpha C V^2 F + P_{\text{sc}} + P_{\text{cont}} + P_{\text{glitch}}) + V I_{\text{leak}}$
 - α activity factor
 - C switching capacitance
 - V power supply voltage
 - F clock frequency
 - V_t threshold voltage
 - $I_{\text{leak}} \sim \exp(-qV_t/kT)$ leakage current

Energy

- Total amount of work done expresses in Joules
 - Power * Time = Energy

Which one do we aim at lowering: Energy or Power or BOTH?



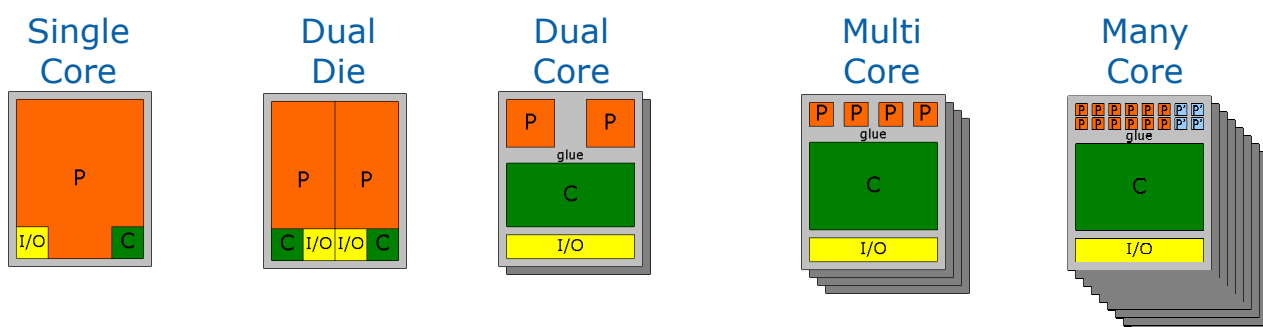
Current Design Solutions

- Multiple voltage domains on-die
 - Trick used to reduce power while maintaining performance
 - Cache voltage lower than core/uncore voltage
 - Cache mainly needs to hold state
 - Speed critical for execution units, overall communication etc → leads to higher voltage requirements here
 - Impact
 - Overall grid metal available per domain reduced
 - May need to compromise grid requirements depending upon distribution of voltage domains



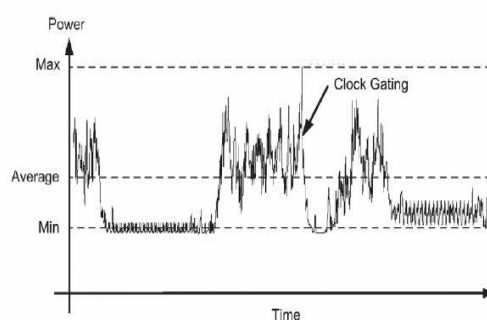
Current Design Solutions

- Multi-core trend
 - Attractive for throughput based solutions
 - Enables reduction in power consumption while maintaining throughput
 - Dynamic power = CV^2F
 - Power = 1Core @ $V, F \sim 2$ Cores @ $0.8V, 0.8F$



Current Design Solutions

- Active power management techniques
 - V/f scaling
 - Multiple operating modes for various benchmarks
 - Clock gating & power down mechanisms
 - ➔ Higher I_{STEP} ($I_{MAX} - I_{MIN}$)
 - Power gates



SUN Microsystems CPU Sample Current Profile

Source: Harris, Addison-Wesley '05



Is it sufficient ?

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2015 Likely Scenario

5 Billion Connected People

Always On

In Pursuit of Killer “Experiences”

Network Capacity?

100 Tbits/sec Today. 100,000 Tbits/sec Needed.

*That is **1000x** Increase!*

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That's a lot of power!



Summary

- Technology trends in nano-era have elevated our power and reliability challenges
- Call for action: We need to be able to develop easy and revolutionary techniques to counter this in the increasing world of complicated microprocessor design
 - Plenty exist....but not sufficient
- Plenty of opportunities for research



Talk to/email me for further input/questions

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