

Traffic Pattern Characterization of Chip-Multiprocessor (CMP)

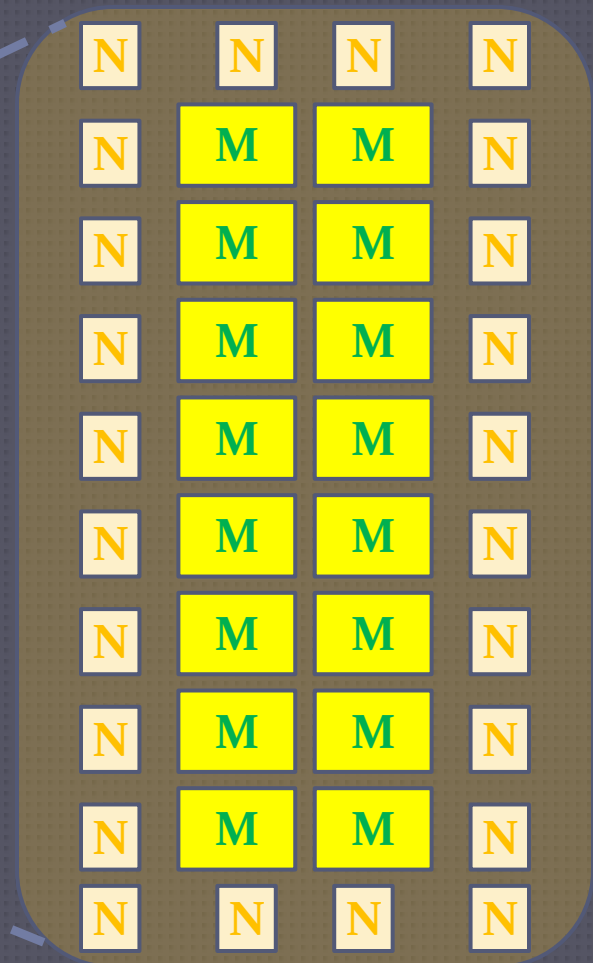
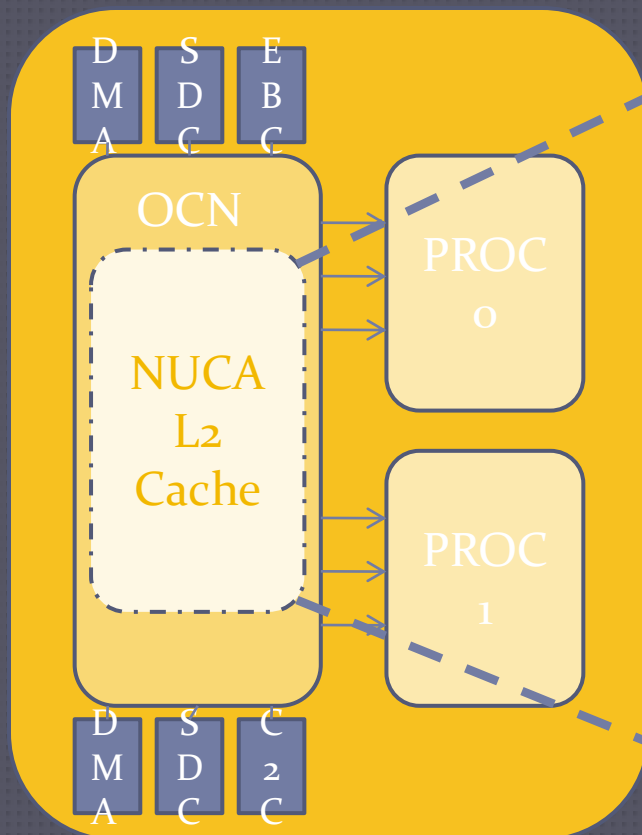
Presented by Carole-Jean Wu

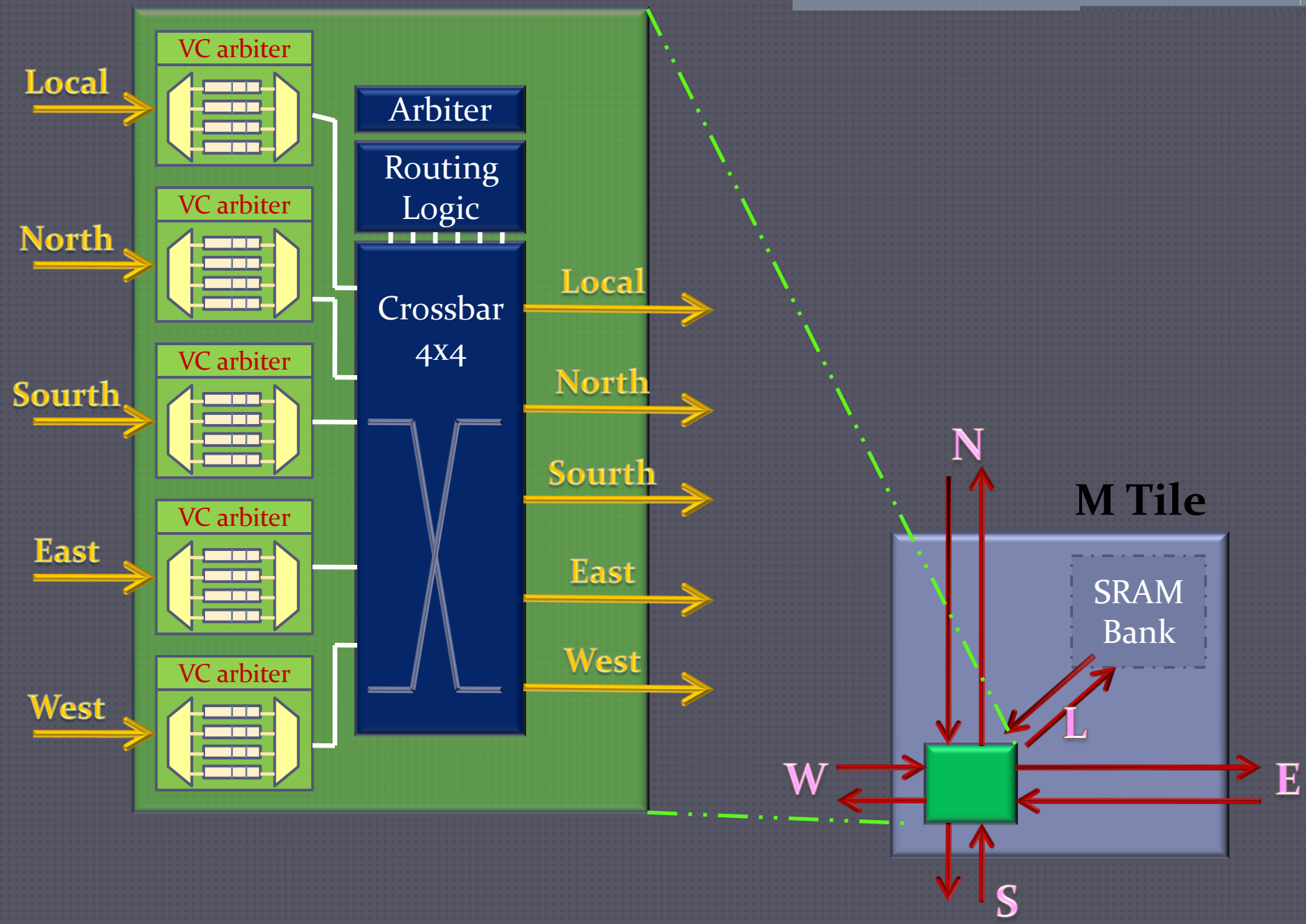
Overview

- OCN Architecture
 - Austin TRIPS
- Network Simulator
 - Design Specification
 - Experimental Results
- Conclusion

OCN Architecture

TRIPS On-Chip Network (OCN)





Network Simulator

Design Specification - Router

- Incoming packets are latched into the input FIFOs
 - Packets range in size from 16 bytes to 80 bytes long
 - Broken into 1 to 5 16-byte flits
 - 16-flit input channel available in each direction
- 4x4 crossbar connecting each input to every possible output
 - In the case of contention, use round-robin to ensure fairness and livelock avoidance

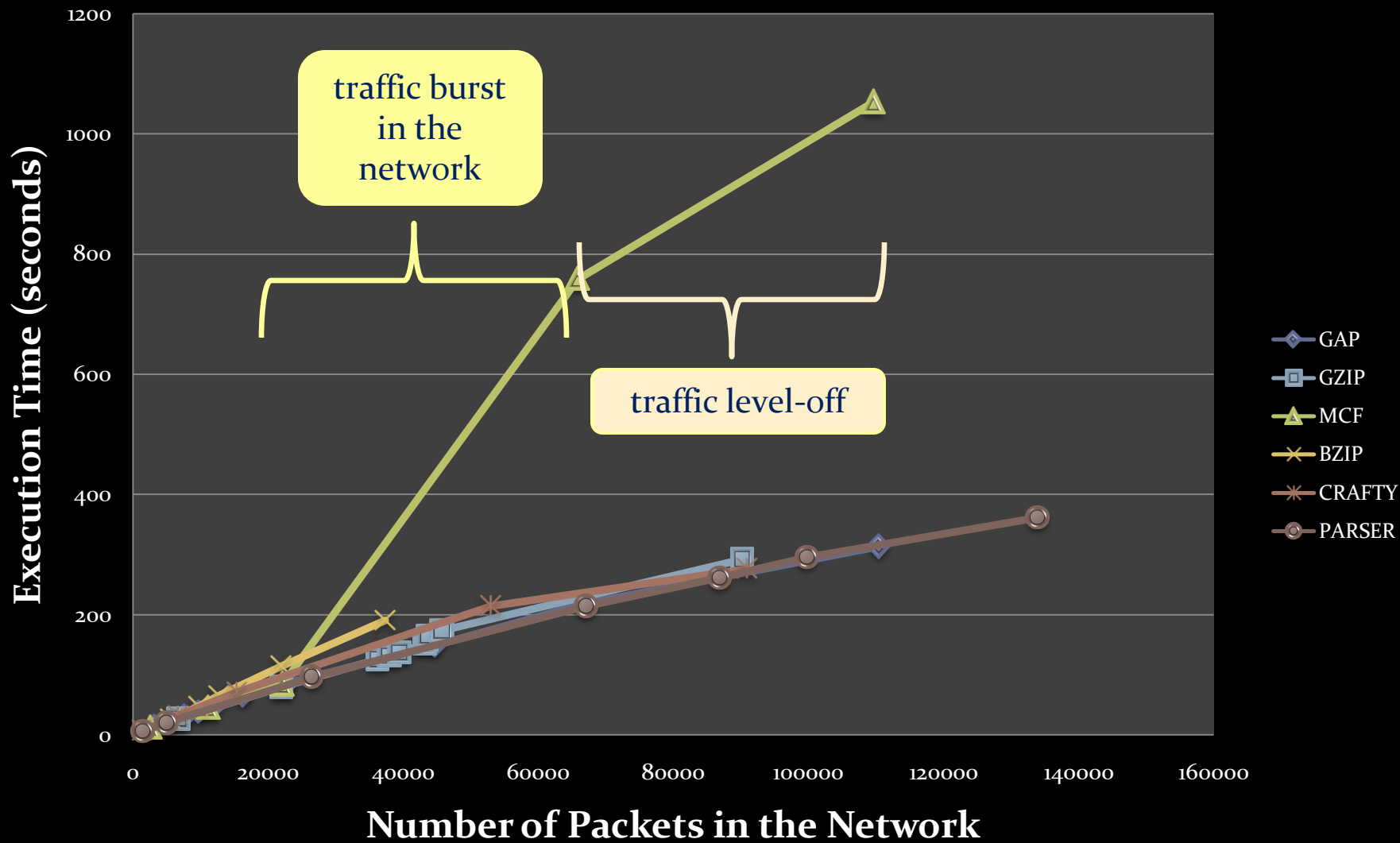
Design Specification - Router

- Credit-based flow control
 - Tracks the number of available buffers in neighboring receiver FIFOs
 - Takes flow control off the packet transmission critical path

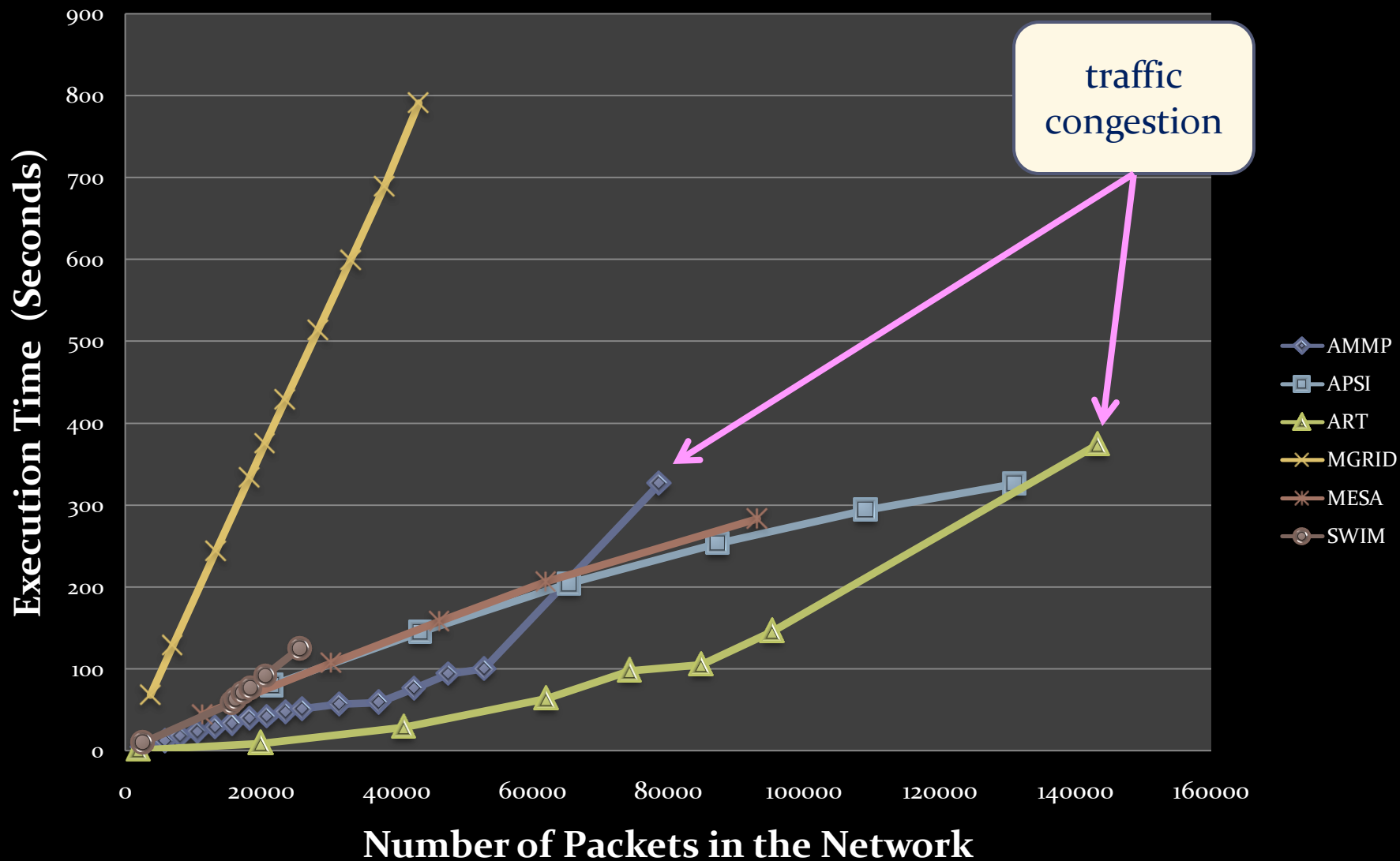
Design Specification - Router

- 4 by 10 Mesh Network
- Store and Forward, Y-X Dimension-order Routing
- Credit-based Flow Control

Simulation Results SPEC INT 2K



Simulation Results SPEC FP 2K



Conclusion

- Traffic congestion (due to L2 cache accesses) does not occur often for CPU-bound applications
 - Memory –bound application is affected more seriously
- Current configuration provides
 - balanced work load
 - smooth traffic (linear) most of the time

Special Thanks

- Paul Gratz (UT-Austin) for providing OCN traces and explanations of OCN design scheme
- Li-Shiuan for guidance
- Yuyuan, Kostas, and Manos for inspirations & lots of 😊 & fun!