

# CAROLE-JEAN WU

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## Research Interests

- Computer architecture: chip-multiprocessors (CMPs) with an emphasis on the last-level cache (LLC)
- Shared resource management for CMP and many-core systems
- Performance characterization, analysis and prediction for CMPs
- High performance and power-efficient LLC designs

## Education

**Princeton University** 5/2012 (expected)

*Ph.D. candidate in Electrical Engineering*

*M.A. in Electrical Engineering* 5/2008

Advisor: Prof. Margaret Martonosi

Dissertation: Dynamic Techniques for Mitigating Inter- and Intra-Application Cache Interference

**Cornell University** 5/2006

*B.S. in Electrical and Computer Engineering*

Dean's List: 2003 2004 2005; Cum Laude Honors

Advisor: Prof. José Martínez

Undergraduate Honor Thesis: Predictability of Microprocessor L2 Cache Miss Values

## Honors and Awards

- Intel Ph.D. Graduate Fellowship 2011-12  
A prestigious award given to 21 outstanding Ph.D. students in semiconductor research
- Excellence in Leadership Award from Computer Architecture Day @ Princeton 2009
- First Year Graduate Fellowship from Princeton University 2006-07
- Undergraduate Research Funding from Intel Corporation (CURB) 2005-06
- Best COOP Student of Year from Cornell's ECE Department 2005-06  
A departmental award given to the most outstanding student in the cooperative internship program

## Conference and Journal Publications

**Carole-Jean Wu**, Amer Jaleel, Margaret Martonosi, Simon Steely Jr., and Joel Emer.

PACMan: Prefetch-Aware Cache Management for High Performance Caching.

In *Proceedings of the 44<sup>th</sup> International Symposium on Microarchitecture (MICRO-44)*. December 2011.

**Carole-Jean Wu**, Amer Jaleel, Will Hasenplaugh, Margaret Martonosi, Simon Steely Jr., and Joel Emer.

SHiP: Signature-Based Hit Predictor for High Performance Caching.

In *Proceedings of the 44<sup>th</sup> International Symposium on Microarchitecture (MICRO-44)*. December 2011.

**Carole-Jean Wu** and Margaret Martonosi.

Characterization and Dynamic Mitigation of Intra-Application Cache Interference.

In *Proceedings of IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*.

April 2011. **Best Paper Award Nominee**

**Carole-Jean Wu** and Margaret Martonosi.

Adaptive Timekeeping Replacement: Fine-Grained Capacity Management for Shared CMP Caches.

In *Proceedings of ACM Transactions on Architecture and Code Optimization (TACO) Vol. 8, Issue 1, Article 3*.

February 2011.

**Carole-Jean Wu** and Margaret Martonosi.

A Comparison of Capacity Management Schemes for Shared CMP Caches.

In Proceedings of the *7th Annual Workshop on Duplicating, Deconstructing, and Debunking*, in conjunction with ISCA-35, June 2008.

## Work Experience

9/2010 - 5/2011 **Intel Graduate Intern Technical**

**Intel Corporation (IAG-CAP-VSSAD)** *Hudson, MA.* Manager: Aamer Jaleel/Joel Emer

- Proposed instruction-level, signature-based cache hit predictors to guide cache replacement.
- Designed novel high performing memory management techniques to improve cache utilization for multimedia, games, enterprise servers, and scientific workloads.
- Submitted two papers to International Symposium on Microarchitecture (MICRO).

6/2009 - 8/2009 **Google Platform Engineering Intern**

**Google Inc. (Platforms Development)** *Mountain View, CA* Manager: Chris Sadler

- Developed a portfolio of application-level power prediction algorithms for data centers. This portfolio includes machine learning algorithms and linear regression techniques that exploit application CPU/power utilization history as well as algorithms that simply react to demand.
- Analyzed Google benchmark and random CPU utilization traces sampled in a production environment. Evaluated the effectiveness in prediction accuracy and usability of the studied algorithms for representative workloads.

6/2008 - 8/2008 **Intel Graduate Intern Technical – System Engineer**

**Intel Corporation (CTG - STL- PSL)** *Portland, OR.* Manager: Matthew Hoekstra

- Analyzed performance and scalability issues related to System Management Mode (SMM) on Intel's many-core and Tera-scale platforms.

6/2007 - 8/2007 **IBM Research Intern**

**IBM TJ Watson Research Center, Hawthorne, NY.** Manager: Evelyn Duesterwald

- Created the visualization software, TuningFork, for large-scale multicore systems.

5/2005 - 8/2005 **Intel Technical Intern – Software Engineer**

**Intel Corporation (SSG - AET- ATP)** *Chandler, AZ.* Manager: Chuck Yount

- Profiled and characterized threading behaviors of various applications using Intel ThreadTracker, Thread Profiler and VTune performance analyzer.
- Generated multi-threaded traces for IA32 pre-Si simulations for various applications, validated traces were representative, and performed pre-Si architectural analysis.

8/2004 - 12/2004 **Intel Technical Intern – Software Engineer**

**Intel Corporation (SSG - AET- ATP)** *Chandler, AZ.* Manager: Chuck Yount

- Built RT viewer, a graphical tool, which characterizes threading behavior of an application in the pre-Si environment in a multi-core/multi-processor system.
- Debugged a media decoder for Microsoft and analyzed performance using Intel VTune performance analyzer.

## Teaching Experience

9/2011 – 12/2011 **Teaching Transcript Program**

McGraw Center for Teaching and Learning, Princeton University, *Princeton, NJ*

- Completed pedagogy programs and obtained Assistant in Instruction certificate.
- Enhanced my teaching skills via classroom observation and feedback sessions.

2/2009 - 5/2009

**Assistant in Instruction**

Electrical Engineering Department, Princeton University, *Princeton, NJ*

- Prepared precept sessions, assignments, and exams for “ELE391 Wireless Revolution: Telecommunications for the 21st Century” (~150 students).
- Held homework sessions and office hours to reinforce student learning.

8/2003 - 12/2005

**Academic Excellence Workshop Facilitator**

Life Program Office, *Cornell University, Ithaca, NY*

- Led enrichment workshops for calculus classes and promoted group learning for better understanding of course materials.

6/2004 - 8/2004

**Teaching Assistant for Pre-Freshman Program**

Math Department, *Cornell University, Ithaca, NY*

- Prepared undergraduate Calculus lesson plans, lectured the pre-freshman.

## Skills and Languages

- Verilog, C, C++, Java, Assembly, Unix, Perl
- PSPICE, Capture CIS, MATLAB, Intel VTune analyzer, ThreadTracker, ThreadProfiler, Pipetrace Viewer, TuningFork
- ATOM analysis tool, BOCHS emulator, SESC, GEMS, and CMP\$im system simulators
- BIOS, Extensible Firmware Interface (EFO) -- TIANO

## Technical Talks

- 11/2011      **Computer Architecture 101— Multi-Level Caches: How to Design Them?**  
Seminar designed to introduce the dynamics between computer processors and cache memory, critical challenges faced by computer architects, and future research topics for juniors and seniors.
- 11/2011      **Characterizing and Improving Last-level Cache Management using Signature-based and Prefetch-aware Approaches**  
Invited talk given to industry liaisons and academia researchers at the GigaScale Systems Research (GSRC) e-seminar.

## Professional Activities

- 5/2008 – Present **Member of IEEE and ACM**
- 9/2007 – Present **Co-founder of Princeton’s Computer Architecture Reading Group**
- 3/2007 – Present **Student Researcher, GigaScale Systems Research Center (GSRC)**
- 5/2005 – 5/2006 **Vice President of HKN**  
Eta Kappa Nu, Electrical and Computer Engineering Department, *Cornell University, Ithaca, NY*
- Conducted tutoring programs and clarified issues of subject matter for students major in Electrical and Computer Engineering.

## Conference and Journal Reviews

- IEEE/ACM International Symposium on Computer Architecture (ISCA)
- IEEE/ACM International Symposium on Microarchitecture (MICRO)
- IEEE International Symposium on High Performance Computer Architecture (HPCA)
- ACM International Conference on Computer Frontier (CF)
- ACM Transactions on Architectures and Code Optimization (TACO)

## References

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