X-ray lithography for sub-100-nm-channel-length transistors using masks fabricated with conventional photolithography, anisotropic etching, and oblique shadowing

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In order to fabricate submicrometer-channel-length MOSFET's using x-ray lithography, a novel mask fabrication technique was developed. The mask enabled PMMA lines with widths of 100, 160, 250, 270, and 5000 nm to be exposed simultaneously on the same substrate. The mask consists of a polyimide membrane with narrow absorber lines on the front side (facing the substrate) and coarse absorber patterns on the back side (facing the x-ray source). The narrow absorber lines are formed by oblique shadowing of gold onto sidewalls of rectangular mesas molded on the polyimide from wells anisotropically etched in (110)Si. As a result, exposed lines are straight, controlled in width to $\sim 10\%$, and have very small edge ripple. Source and drain pattern areas are formed in gold on the back surface of the membrane by conventional photolithography and ion beam etching. PMMA lines exposed with the x-ray mask were used for channel masking during source–drain ion implantation. Operating MOSFET's were fabricated with minimum channel length estimated to be 75 nm.

I. INTRODUCTION

As part of a project to study short-channel effects in MOSFET's (metal-oxide–semiconductor field-effect transistors) we have developed an x-ray lithographic technique that enables the resist lines, which mask the channel regions during ion implantation of the source and drain, to be varied in width on the same substrate from $\lesssim 100$ nm to $5\,\mu$m. The x-ray mask fabrication does not involve electron-beam lithography, but instead uses conventional photolithography, anisotropic etching, and oblique shadowing. A novel feature of the technique is that x-ray absorber patterns are formed on both front (facing the substrate) and back (facing the x-ray source) surfaces of the x-ray mask, as illustrated in Fig. 1. Figure 2 illustrates schematically the steps in the fabrication of the x-ray mask. They are anisotropic etching of crystallographically aligned rectangular wells in (110)Si through rectangular windows in SiO_2; spinning of polyimide over the (110)Si; formation of an Au absorber pattern on the polyimide; attachment of an aluminum ring to the polyimide and removal of the Si by chemical etching; and shadow evaporation of Au onto crystallographically smooth mesa sidewalls. These steps will now be described in detail.

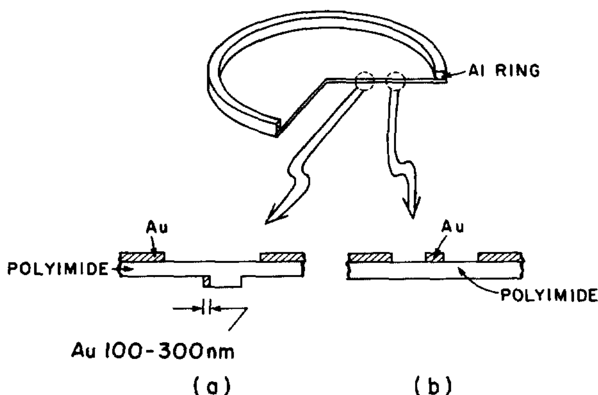

FIG. 1. Schematic of x-ray mask. (a) Absorber pattern for submicron MOSFET, on both front and back surfaces. (b) Absorber pattern for $5\,\mu$m-channel-length MOSFET, on back side only.

II. FORMATION OF CRYSTALLOGRAPHICALLY ALIGNED RECTANGULAR WELLS

Thermal SiO_2 was grown on a (110)Si wafer. In order to ensure accurate crystallographic orientation we first etched anisotropically nine pairs of alignment marks in the Si, using

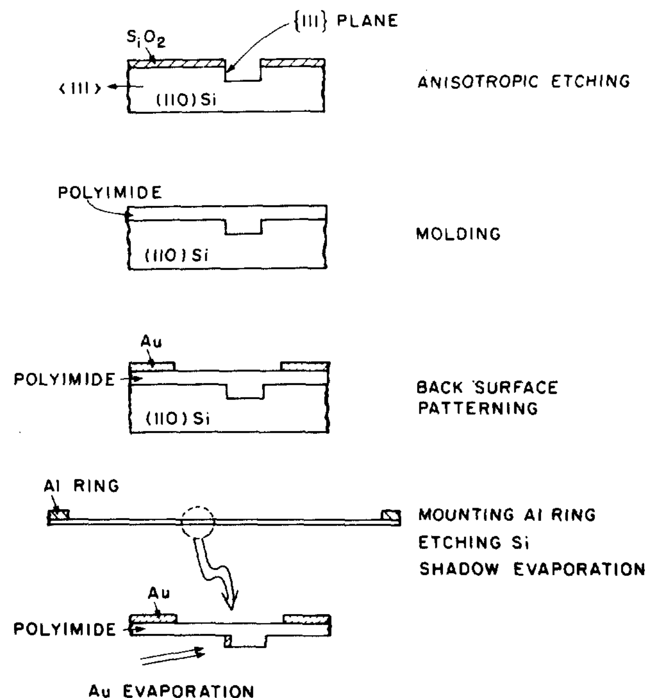

FIG. 2. Illustration of the steps involved in making x-ray mask.

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SiO_2 as a mask. Alignment mark spacing and geometry were chosen for compatibility with a GCA DSW-4800 optical projection lithography system. Each pair of alignment marks consists of crosses on opposite sides of the pattern area, 38.1 mm apart, and, associated with each cross, two small rectangular boxes. Each pair of alignment marks is rotated relative to its neighbor by 0.5°. The anisotropic etching of alignment marks was carried out at 80 °C in a KOH/isopropyl alcohol/H_2O solution with volume ratios 3:2:8. The etch rate in a ⟨110⟩ direction is about 10 times faster than in a ⟨111⟩ direction. The addition of isopropyl alcohol to the KOH/water solution yields etched structures having flat bottoms[1] with faint striation running in the $[1\bar{1}0]$ direction in the (110) plane [i.e., the lines of intersection of the inclined {111} planes with the (110) plane]. After anisotropic etching, inspection of the boxes in an optical microscope readily reveals which pair of alignment marks has the optimal orientation. That is, for the optimal pair, sidewalls are smooth and the striations at the bottom of the etched boxes run at an angle of 54.7° to the sidewalls, indicating that the axes of boxes are most nearly parallel to a ⟨112⟩ direction in the Si(110) plane. This optimal pair of alignment marks is used in exposing the window patterns and in all subsequent lithography. Because of the good crystallographic alignment, two sidewalls of the etched wells are essentially {111} planes and hence vertical and extremely smooth (on a scale less than 10 nm) despite considerable raggedness in the edges of the SiO_2 windows. This is illustrated in Fig. 3.

III. BACK SURFACE PATTERNS

After etching the rectangular wells, the SiO_2 was removed and a polyimide layer (DuPont PI-2555) about 1 μm thick was spun on the Si, and cured.[2] Other membrane materials could, of course, be used in place of polyimide. A film consisting of 10 nm of Cr and ~150 nm of Au was then evaporated onto the polyimide. This layer was patterned using optical projection photolithography and ion beam etching. The resulting back-surface patterns consist of rectangular openings in Au centered over one of the {111} sidewalls of the wells in the Si. In addition to these rectangles, which are used to define areas for source and drain implants of submicron MOSFET's, pairs of rectangles separated by 5 μm are also formed in separate areas on the back surface. These produce 5-μm-channel-length MOSFET's.

IV. SHADOW EVAPORATION

An aluminum ring was bonded to the polyimide using epoxy, and the (110)Si substrate etched away in a HF/HNO_3 solution. This leaves rectangular mesas on the front side of the polyimide membrane. The absorber lines on the front side are formed by oblique evaporation of gold onto one of the mesa sidewalls (so-called shadow evaporation). The narrow absorber lines that result split the rectangular patterns on the back surface into source and drain regions. The contrast of the front-surface absorber is determined by the depth to which the original wells were etched in the (110)Si. We used a depth of 0.2 μm, which corresponds to 25 dB attenuation for gold at the C_K x-ray wavelength (4.5 nm).[3] This is well in excess of the contrast needed to expose fine patterns in PMMA, which has a development rate proportional approximately to the third power of dosage.[4]

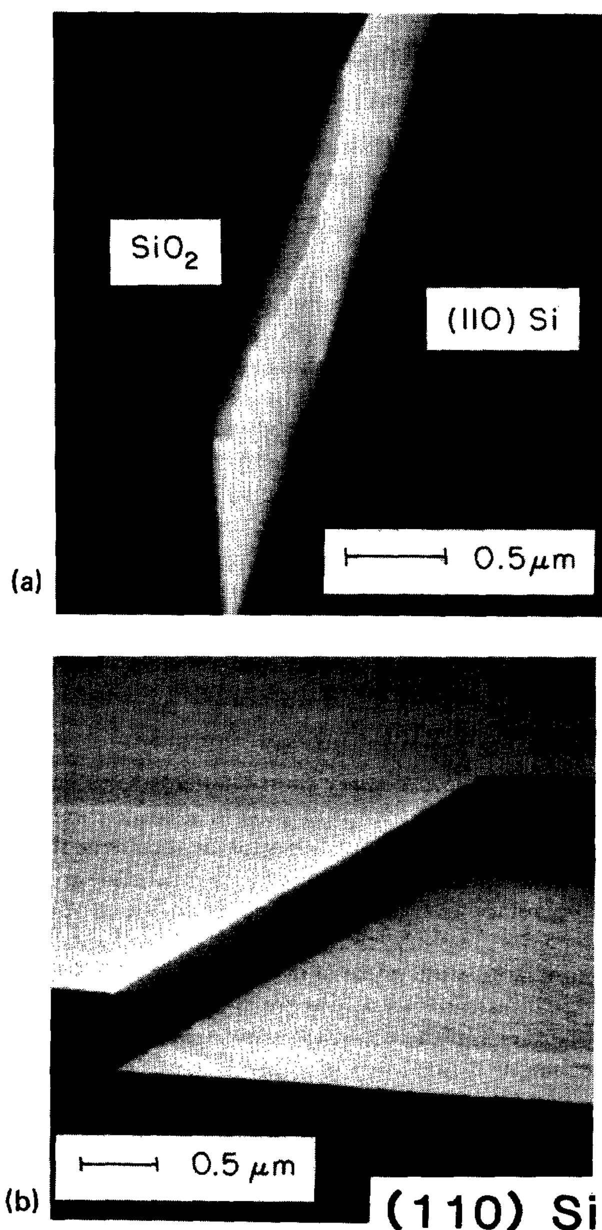

FIG. 3. (a) Anisotropically etched well in (110)Si, before removal of SiO_2 mask. Note edge raggedness of SiO_2. (b) After removal of SiO_2 mask. Note sidewall smoothness and that the well bottom is flat.

The linewidth is determined by the amount of gold deposited on the mesa sidewalls. In our work we deposited gold to four different thicknesses (100, 160, 250, and 270 nm) in separate regions of the mask. The angle of deposition was 4° in all cases which gave predictable coatings on sidewalls and flat regions. Angles lower than this frequently led to nonuniform deposits on the flat regions of the membrane. After sidewall shadowing, excess gold is removed from the flat regions by ion-beam etching.

V. EXPOSURE

Exposures were carried out with the C_K x ray ($\lambda = 4.5$ nm). The mask was held in intimate contact with the sub-

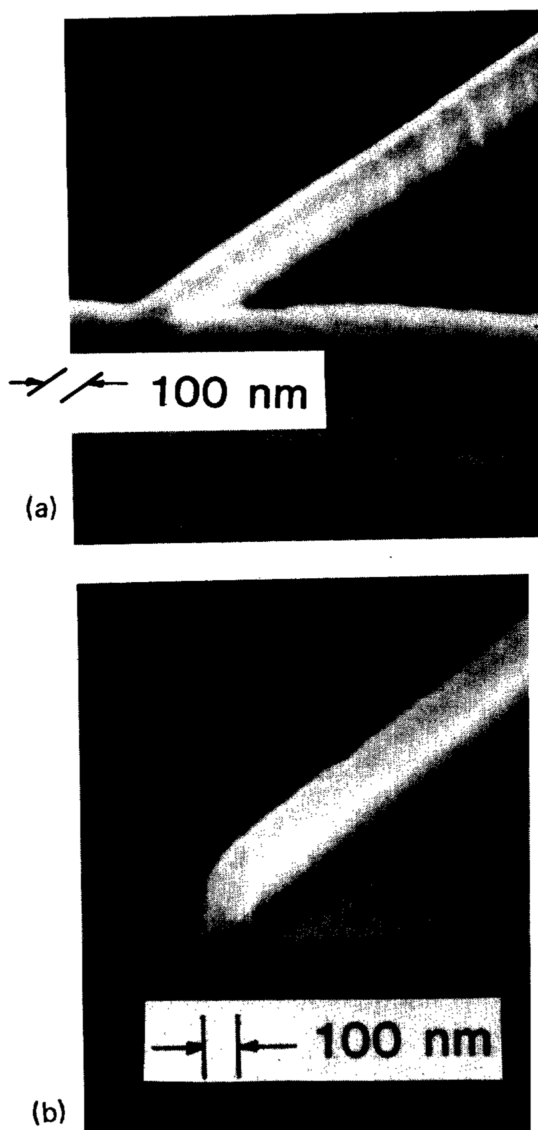

FIG. 4. (a) Scanning electron micrographs of PMMA resist pattern used as mask during source–drain ion implantation. (b) Cross section of PMMA line used as channel mask.

strate by electrostatic means. This gave well-defined resist structures, as illustrated in Fig. 4. Because the mesa sidewalls are smooth, on the scale of 10 nm or less, resist lines are straight and nearly free of ripple. What ripple does occur is probably due to granularity of the evaporated Au. The height of the resist line is 250 nm, which is adequate to mask implantation with As ions at 30 keV.

Note that this technique does not provide for self-alignment of gate and channel. That is, a PMMA resist structure masks the implantation, not a gate as in the conventional process. The capacitance due to overlap of the gate with the source and drain did not pose a problem since our initial interest was in low frequency characterization of the short-channel devices. We believe the process can be modified to achieve self-aligned gates.

Operating MOSFET's with estimated minimum channel lengths of 75 nm (original PMMA width of 235 nm) have been fabricated using the process described here. Results will be reported elsewhere.[5]

VI. CONCLUSIONS

We have described a method for fabricating x-ray masks used in a process for fabricating sub-100-nm-channel-length MOSFET's. Coarse patterns are formed on the back side of the mask membrane using conventional photolithography and ion-beam etching, and fine-line patterns are formed on the front side using oblique shadowing onto sidewalls of mesas formed by molding in wells anisotropically etched in (110)Si. The C_K x ray was used for exposure, yielding PMMA lines suitable for ion-implant masking. These lines were extremely straight with very small ripple. Linewidths were controlled within 10% accuracy and varied from 100 nm to 5 μm on the same substrate. Operating MOS transistors were fabricated with minimum channel lengths estimated to be 75 nm.

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