

due primarily to the low output conductance. The present devices exhibited an on/off current ratio of $\sim 10^4$ and a drain-gate breakdown voltage of 7V, apparently limited by gate leakage current (single channel 2D MESFET breakdown voltages of 20V will be reported elsewhere [8]). The S-parameters were measured using an HP 8510C network analyser up to 50GHz. A conventional microwave small signal circuit model was used for parameter extraction and de-embedding. The extracted parameters were relatively constant over the frequency range of interest and in good agreement with those values obtained at DC. The unity-gain cutoff-frequency f_T was 14GHz and f_{max} was 45GHz, the highest values yet reported for such structures.

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Stacked quantum dot transistor and charge-induced confinement enhancement

L.J. Guo and S.Y. Chou

A new quantum dot transistor that has a polysilicon dot floating gate stacked on top of a silicon quantum dot channel has been fabricated. It is observed that charging of the floating gate not only shifts the threshold voltage of the quantum dot transistor, but also significantly increases the peak-to-valley ratio and peak separation in the conductance oscillations.

As the size of a transistor continuously scales down, single electron effects become important [1–3]. Previously, we have studied charge transport in single-electron quantum dot transistors which have a channel consisting of a silicon dot separated from the source and the drain by two constrictions [4], and in single-electron MOS memories that have a polysilicon dot floating gate

stacked on a straight channel [3]. In this Letter, we propose and demonstrate a novel stacked quantum dot transistor (QDT) that has a polysilicon dot floating gate stacked on top of a silicon dot channel, and report how transport through the silicon dot channel can be affected by the charges stored in the floating dot gate. We have observed that the peak-to-valley ratio and the peak separation of the conductance were enhanced after charging the electrons into the floating gate. This effect is explained as a result of the enhanced charge confinement in the silicon quantum dot channel.

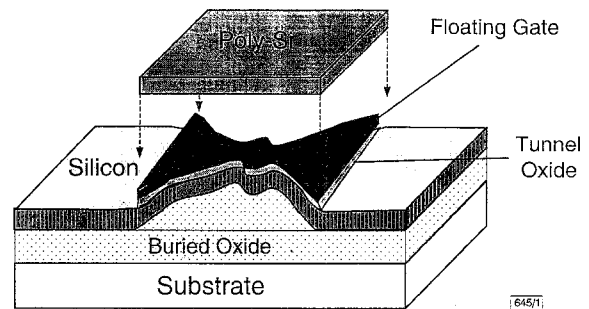


Fig. 1 Schematic diagram of stacked quantum dot transistor fabricated on SOI wafer

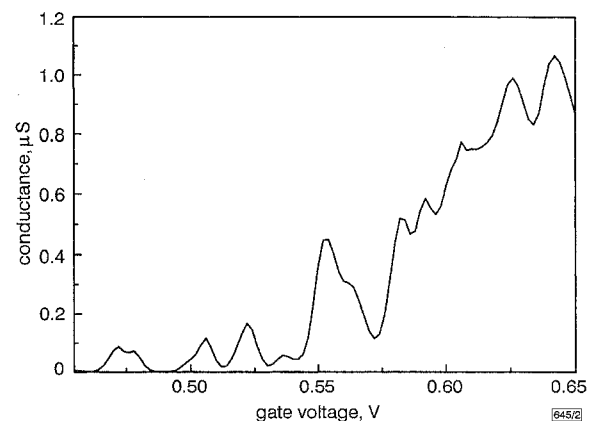


Fig. 2 Conductance oscillations of stacked QDT taken at 4.2K before floating gate was charged with electrons

A schematic diagram of the device structure is shown in Fig. 1. It has a silicon quantum dot channel similar to that which we have demonstrated previously [4], and a polysilicon dot stacked on top of the Si dot channel as a floating gate. The device was fabricated on a silicon-on-insulator (SOI) wafer, with a boron doping of $3 \times 10^{15} \text{cm}^{-3}$ in the 35nm thick silicon layer. The first step of the fabrication process was the growth of 10nm thick chemical-vapour-deposited (CVD) polysilicon on the SOI wafer, with a layer of $\sim 1 \text{nm}$ thick native oxide sandwiched inbetween. The silicon dot channel and the polysilicon floating gate were defined using electron beam lithography, and were etched in a self-aligned manner using chlorine reactive ion etching. Next, the sample was oxidised, which partially consumed the silicon in the channel and the polysilicon in the floating gate, leaving the Si dot with a diameter of $\sim 40 \text{nm}$ and the polysilicon film with a thickness of $\sim 5 \text{nm}$. Next, a CVD oxide was deposited to give a total control oxide thickness of 36nm. The rest of the process is similar to our earlier work on silicon quantum dot transistors.

The conductance against gate voltage characteristics taken at 4.2K (Figs. 2 and 3) shows the Coulomb blockade oscillations [5] of a stacked QDT before and after the floating gate was charged with electrons. It can be seen that after charging, not only had the threshold voltage of the transistor shifted ($\sim 0.3 \text{V}$), but the oscillation peaks were also enhanced and more well separated. Since the peak width is primarily due to thermal broadening, the full width at half maximum (FWHM) of the peak in terms of gate voltage can be related to temperature T as $\alpha(\text{FWHM}) = 3.5k_B T$ [6], where k_B is the Boltzman constant, and α is a scaling factor that converts the gate voltage (V_G) to the energy (E): $\alpha = \delta E / \delta V_G$. Using α , we found that the typical energy level separation (ΔE) had increased from 2.5 to 5.5meV after charging – an increase by a factor of two. Furthermore, the charge can be held in the floating gate for many days.

Further evidence of the increase in energy spacing in the dot channel is the decrease in valley current (I_v) when more electrons are charged into the floating gate, as shown in Fig. 4, where the valley positions are indicated for three different charge densities on the floating dot gate. Since $I_v \propto \exp(-\Delta E/2kT)$, the reduction in the valley current implies the increase in energy level separation.

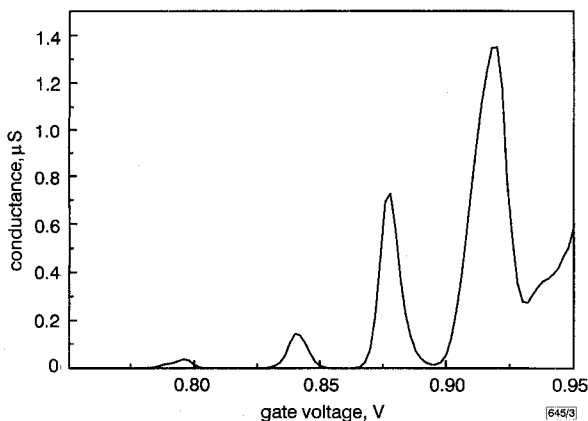


Fig. 3 Conductance oscillations of stacked QDT taken at 4.2K after floating gate was charged with electrons

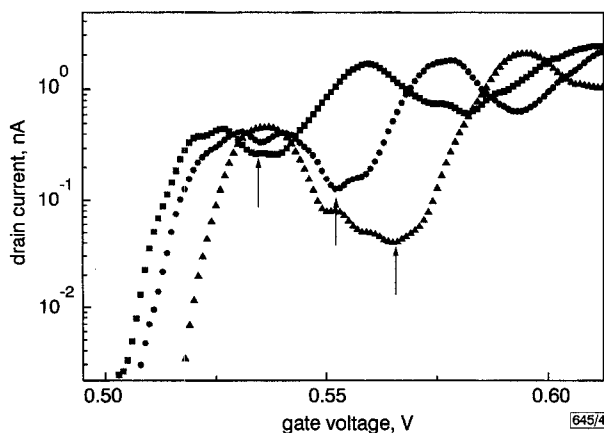


Fig. 4 Drain current against gate voltage, showing decrease of valley current with charging of floating gate

Charging carried out by applying 10ms, 13V pulses to control gate
 ■ 5 pulses
 ● 10 pulses
 ▲ 15 pulses
 Source drain bias: 1.2mV

In this case, incremental charging was performed by applying a series of voltage pulses of 13V to the control gate. The increase in energy level separation was estimated to be 1.5 and 2.3meV after each incremental charging. Both observations indicate that charging of the floating gate can enhance the charge confinement in the Si dot. This process is also reversible: after the electrons were removed from the floating gate, the transistor's I-V characteristics returned to its original behaviour before charging.

Such an effect can be attributed to the Coulomb interaction between the electrons in the floating gate and those in the Si channel dot. Before the floating gate is charged, the electrons in the channel dot can distribute throughout the vertical direction of the thin silicon film, owing to volume inversion formed near the threshold [7]. However, when the negative charges are stored in the floating gate, because of the Coulomb repulsion, the channel electrons are depleted away from the interface between the silicon channel and the tunnel oxide. That is, the electron distribution in the channel dot was compressed, leading to a smaller effective quantum dot. In this case, the Coulomb charging energy increases as a result of the effective size reduction of the quantum dot.

In conclusion, we have demonstrated a quantum dot transistor with a polysilicon dot floating gate stacked on top of an Si dot channel. By charging the floating dot, not only can the threshold voltage of the transistor be shifted, but also the conductance oscillations in the quantum dot channel can be greatly enhanced. Such

an enhancement is attributed to the reduction of the effective quantum dot size, which leads to an increase in energy level separation.

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Surface recombination related frequency dispersion of current gain in AlGaAs/GaAs HBTs

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The dispersion effect of current gain related to surface recombination in AlGaAs/GaAs HBTs has been studied. For an HBT with an emitter area of $3 \times 20 \mu\text{m}^2$, the surface recombination current-to-total base current ratio is ~ 0.47 at $< 100\text{MHz}$, and the ratio is decreased to zero at frequencies between 100MHz and 3GHz, clearly indicating that the current gain is dispersive.

Introduction: AlGaAs/GaAs heterojunction bipolar transistors (HBTs) are applicable for high speed digital and microwave circuits. In order to obtain the required high f_i and f_{max} , emitter size reduction is essential. As the emitter size decreases, surface recombination at the emitter periphery increases and current gain also decreases. Many studies have attempted to characterise the base surface recombination current effect [1, 2]. However, few reports are available on the frequency-dependence of this current component. In fact, the frequency dispersion of output resistance (R_o) and transconductance (g_m) of GaAs MESFETs have been investigated by many authors, and these phenomena are explained by surface-states [3, 4]. In this work, we report that HBTs also have current gain dispersion which is related to surface recombination.

Device structures and measurements: The MOCVD-grown epi-layer structure has a 700Å thick, 30% Al mole fraction emitter layer and 1000Å thick carbon-doped base layer. The emitter, base, and collector dopant concentrations are 2×10^{17} , 2×10^{19} , and $2 \times 10^{16} \text{cm}^{-3}$, respectively. Several different sized HBTs are fabricated by a conventional MESA-type self-aligned base metal HBT process without adopting any surface passivation. Devices with four different emitter sizes were measured; 4×30 , 4×10 , 3×30 , and 3