

Observation of electron resonant tunneling in a lateral dual-gate resonant tunneling field-effect transistor

S. Y. Chou, D. R. Allee, R. F. W. Pease, and J. S. Harris, Jr.

Department of Electrical Engineering, Stanford University, Stanford, California 94305

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A new lateral resonant tunneling field-effect transistor (LARTFET) has been fabricated using molecular beam epitaxy and ultrahigh-resolution electron beam lithography. The LARTFET has two 80-nm-long gate electrodes separated by 100 nm. The dual gates create double potential barriers in the channel and a quantum well in between. Conductance oscillations are observed, which, for the first time, indicate electron resonant tunneling through the energy states in a lateral double-barrier quantum well formed electrostatically. Furthermore, after illumination, two additional negative transconductance peaks are observed. These additional peaks may be related to electron resonant tunneling through the donor-related deep levels in silicon-doped $\text{Al}_{0.35}\text{Ga}_{0.65}\text{As}$.

Resonant tunneling (RT) diodes have exhibited their potential applications in ultrahigh-speed circuits.^{1,2} However, for circuit design, a transistor is more desirable than a diode. A popular approach to make a negative transconductance transistor is to put a double-barrier quantum well structure inside a bipolar transistor or in series with a modulation-doped field-effect transistor (MODFET)³; the double-barrier quantum well structure is used as an energy filter and the well cannot be controlled directly. On the other hand, there have been considerable efforts to make a third contact to the well of a double-barrier quantum well RT diode, so that the well potential and therefore the resonant tunneling current can be controlled by this additional terminal.⁴ One of the key problems in contacting the well directly is the large base current. Another approach of making a RT transistor, as we proposed previously, is to use three closely placed nanometer gates in a MODFET to create a lateral electrostatic double-barrier quantum well.⁵ Since the gates are capacitively coupled to the quantum well, high input impedance is assured. In this letter, we report the first observation of electron resonant tunneling through energy states in a lateral double-barrier quantum well formed electrostatically by two closely placed nanometer gates in a MODFET.

The new lateral RT field-effect transistor (LARTFET) is very similar to a conventional MODFET, except that it has dual closely placed nanometer gates instead of a single gate, as shown schematically in Fig. 1. The dual gates electrostatically create double potential barriers in the channel and a quantum well in between. By controlling the gate potential, the barrier heights can be adjusted continuously.

The modulation-doped structure is grown on a semi-insulating GaAs substrate using molecular beam epitaxy (MBE) at a substrate temperature of 580 °C which is determined by pyrometer measurement. After growing a 40 nm GaAs layer, eight periods of $\text{Al}_{0.35}\text{Ga}_{0.65}\text{As}/\text{GaAs}$ superlattice (6 nm/5 nm) are grown, followed by growing a 0.5- μm -thick GaAs buffer layer. Then the following is grown: a 2.5 nm undoped $\text{Al}_{0.35}\text{Ga}_{0.65}\text{As}$ spacer layer, a 45 nm doped $\text{Al}_{0.35}\text{Ga}_{0.65}\text{As}$ layer with Si doping concentration of $2 \times 10^{18} \text{ cm}^{-3}$, and a 50 nm doped GaAs layer with Si doping concentration of $3 \times 10^{18} \text{ cm}^{-3}$. In device fabrication, a Au/Ge/Ni/Au ohmic contact is patterned by lift-off, and is annealed at 450 °C for 30 s, followed by dual argon ion implan-

tations to isolate each device area. Then a recess removes the doped GaAs cap layer from the gate area. A layer of 70 nm PMMA is spun and electron beam lithography is used to define the gates. Gate metals, Ti/Au, of 15/15 nm thickness, are evaporated and a lift-off process leaves the gates on top of the recessed gate area. Finally, Ti/Au metal contacts are patterned by a lift-off process. The LARTFETs have dual 80-nm-long gates separated by 100 nm. The channel width is $\sim 7 \mu\text{m}$. The two gates are connected to the same contact pads. In addition, conventional MODFETs with a single 80 nm gate are fabricated on the same substrate for comparison.

The dual-gate LARTFETs can be operated, at least, in three modes, as shown in Fig. 1(b). (1) Keep the source-drain voltage constant, and vary the gate voltage. The gate voltage lowers the barrier height and therefore lowers the energy states in the quantum well. Resonant tunneling results when states in the well line up with electrons at the source. (2) Keep the gate voltage fixed and vary the source-drain voltage. Similar to a vertical RT diode, the source-

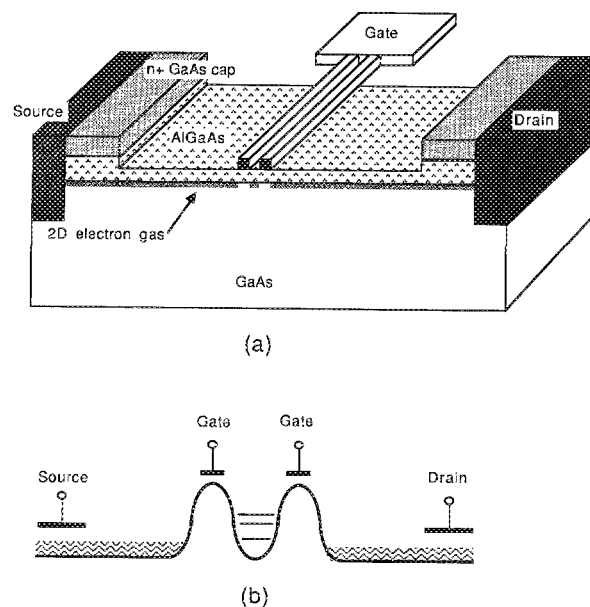


FIG. 1. (a) Schematic of a lateral resonant tunneling field-effect transistor which has dual closed placed fine finger gates instead of a single gate; (b) schematic of energy-band diagram for the device.

drain bias lowers the energy states in the quantum well, and resonant tunneling results when states in the well line up with electrons at the source. Using different fixed gate biases, one has different barrier heights, and therefore different resonant conditions. (3) A back gate can adjust the electron concentration in the channel.

At room temperature, the dual-gate LARTFET behaves as does a conventional MODFET with a maximum extrinsic transconductance of 95 mS/mm and a threshold voltage of -2.6 V. The extrinsic transconductance is limited by the source-drain series resistance.

Devices are operated at 4.2 K and without illumination in both modes 1 and 2. In operation mode 1, i.e., the gate voltage is swept and the source-drain voltage is fixed at 0.5 mV, a very smooth turn-on is observed in drain current measurement of a single 80 nm gate MODFET as shown in Fig. 2(a). However, drain current measurement of a dual 80 nm gate LARTFET exhibits a foot and a shoulder, as shown in Fig. 2(b). The shoulder is ~ 30 mV away from the threshold voltage V_T , which is the intercept of the linear extrapolation of the drain current at the V_G axis. The current-voltage (I - V) characteristics of the dual-gate LARTFET are repeatable after thermal cycling and are observed in all dual 80 nm gate LARTFETs (totally, four LARTFETs were fabricated in two different MBE wafers). It is interesting to note that although there are many quasi-bound energy states in the wide lateral double-barrier quantum well formed electrostatically, only one shoulder is observed in the current measurement. We believe this is because that the energy separations between quantum levels in the well are very small and the separation decreases continuously as the gate bias be-

comes less negative, therefore only the first resonance is observable. To get an idea of the energy separation we use a parabolic well model. Assuming that the barrier height is 50 meV and the width of the well is 200 nm, the energy separation between levels, $\Delta E = \hbar\omega = 2.4$ meV, where \hbar is the Plank's constant over 2π and ω is the frequency of the harmonic oscillator.

The conductance variation of the shoulder decreases as the source-drain voltage increases, and disappears for source-drain voltages greater than ~ 5 mV. This observation is consistent with a small energy separation, because the increase in electron temperature due to the heating caused by the source-drain bias V_{ds} is approximately $qV_{ds}/2$, and the quantum effect will not be resolved if the electron temperature is a few times higher than the energy separation of quantum states in the quantum well.

Devices are also characterized at 4.2 K in operation mode 2, i.e., the source-drain voltage is scanned and the gate voltage is fixed around the threshold voltage of the device to ensure potential barrier(s) are formed in the channel. Figure 3(a) shows that for a single 80 nm gate FET, there is only one "knee" in the I - V characteristics as expected.

Figure 3(b) shows the drain current versus the drain voltage at different gate biases for the dual-gate LARTFET. At low gate voltages, the I - V characteristics of the dual-gate LARTFET exhibit two knees instead of one and conductance oscillations, which suggest electron resonant tunneling through the lateral double-barrier quantum well. As the gate voltage becomes less negative (i.e., the barrier heights are reduced), the two knees converge, because at these gate voltages the barrier heights are too low and the quantum states cannot be resolved.

Figure 4 shows the linear plot of drain current versus drain voltage at different gate voltages for the dual-gate LARTFET. Two features can be seen: (1) the conductance oscillation peak moves towards smaller drain voltage as the gate voltage becomes less negative; (2) at a certain gate vol-

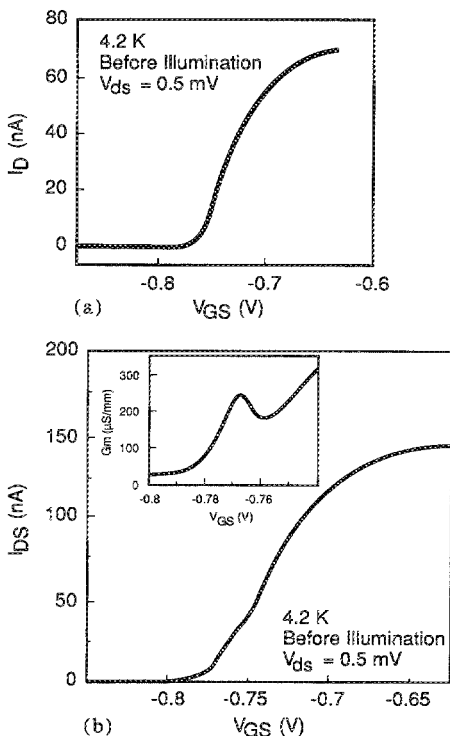


FIG. 2. Drain current vs the gate voltage at a fixed source-drain voltage of 0.5 mV at 4.2 K before illumination (a) for the single 80 nm gate MODFET exhibiting a smooth turn-on, (b) for a dual 80 nm gate LARTFET as a function of the drain voltage at a fixed source-drain voltage at 1 mV, exhibiting a foot and a shoulder.

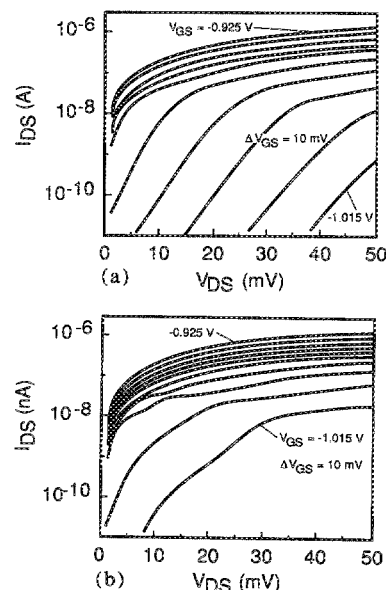


FIG. 3. Logarithmical plot of drain current vs the source-drain voltage at different gate voltages at 4.2 K (a) for a single 80 nm gate FET and (b) for a dual 80 nm gate LARTFET.

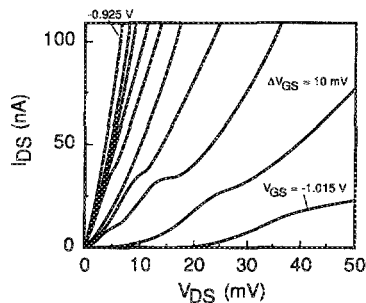


FIG. 4. Linear plot of the drain current vs the source-drain voltage at different gate biases for a dual 80 nm gate LARTFET.

age, the conductance oscillation is maximum. The first feature is due to the fact that, as the gate voltage becomes less negative, the height of the double barrier becomes smaller, lowering the energy levels in the well; therefore, less drain voltage is necessary to move the energy levels to the resonant position. The second feature can be explained as follows. If the gate voltage is less negative, the barrier height is low, and the separations of energy levels become small, reducing the conductance oscillation. If the gate voltage is very negative, both the double barriers and the bottom of the quantum well are well above the conduction-band edge at the source. In order to bring the energy levels in the well into resonance with electrons at the source, a large drain voltage is required, which in turn destroys the symmetry of the double barriers and reduces the conductance oscillation.

Devices are illuminated with a red light emitting diode at 4.2 K. It is observed that the light can partially penetrate the thin gates metal, and that the threshold voltages of the devices shift to more negative and stay there for about 1 h. Very surprisingly, new additional conductance oscillation peaks are revealed after the illumination. Figure 5(a) shows the drain current of a single 80 nm gate FET as a function of gate voltage at 0.5 meV source-drain voltage at 4.2 K after illumination. Compared with the I - V characteristics without illumination two additional negative transconductance peaks appear near the turn-on of the device. The separation of the two peaks is ~ 26 mV. Figure 5(b) shows the drain current of a dual 80 nm gate LARTFET as a function of the gate voltage at 0.5 meV source-drain voltage at 4.2 K after illumination. There are three conductance oscillation peaks. The first two near the turn-on are ~ 26 mV apart, similar to those observed in the single 80 nm gate FET. The third one, which is 31 mV after the V_T , should be the shoulder observed in the I - V characteristics of the device without illumination. It is interesting to note that the conductance variation of the shoulder becomes larger after illumination. This could be explained by the fact that photons free more electrons which were trapped outside the gate area than that under the gates. As a result, the electrostatic potential variation in the channel after the illumination is enhanced, and so is the energy separation of quantum states in the well.

It is also found that the additional peaks disappear when the source-drain voltage is larger than 12 mV. We believe that the two additional peaks are related to the trap states, which become active when photons free the trapped electrons from them. Further experiments show that when the AlGaAs spacer layer thickness is increased from 2.5 to 7 nm, the additional peaks disappear,⁶ indicating that the trap states could be the donor-related deep levels in doped

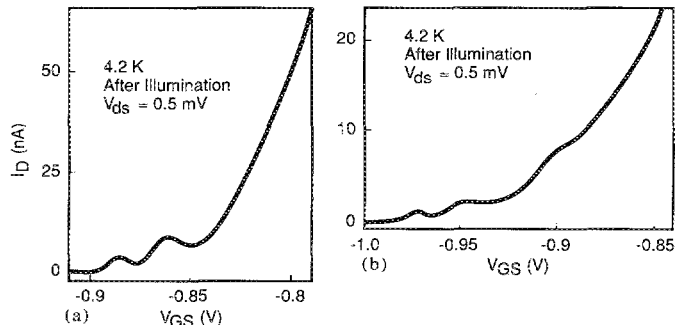


FIG. 5. Drain current measurement as a function of the gate voltage at a 0.5 meV source-drain voltage at 4.2 K after illumination (a) for a single 80 nm gate FET and (b) for a dual 80 nm gate LARTFET.

AlGaAs, which are known to have two major deep levels and can extend into GaAs.^{7,8}

In summary, we have fabricated a new lateral dual-gate resonant tunneling FET using MBE and ultrahigh-resolution electron beam lithography. At 4.2 K, without illumination, conductance oscillations are observed when either the gate voltage is scanned and the source-drain voltage is fixed below 5 mV, or the source-drain voltage is scanned and the gate voltage is fixed below the threshold voltage. We believe this is the first observation of electron resonant tunneling through a lateral double-barrier quantum well formed electrostatically. Furthermore, we observed that the trap states, probably the ionized donor-related deep levels in silicon-doped AlGaAs, can also cause negative differential conductance peaks in the current measurement.

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¹T. C. L. G. Sollner, W. D. Goodhue, P. E. Tannenwald, C. D. Parker, and D. D. Peck, *Appl. Phys. Lett.* **43**, 588 (1983).

²S. Sen, F. Capasso, A. Y. Cho, and D. Sivco, *IEEE Trans. Electron Devices*, **ED-34**, 2185 (1987).

³For example, F. Capasso and R. A. Kiehl, *J. Appl. Phys.* **58**, 1366 (1985); N. Yokoyama, I. Imamura, S. Moto, S. Hiyamizu, and H. Nishi, *Jpn. J. Appl. Phys.* **24**, L853 (1985); A. R. Bonnefoi, T. C. McGill, and R. D. Burnham, *IEEE Electron Device Lett.* **EDL-6**, 636 (1985).

⁴A. C. Seabaugh, M. A. Reed, W. R. Frensley, J. N. Randall, and J. Matyj, *Technical Digest IEDM*, 900 (1988).

⁵S. Y. Chou, J. S. Harris, Jr., and R. F. W. Pease, *Appl. Phys. Lett.* **52**, 1982 (1988).

⁶The details will be published elsewhere.

⁷H. Ohna, Y. Akatsu, T. Hashizume, and H. Hasegawa, *J. Vac. Sci. Technol.* **B 3**, 943 (1985).

⁸P. M. Mooney, T. N. Theis, and S. L. Wright, *Appl. Phys. Lett.* **53**, 2546 (1988).