

Engineering lateral quantum interference devices using electron beam lithography and molecular beam epitaxy

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Various new lateral quantum interference devices (QIDs) have been fabricated using high resolution electron beam lithography and molecular beam epitaxy. These QIDs utilize various nanometer scale electrodes to introduce electrostatic potential barriers in the electron gas at an AlGaAs/GaAs heterojunction. At low temperatures, as the electron mean free path approaches the dimensions of the gate electrode, quantum interference of the electron wave with the barriers and wells creates quasibound states that result in conductance oscillations as the gate voltage is scanned. High resolution electron beam lithography is used to define the nanometer gates, readily allowing the definition and alignment of different electrodes on the same wafer. A planar implantation isolation step is used to facilitate the liftoff of the Ti/Au gates patterned in polymethyl methacrylate (PMMA). Several novel QIDs will be described; emphasis will be on a new lateral double barrier resonant tunneling diode formed by two 80 nm gates separated by 100 nm. At 4.2 K, structure in the drain current is seen as the gate voltage is scanned for drain voltages less than 5 mV.

I. INTRODUCTION

There is currently a great deal of research into the ultimate scaling limits of transistors. Some data indicate that the minimum feature size of silicon insulated gate field effect transistors (IGFETs) cannot be reduced much below $0.1 \mu\text{m}$ due to drain induced barrier lowering.¹ These dimensions are expected to be feasible on a commercial scale in one or two decades. As a result, many investigators are currently searching for novel devices that depend on different physical principles and are operational at dimensions well below $0.1 \mu\text{m}$ thereby continuing the microelectronics revolution.

Much of this research has utilized thin (10 nm) molecular beam epitaxy (MBE) grown layers of materials with different bandgaps (often AlGaAs/GaAs) to study quantum size effects. The most notable devices have been the superlattice² and the resonant tunneling diode.³ However, MBE is a layer growth technology and the electrons are confined only perpendicular to the wafer. The quantum size effects would be enhanced if confinement occurred in all three dimensions. Furthermore, once the AlGaAs and GaAs layers are grown, the height of the potential barriers and the depth of the wells are fixed.

Bate⁴ first proposed a lateral surface superlattice that overcomes these problems. A grating or grid gate in a field effect transistor imposes a periodic potential on a heterojunction interface. The electrons at the heterojunction interface are confined in two or all three dimensions depending on whether a grating or grid gate is used. Furthermore, the periodic potential is tunable with the gate voltage. Warren *et al.*⁵ has observed conductance oscillations at 1.2 K in a Si/SiO grating gate lateral surface superlattice indicative of minibands formed by the periodic potential. Ismail *et al.*^{6,7} has observed conductance oscillations in both a grating and grid gate lateral surface superlattice in GaAs/AlGaAs.

We have fabricated several quantum interference devices (QIDs) that utilize nanometer scale electrodes to introduce electrostatic potential barriers in the electron gas at an AlGaAs/GaAs heterojunction (Fig. 1). At low tempera-

tures, as the electron mean free path approaches the dimensions of the gate electrode, quantum interference of the electron wave with the barriers and wells creates quasibound states that result in conductance oscillations as the gate voltage is scanned. Once device has two 80 nm gate electrodes separated by 100 nm [Fig. 2(a)]; both gates are at the same potential. This device is merely a dual gate modulation doped field effect transistor (MODFET) with very small, closely spaced gates. This electrode configuration introduces a double-barrier, single-well potential at the heterojunction interface. The barrier heights and hence the position of the quasibound states can be controlled with the gate potential

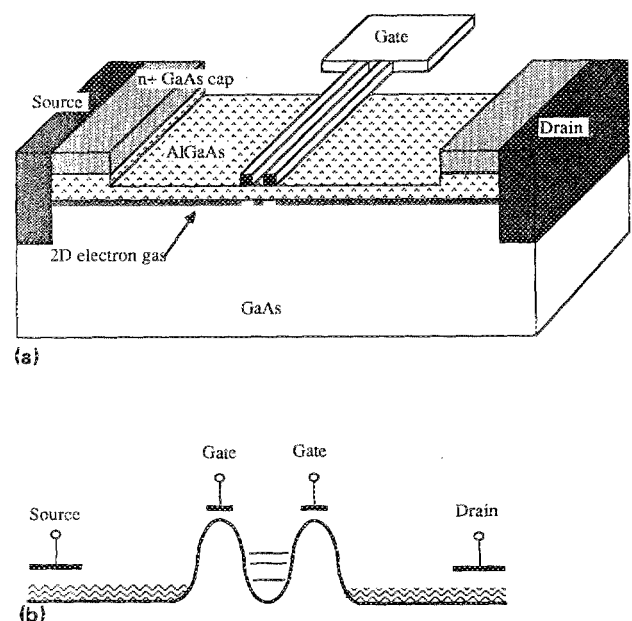


FIG. 1. (a) Schematic of a lateral QID with two nanometer scale closely spaced gate electrodes. This gate configuration introduces two electrostatic barriers and one potential well at the heterojunction interface. (b) Schematic of the energy band diagram at the heterojunction interface showing the quasibound states formed in the central well.

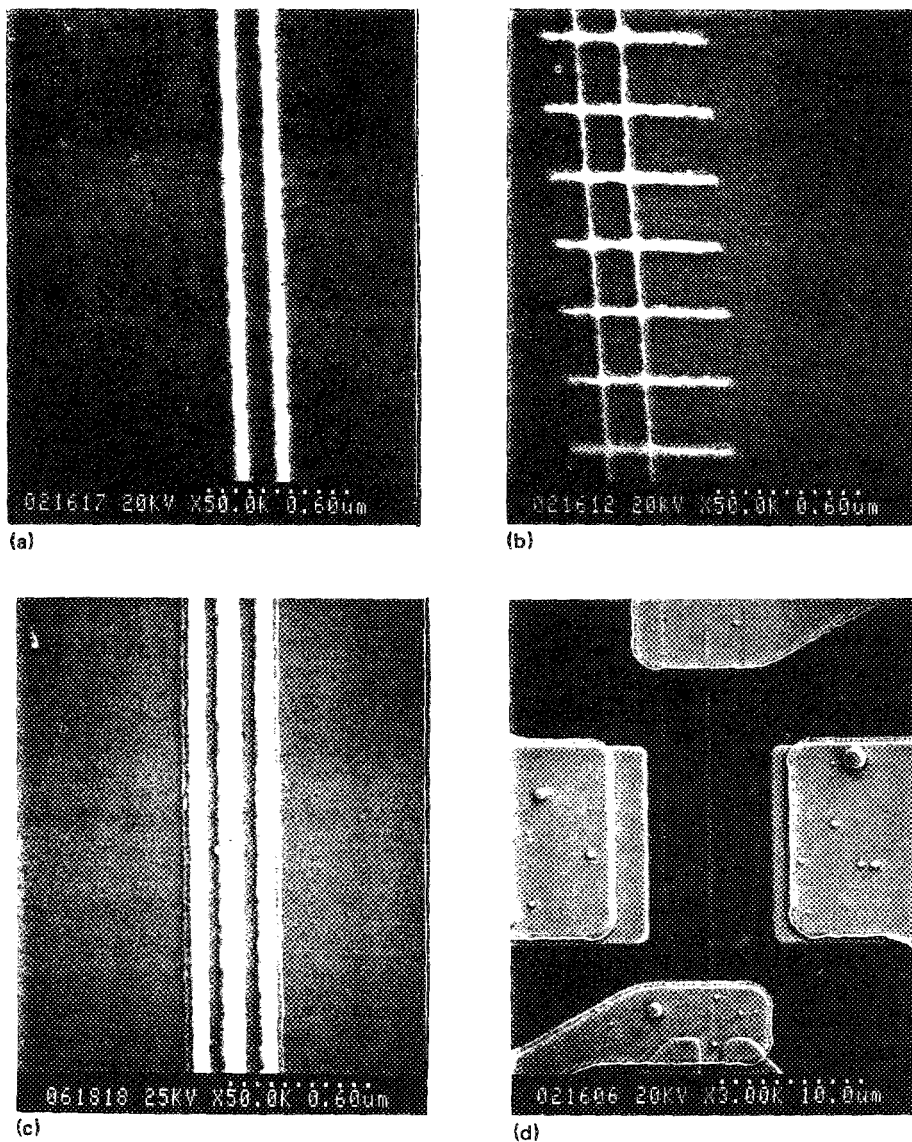


FIG. 2. Scanning electron micrographs of a (a) dual gate QID, (b) railway gate QID, (c) triple gate QID where the central gate is used to independently control the depth of the central well, and (d) low-magnification view showing the broad gate recess, and the ohmic and gate contacts.

forming a tunable, lateral resonant tunneling transistor.

Another device differs from the one just described in that railway ties have been added to the two nanometer finger gates or rails [Fig. 2(b)]. This additional confinement prevents the electrons from scattering along the rails in the central well, resulting in stronger conductance oscillations. Kroemer⁸ has pointed out that a lack of confinement and hence quantization of energy levels in the dimensions perpendicular to the direction of tunneling can significantly reduce the strength of conductance oscillations because electrons with sufficient lateral momentum can scatter to higher quasibound states. The width of the ties and rails is 50 nm; the spacings between the ties and between the two rails are 230 and 150 nm respectively. The ties are 0.75 μm long and extend beyond the two rails. The potential at the heterojunction interface creates an array of one-dimensional electron wires on both sides of three-dimensionally confined electron boxes.

A third device, first proposed by Chou *et al.*⁹ has three gate electrodes [Fig. 2(c)]. The outer two gates control the

amplitude of the potential barriers as in the first device discussed above. The central gate is connected to a different gate pad allowing independent control of the depth of the central well.

II. FABRICATION

The devices were fabricated on a semi-insulating substrate with MBE layers grown at 580 $^{\circ}\text{C}$ (Fig. 3). A 40 nm GaAs layer is first grown followed by eight periods of a $\text{Al}_{0.35}\text{Ga}_{0.65}\text{As}/\text{GaAs}$ superlattice (6 nm/5 nm). A 500 nm buffer layer is then grown, followed by a 2.5 nm undoped $\text{Al}_{0.35}\text{Ga}_{0.65}\text{As}$ spacer layer, a 45 nm $\text{Al}_{0.35}\text{Ga}_{0.65}\text{As}$ layer doped with Si at $2 \times 10^{18} \text{ cm}^{-3}$, and finally a 50 nm n^+ GaAs cap layer. The sheet resistance for this wafer was 250 Ω/sq . More recently we have fabricated devices on a wafer with a thicker $\text{Al}_{0.35}\text{Ga}_{0.65}\text{As}$ spacer layer, 6 nm, and a very thin n^+ GaAs cap, 10 nm. The thicker spacer layer increases the electron mobility at the heterojunction interface by reducing the Coulombic scattering. The cap layer is so thin that the

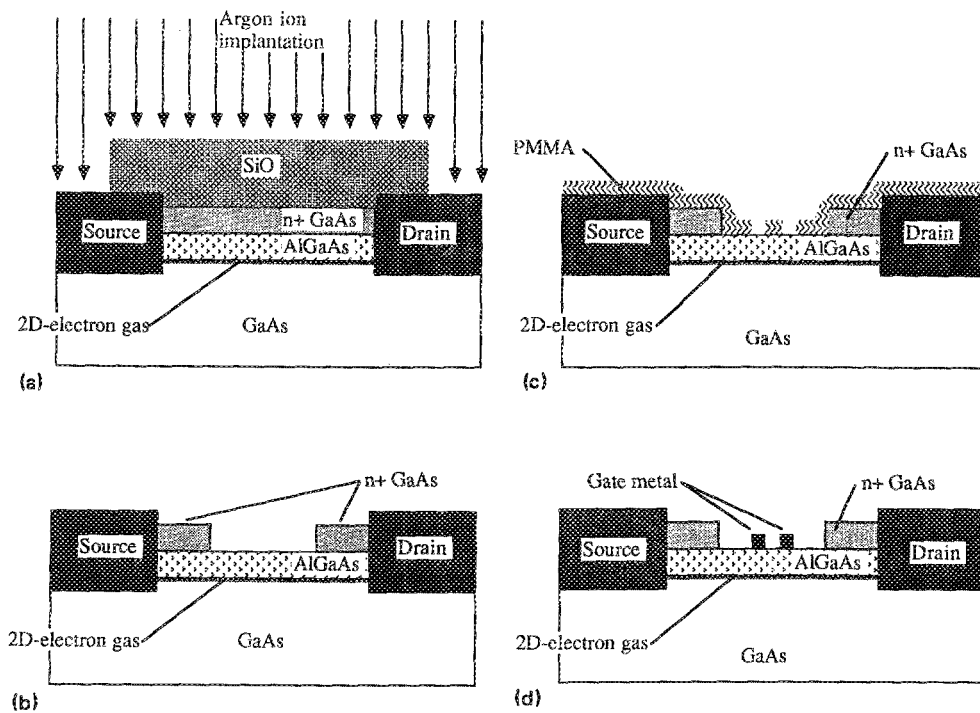


FIG. 3. QID fabrication sequence: (a) argon ion implantation for device isolation, (b) broad gate recess (necessary only when a thick n^+ GaAs cap is present), (c) PMMA patterned with high resolution electron beam lithography, and (d) gate metallization after liftoff. Ohmic contact formation and final contact metallization are not shown.

gate electrodes can be placed directly on top avoiding the wide gate recess and simplifying the fabrication sequence. Furthermore, to avoid the collapse of the I - V current characteristic at 4.2 K due to DX centers, the doped $\text{Al}_{0.35}\text{Ga}_{0.65}\text{As}$ was replaced with five periods of a superlattice where only the GaAs is doped; one period is GaAs(0.5 nm, undoped)/GaAs(2.8 nm, $3 \times 10^{15} \text{ cm}^{-3}$ with Si)/GaAs(0.8 nm, undoped)/ $\text{Al}_{0.35}\text{Ga}_{0.65}\text{As}$ (3.5 nm, undoped). The sheet resistance for this wafer was $2000 \Omega/\text{sq}$.

Optical lithography was used to define the ohmic contacts, the active regions, the wide gate recess when included in the process, and the final metallization. An undercut resist profile suitable for liftoff was obtained by soaking the optical resist in chlorobenzene before exposure. The mask set was the set used previously for the fabrication of metal semiconductor field effect transistors (MESFETs) and MODFETs with gate lengths down to 60 nm.¹⁰ In addition to various test structures, this mask set has an array of devices with source drain spacings ranging from 1 to 10 μm . All active regions were 7 μm wide. Each device has two gate contacts on either side of the active region; this feature is necessary for lateral QIDs that have two nanometer scale gate electrodes at different potentials.

The ohmic contact metallization was 40 nm of Au, 10 nm of Ge, 12.5 nm of Ni, and 150 nm of Au deposited sequentially with e -beam evaporation. This metallization was rapid thermal annealed at 450 $^\circ\text{C}$ for 30 s in a forming gas atmosphere. The contact resistance for the wafer with the thick cap layer was $0.2 \Omega \text{ mm}$. As expected, the wafer with the thin cap layer had a much higher contact resistance of $2.5 \Omega \text{ mm}$. This relatively high contact resistance in the latter case reduces the extrinsic transconductance but is not particularly important for these QIDs because the conductance oscillations occur for a drain current on the order of 10 nA.

The devices were then isolated with a dual argon im-

plantation masked by 600 nm of plasma enhanced chemical vapor deposited (PECVD) SiO_x . The two implant energies were 50 and 130 keV; the dose for each implant was optimized to $1.5 \times 10^{12} \text{ cm}^{-2}$ (Fig. 4). This combination successfully disordered the n^+ cap layer as well as the heterojunction interface resulting in an isolation resistance greater than $10^7 \Omega$ between devices at room temperature (480 μm device separation). Planar implantation isolation was used because of the difficulty of fabricating continuous nanometer scale gate electrodes over the mesa edges left by wet etching isolation.

For the wafers with the thick (50 nm) n^+ GaAs cap layer, a broad gate recess was necessary. The recess was defined using a readily available optical mask originally designed for the definition of large gate electrodes. Typically, devices were fabricated with a 10 μm source drain space and a 5 μm

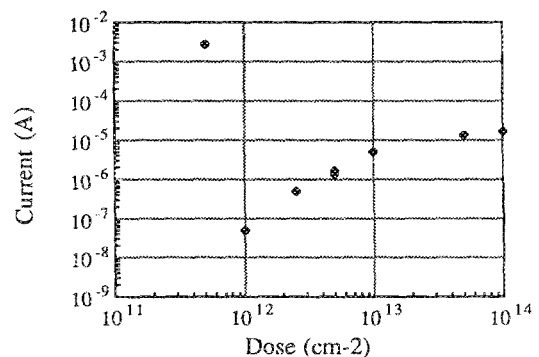


FIG. 4. The room temperature leakage current at 1 V between devices (480 μm separation) as a function of argon ion implant dose. Each dose is actually implanted twice, once at 50 keV to disorder the n^+ cap and once at 130 keV to disorder the heterojunction interface.

long recess. A selective wet etch was used, 1:200 $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2$, that stops at the surface of the AlGaAs.

The gate fabrication was done with high resolution e -beam lithography using a custom e -beam system that has been described in detail previously.¹¹ The principle features of this column are a commercial tungsten filament thermionic emitter operating at 40 kV and three magnetic lenses that provide a demagnification of about $10\,000\times$. Beam blanking is accomplished with electrostatic blanking plates in the first magnetic lens. Scanning of the e -beam is achieved with double deflection magnetic scan coils located in the upper polepiece of the third lens. The scan field can be varied from $0.25\times 0.25\ \mu\text{m}$ to $66\times 66\ \mu\text{m}$. The pattern generator used in this work is a custom raster scan system that sweeps the beam continuously in the x direction and steps the beam digitally in the y direction.

The third or objective lens was carefully designed to minimize the lens aberrations and to allow large samples to be written upon. The unusual feature of this type of lens is that the lower polepiece has no bore and the sample sits inside the lens.¹¹ There are several advantages of this configuration. The absence of a final bore makes the alignment of the lower polepiece much less critical. It is then easy to temporarily remove the lower polepiece to place a relatively large sample in the lens. The current objective lens has a 4 mm bore in the upper polepiece and a 5 mm gap, and can accommodate 3 in. wafers. The position of the sample is controlled by two orthogonal micrometers that provide 13.5 and 17 mm of traverse in the x and y directions, respectively. Finally, the short focal possible with this design results in low spherical and chromatic aberration coefficients. With a typical lens excitation of 3000 A turns and a beam potential of 40 kV, the focal length is 2.1 mm; the spherical and chromatic aberration coefficients are both about 1.5 mm. For registration and focusing, two silicon solar cells are mounted on the tip of the upper polepiece detecting backscattered electrons.¹² The probe diameter is less than 5 nm for beam currents under 5 pA.

The nanometer gate electrodes were written in 70 nm thick PMMA. The resist was spin cast from a 2% solution of 950 K PMMA in chlorobenzene. The spin speed was 8000 rpm for 30 s to minimize resist nonuniformity. The resist was prebaked for 4 h at 175 °C. After e -beam exposure, the PMMA was developed in 3:7 cellosolve:methanol followed by a methanol rise. The gate electrode was formed by liftoff of e -beam evaporated TiAu (15:15 nm). Finally, large source gate and drain contact pads were formed by optical lithography and e -beam evaporation and liftoff of TiAu. The devices were then cleaved and bonded into cans for testing.

III. RESULTS

The I - V characterization of these devices is extensively discussed elsewhere.^{13,14} Here, we will briefly review some of the results for the dual gate QID. At room temperature, this device behaved as a standard MODFET with a peak extrinsic transconductance of 95 S/m and threshold voltage of -2.6 V. In order to be able to observe the conductance oscillations due to electron resonant tunneling through the quasibound states, thermal broadening and energy broaden-

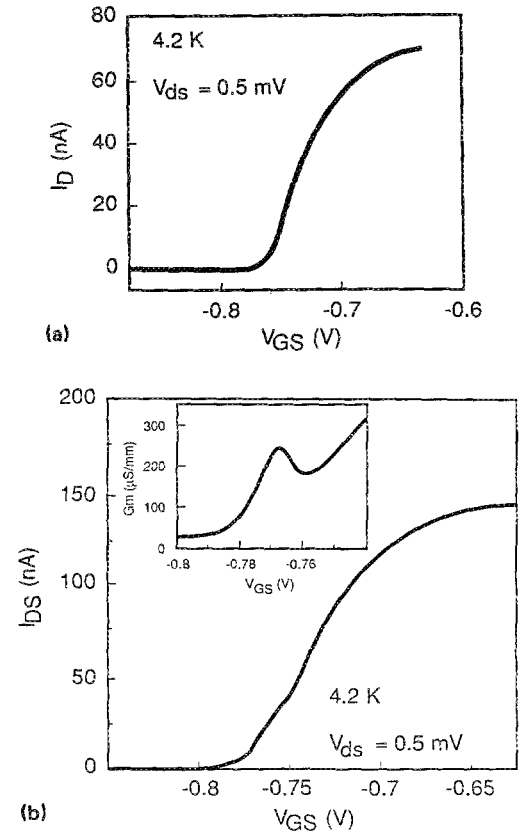


FIG. 5. The drain current vs the gate voltage at a fixed drain voltage of 0.5 mV at 4.2 K for (a) the single 80 nm gate control device exhibiting a smooth turn-on and (b) the dual 80 nm gate QID exhibiting a conductance oscillation.

ing must be less than the separation of the quasibound states requiring that the devices be cooled to a few degrees Kelvin. At 4.2 K the drain current of the QID and a control device with a single 80 nm gate were measured with a lock-in amplifier as the gate voltage was slowly scanned (Fig. 5). The amplitude of the drain voltage was 0.5 meV. Unlike the control device which had a smooth turn-on, a single oscillation in the drain current is clearly visible for the dual gate QID. This structure in the drain current is repeatable after thermal cycling and is present in all dual gate QIDs we fabricated (four have been fabricated on two different wafers). The conductance oscillation gradually disappears as the drain voltage is raised to 5 mV because the drain bias is an additional source of electron heating. This value is roughly consistent with our estimate, 2 meV, for the separation of the quasibound states.

IV. CONCLUSIONS

In summary, we have fabricated several lateral QIDs by using nanometer scale gate electrodes to form electrostatic barriers and wells at a GaAs/AlGaAs heterostructure interface. Conductance oscillations are observed in the drain source current at 4.2 K as the gate voltage is scanned. This structure is indicative of electron resonant tunneling through the quasibound states formed by the particular configuration of barriers and wells.

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