Fabrication of 70 nm channel length polymer organic thin-film transistors using nanoimprint lithography

Michael D. Austin[a] and Stephen Y. Chou
NanoStructure Laboratory, Department of Electrical Engineering, Princeton University, Princeton, New Jersey 08540

(Received 10 July 2002; accepted 9 October 2002)

We report on the fabrication of short-channel polymer organic thin-film transistors (OTFTs) using nanoimprint lithography. Currently, there is significant interest in OTFTs due to their potential application in inexpensive, large-area electronics. However, polymer carrier mobilities are typically poor, and thus to increase the OTFT drive current per unit area, there is a need for short-channel devices. We have fabricated working devices with channel lengths from 1 μm down to 70 nm with high yields. The performance of these devices was studied as the channel length was reduced. We find that drive current density increases as expected, while the on/off current ratio remains 10^4. However, at short-channel lengths, OTFTs no longer saturate due to space charge limiting current effects. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1526457]

Currently, there is much interest in using soluble semiconducting polymers as the active material for organic thin-film transistors (OTFTs) in large-area applications that require inexpensive, low-temperature processing such as displays[1] and disposable circuits.[2] Polymer films can be applied at room temperature by spin coating or casting, and thus are ideally suited for such applications. However, carrier mobilities in semiconducting polymers are lower than those of either amorphous silicon, the traditional active material of thin-film transistors (TFTs), or crystalline pentacene.[3] Although much progress has been made developing semiconducting polymer devices with higher mobilities,[4] device performance can be improved by reducing the channel length. Previous attempts at fabricating short-channel devices included wells,[5] electron-beam lithography (EBL),[6] phase shift masks,[7] and cold welding metal transfer.[8] However, in order to realize the low-cost advantage of using polymers, the lithography process must be capable of high-throughput, inexpensive, submicron patterning, qualities that previous techniques have yet to fully demonstrate. Here, we report on the fabrication of short-channel devices using nanoimprint lithography (NIL), a process that allows for large-area, parallel, arbitrarily complex patterning with sub-10-nm resolution.[9]

NIL is a simple patterning process whereby a mold is pressed into an imprint polymer. On a single silicon dioxide mold 20 devices were patterned by EBL with channel lengths varying from 1 μm down to 70 nm. The 70 nm device mold shown in Fig. 1 has 56 fingers, a W/L ratio of over 3000, and a height of 70 nm.

The OTFT devices were fabricated on a heavily doped n-type silicon substrate with 5 nm of thermally grown oxide that served as a backside gate. The gold source and drain contacts were patterned by NIL on the substrate, and then the semiconducting polymer was coated directly over the entire sample. We used a well-studied p-type semiconducting polymer, poly(3-hexylthiophene) (P3HT), which currently has the highest reported polymer carrier mobility of 0.1 $cm^2/V\,s$.[4] The P3HT was purchased from Aldrich Chemical and was used without further processing. It has a head-to-tail regioregularity better than 98.5%, which has been shown to give better carrier mobilities than the regiorandom configuration.[10]

The NIL process, described previously in detail,[9] starts with a 100 nm film of imprint polymer on the substrate. The NIL mold was pressed into the polymer and the entire assembly was heated above the polymer glass temperature so that the polymer flowed and conformed to the topology of the

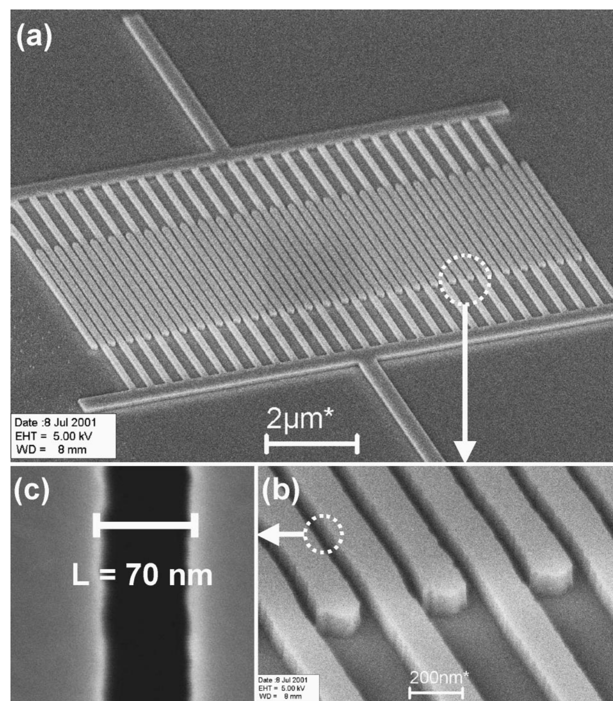

FIG. 1. NIL mold includes 20 devices varying in channel length from 1 μm down to 70 nm. (a) shows a scanning electron microscopy picture of a 70 nm OTFT device with a 4 μm channel width, 56 source and drain interdigitated fingers, and a W/L ratio greater than 3000. The mold is fabricated from a silicon dioxide substrate, and is 70 nm in height. (b) and (c) show successive image magnifications revealing the uniform 70 nm channel length between the source and drain figures with very little variation in the critical dimension over the entire active region.

[a]Electronic mail: mdaustin@princeton.edu

 © 2002 American Institute of Physics
Downloaded 14 May 2003 to 128.112.49.61. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/aplo/aplcr.jsp

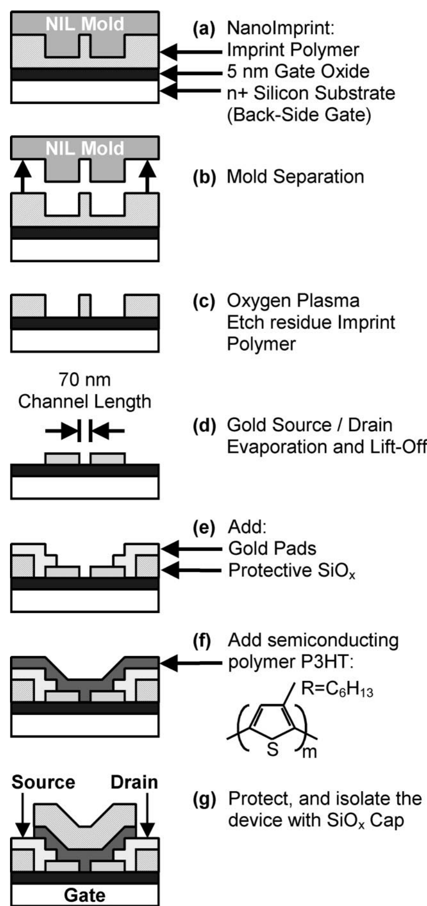

FIG. 2. (a)–(g) summarize the processing steps used to fabricate our OTFTs: (a) The NIL mold was pressed into the imprint polymer, (b) and then separated. (c) An oxygen plasma RIE removed the residue polymer. (d) Gold source and drain terminals were then evaporated. After lift-off, the channel length was 70 nm. (e) Large gold pads were added for $I-V$ measurements with a layer of SiO_x to protect the gate oxide from measurement probe damage. (f) The *p*-type semiconducting polymer P3HT was applied over the entire substrate. (g) To protect the P3HT from exposure to moisture and oxygen and to electrically isolate the devices, a SiO_x cap was evaporated over the polymer and patterned with photolithography.

mold, as shown in Fig. 2(a). An oxygen plasma reactive ion etch (RIE) was used to remove the residual imprint polymer, allowing the gate oxide to be exposed. The metal for the source and drain contacts (4 nm chrome adhesion layer and 20 nm gold) was then deposited by electron-beam evaporation. Finally, lift-off in warm acetone finished the NIL process leaving the substrate patterned with 20 OTFT devices, as shown in Fig. 2(d). The mold used to fabricate these devices was used in over 50 imprints, and showed no indication of process performance degradation, including defects, mold damage, or loss of critical dimension control.

After patterning the source and drain contacts, a 100 nm film of silicon dioxide was deposited around the active region by electron-beam evaporation, as shown in Fig. 2(e). Large gold contact pads were then added to allow for wire bonding or probing for device current–voltage measurements. Without the protective SiO_x the measurement probes would often break through the 5 nm gate oxide, destroying the device.

The samples were then cleaned with acetone, placed in a dry nitrogen glovebox, and baked at 140 °C for at least 1 h to remove any moisture. A film of hexamethyldisilazane (HMDS) was spin coated over the substrate, followed by the application of the semiconducting polymer P3HT, as shown in Fig. 2(f). We attempted both spin coating and casting of the P3HT solution onto the sample substrate, as casting has been shown to give better carrier mobilities.[10] For spin coating, a 2.2 gm/l solution was applied at 3000 rpm for 45 s, resulting in a uniform 50 nm film. For casting, the sample was repeatedly dipped in a 0.14 gm/l solution, resulting in a film thickness of 5–10 nm. The spin-coated samples typically achieved mobilities of 10^{-5} $cm^2/V\,s$, while the casted devices were as high as 10^{-3} $cm^2/V\,s$. The difference in mobilities observed between the spin-coated samples and the dipped samples may be due to the associated difference in film thickness. The dependence of mobility on film thickness needs further study.

There is a decrease in performance of the devices within 2–4 h of P3HT exposure to atmosphere due to rapid doping of the polymer film by oxidation.[4] In addition, since the P3HT covers the entire surface of the substrate, a gate oxide failure during current–voltage measurement on any one device will short the other devices on the chip. To protect the polymer, and electrically isolate the devices, further processing was necessary. After the P3HT was allowed to dry in the glovebox, the samples were moved immediately into a vacuum chamber, resulting in brief exposure to atmosphere for 1–2 min. In the vacuum chamber, 150 nm of silicon dioxide was evaporated directly over the polymer. A photoresist island was then patterned over the active region of the device and used as an etch mask. A CHF_3 RIE plasma was then used to remove the surrounding SiO_x and P3HT, leaving the devices protected from atmosphere and isolated from each other, as shown in Fig. 2(g). Device yields were better than 95% for the 70 nm devices, and 98% for the others.

All device measurements were performed in atmosphere with an HP 4145B analyzer. Figure 3 shows typical plots of the drain current density for 1000, 200, and 70 nm channel length devices. The P3HT in these devices was applied by casting. The 1000 nm channel devices demonstrate standard field-effect transistor (FET) characteristics with a FET mobility in saturation of 8×10^{-4} $cm^2/V\,s$. The drain current density increases as the channel length is reduced while the on/off ratio remains 10^4; however, this control is weakened as the drain voltage is increased. It should be noted that due to the thin 5 nm gate oxide, a gate leakage tunneling current typically of the order of 10 pA adds error to the measurement of the "off" current. It can be seen in Fig. 3(c) that the 70 nm OTFT devices are no longer capable of standard FET saturation, and instead demonstrate a continuous growth in drain current with drain voltage. The inability to saturate is widely observed in short-channel OTFT devices,[6,11–13] although the reported mechanisms for this phenomenon vary.

Figure 4 shows the drain current density of the fabricated devices as a function of the drain voltage normalized by their respective channel lengths. Before the devices enter saturation, the longer channel length devices show a higher current density for a given V_d/L, thus clearly suggesting that the parasitic contact resistances dominate the drain current characteristics.[14] The dominating effects of the contact resistance are more clearly observed in the inset of Fig. 4, where the devices supply the same current density at low V_d, regardless of channel length, as a function of V_d. However, as

Downloaded 14 May 2003 to 128.112.49.61. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/aplo/aplcr.jsp

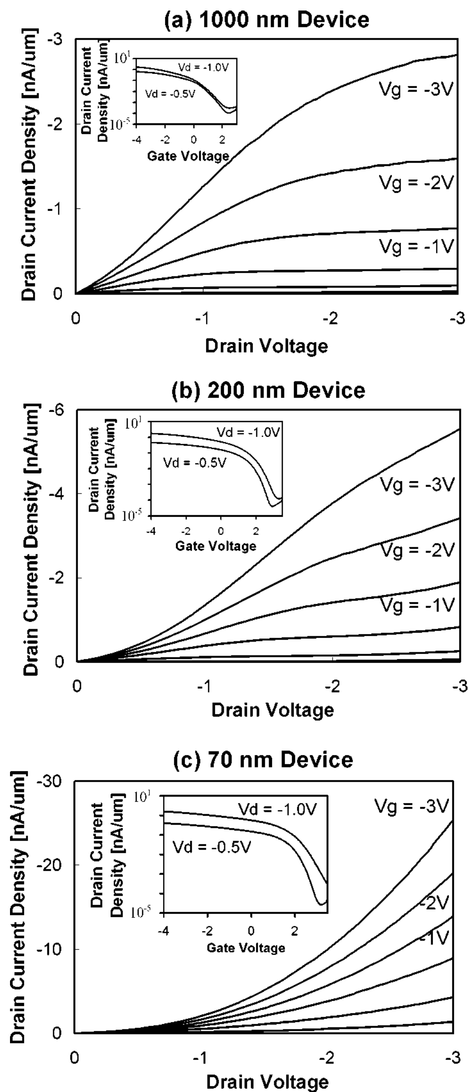

FIG. 3. Typical performance of polymer OTFT devices with channel lengths of (a) 1000 nm, (b) 200 nm, and (c) 70 nm. The drain current density (I_d/W) vs drain voltage (V_d) curves show the devices working in accumulation mode, with gate voltage from 2 to -3 V in steps of -1 V. The insets show the transfer characteristics of the devices with a log plot of the drain current density as a function of the gate voltage (V_g) for drain voltages of -0.5 V and -1.0 V.

the devices enter into saturation, devices with different channel lengths produce similar current densities as a function of V_d/L, which strongly suggests that the drain current is determined by the bulk characteristics of the polymer and not the contacts.

We believe a phenomenon similar to the metal–oxide–semiconductor FET (MOSFET) short-channel "punch-through" effect[15] caused by space charge limiting current (SCLC) is preventing saturation. Here, space charge does not originate from depletion regions, as our devices operate in accumulation mode, but rather from a collection of carrier charge in the channel due to the poor polymer mobility and the high current densities associated with shorter channel lengths. Conductivity experiments of semiconducting polymers at high electric fields[16] reveal the characteristic SCLC relationship $I_d \propto V_d^n$, where n depends on the trap concentration and is typically greater than or equal to 2. For our 70 nm OTFT devices, Fig. 4 clearly shows two regimes. At low V_d/L the conductivity is dominated by contact resistance,

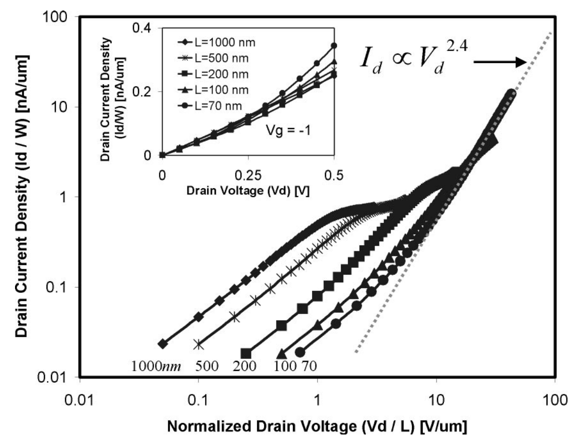

FIG. 4. Output characteristics of the devices with respective channel lengths of 1000, 500, 200, 100, and 70 nm. Shown is the drain current density (I_d/W) as a function of the drain voltage normalized by the device's respective channel length (V_d/L) on a log–log graph. The inset shows the current density (I_d/W) as a function of the drain voltage (V_d) on a linear graph at low drain voltages. The gate voltage for all curves is -1 V.

and thus n is equal to 1. At higher V_d/L, the 70 nm devices move into a different regime where n is approximately 2.4, suggesting that SCLC effects are dominating the drain current characteristics of the short-channel devices.

A comparison of mobilities for various channel lengths is difficult as the short-channel devices do not saturate, and thus extrapolation of a FET mobility is of questionable validity. The 1000 nm device FET saturation mobility of 8×10^{-4} cm^2/V s is well below that of previously recorded devices using P3HT.[4] Possible explanations include the brief exposure of P3HT to atmosphere, the use of bottom source/drain gold contacts instead of top contacts, and the increased relative effects of parasitic contact resistance with reduction in channel length.

This work is supported in part by DARPA. This work was presented as a talk by the authors at the 46th Electron, Ion, and Photon Beam Technology and NanoFabrication Conference 29 May (2002).

[1] H. E. A. Huitema, G. H. Gelinck, J. B. P. H. van der Putten, K. E. Kuijk, C. M. Hart, E. Cantatone, P. T. Herwig, A. J. J. M. van Breeman, and D. M. de Leeuw, Nature (London) **414**, 599 (2001).
[2] C. Drury, C. Mutsaers, C. Hart, M. Matters, and D. de Leeuw, Appl. Phys. Lett. **73**, 108 (1998).
[3] J. H. Schon, C. Kloc, and B. Batlogg, Org. Electron. **1**, 57 (2000).
[4] H. Sirringhaus, N. Tessler, and R. H. Friend, Science **280**, 1741 (1998).
[5] F. Garnier, R. Hajlaoui, and M. Kassmi, Appl. Phys. Lett. **73**, 1721 (1998).
[6] J. Collet, O. Tharaud, A. Chapoton, and D. Vuillaume, Appl. Phys. Lett. **76**, 1941 (2000).
[7] J. A. Rogers, A. Dodabalapur, Z. Bao, and H. Katz, Appl. Phys. Lett. **75**, 1010 (1999).
[8] C. Kim, M. Shtein, and S. Forrest, Appl. Phys. Lett. **80**, 4051 (2002).
[9] S. Y. Chou, P. R. Krauss, and P. J. Renstrom, Science **272**, 85 (1996).
[10] H. Sirringhaus, P. J. Brown, R. H. Friend, M. M. Nielsen, K. Bechgaard, B. M. W. Langeveld-Voss, A. J. H. Spiering, R. A. J. Janssen, E. W. Meijer, P. Herwid, and D. M. de Leeuw, Nature (London) **401**, 685 (1999).
[11] J. H. Schon and B. Batlogg, J. Appl. Phys. **89**, 336 (2001).
[12] L. Torsi, A. Dodabalapur, and H. Katz, J. Appl. Phys. **78**, 1088 (1995).
[13] L. Torsi, A. Dodabalapur, L. J. Rothberg, A. W. P. Fung, and H. E. Katz, Phys. Rev. B **57**, 2271 (1998).
[14] R. A. Street and S. Salleo, Appl. Phys. Lett. **81**, 2887 (2002).
[15] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. (Wiley, New York, 1981), p. 478.
[16] P. W. M. Blom, M. J. M. de Jong, and J. J. M. Vleggaar, Appl. Phys. Lett. **68**, 3308 (1996).

Downloaded 14 May 2003 to 128.112.49.61. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/aplo/aplcr.jsp