

## Room-temperature Si single-electron memory fabricated by nanoimprint lithography

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We report the design, fabrication, and characterization of room-temperature Si single-electron memories using nanoimprint lithography (NIL). The devices consist of a narrow channel metal–oxide–semiconductor field-effect transistor and a sub-10-nm storage dot, which is located between the channel and the gate. The memories operate at room temperature by charging and discharging one electron in or out of the dot. The charge retention time is up to two days. NIL is shown to be tailored for nanodevice fabrication. By using NIL as a nanolithography tool, the single-electron memory is more feasible for mass production. © 2003 American Institute of Physics.

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As transistors continue to shrink according to Moore's law, single-electron effects are becoming significant in many device structures. The devices utilizing those effects, such as single-electron memory (SEME), have a number of attractive and unique properties such as ultra-low-power consumption, ultrahigh density, and quantized threshold voltage shift. SEME working at room temperature is also considered to be a promising candidate for the future generation of flash memories.<sup>1–4</sup> To make SEME work at room temperature, the storage node must be smaller than 10 nm to guarantee that the quantized energy level spacing is larger than the thermal energy.<sup>5</sup> Previously, Si SEME fabricated using electron-beam lithography (EBL) was reported.<sup>2</sup> However, EBL has low throughput and high cost, making it impractical for mass production. Other approaches have been used to meet the fabrication challenges, such as using grown Si dots or isolated nanocrystal Si as storage dots.<sup>1,4</sup> But the multidot nature and the random location of those dots lead to a large fluctuation of the device performance. Therefore, they are unsuitable for large-scale integration.

Here, we report the design, fabrication, and characterization of room-temperature Si single-electron memories fabricated using nanoimprint lithography (NIL). The devices consist of a narrow channel metal–oxide–semiconductor field-effect transistor and a 10-nm-size storage dot embedded between the channel and gate (Fig. 1). The channel layer, which requires sub-10-nm resolution, is defined using NIL, and the floating dot is formed and self-aligned with the narrowest part of the channel to give the stored electron maximum screening ability, and no additional lithography is needed for the dot. The memory operating at room temperature by charging a single electron into or out of the storage dot was observed. NIL is shown to be tailored for nanodevice fabrication.<sup>6</sup> In addition, the high throughput, low cost, and good fidelity of NIL make SEME more feasible for large-scale integration and mass production.

There are two major parts in the fabrication process: mold fabrication and device fabrication. In fabricating NIL molds, a master mold was fabricated first using EBL and

reactive ion etching (RIE). Next, the master mold was duplicated into several Si daughter molds using the NIL process. Then, we oxidized each daughter mold at 850 °C in dry O<sub>2</sub> and etched SiO<sub>2</sub> in HF to shrink the mold feature size. The oxidation and etching process may be repeated to achieve the required feature sizes. The mold is used in the NIL process to define the channel layer. The device fabrication began with a silicon-on-insulator substrate, and the top Si layer was thinned to 35 nm thick. First, a 2.4-nm-thick tunneling oxide was thermally grown in diluted O<sub>2</sub>, and a 13 nm polysilicon was deposited by low-pressure chemical vapor deposition. Second, the Si layer and the polysilicon layer were patterned using NIL and RIE etching. Figure 2 shows a scanning-electron microscope image of the patterned channel and floating polylayer. Third, a 13.6 nm gate oxide was thermally grown at 850 °C in dry O<sub>2</sub>, and followed by a 33 nm SiO<sub>2</sub> plasma enhanced chemical vapor deposition. The samples were annealed at 850 °C in N<sub>2</sub> to improve the SiO<sub>2</sub> quality. Finally, a 3- $\mu$ m-long polysilicon gate that covered the floating dot and part of the channel was deposited and patterned. After source/drain implantation, dopant activation, final contact, and sintering, the memories were fabricated.

Note that during gate oxidation, since SiO<sub>2</sub> grows faster in the thin poly-Si layer, the two “necks” of the poly-Si layer were totally oxidized, leaving an isolated quantum dot formed in the floating poly-Si layer, while the underneath channel was still continuous. In this way, the floating dot was

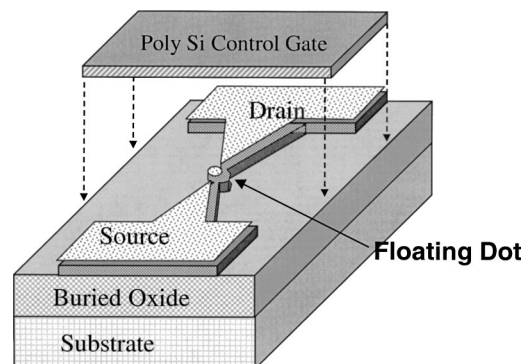


FIG. 1. Schematic of single-electron memory made by NIL.

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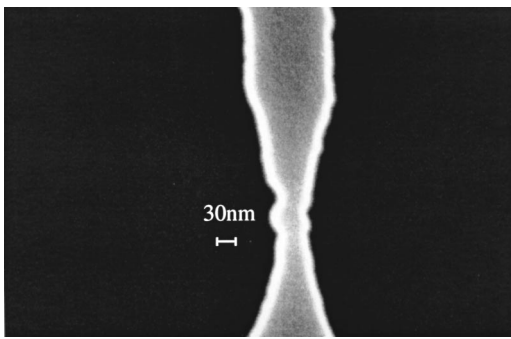
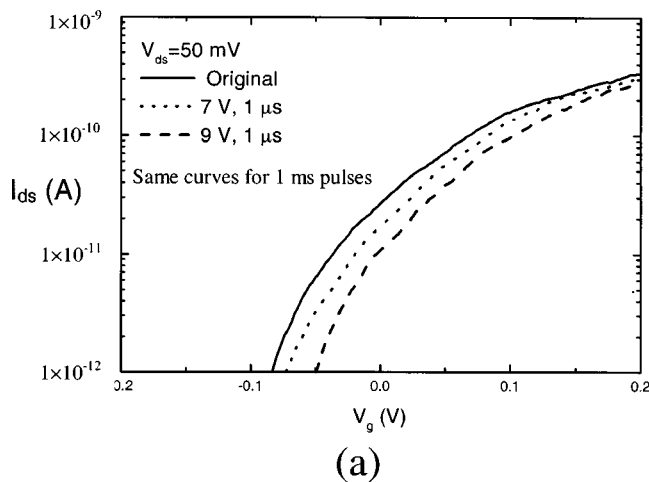


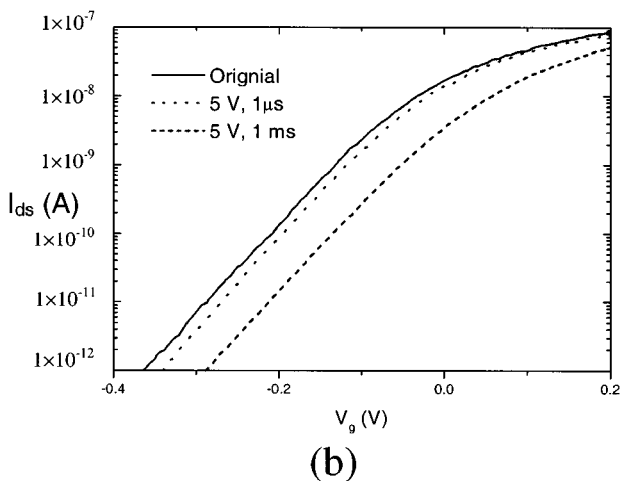
FIG. 2. Imprinted channel and floating poly-Si layer. After gate oxidation, an isolated quantum dot will form in the floating poly, while the channel is still connected. The quantum dot will be the storage node.

formed and self-aligned with the narrowest part of the channel.

The devices were characterized at room temperature using a two-step process. First, a voltage pulse was applied to the control gate while the source was grounded and the drain held at a 50 mV bias. Second, the drain current was measured as a function of control gate voltage ( $I-V$ ). A simple



(a)



(b)

FIG. 3. (a) Drain current vs control gate voltage curves of one single-electron memory measured at room temperature with drain bias of 50 mV. The curves indicate single-electron memory effects. By applying a 7 V, 1  $\mu$ s pulse, the  $I-V$  curve moved right to the second curve. By applying a 9 V, 1  $\mu$ s pulse, the  $I-V$  curve moved right to the third curve. Varying the pulse duration from 1  $\mu$ s to 1 ms has no effect on the measurements. (b) The memory with continuous floating poly-Si and no quantum dot has traditional voltage shifts depending on the voltage time duration.

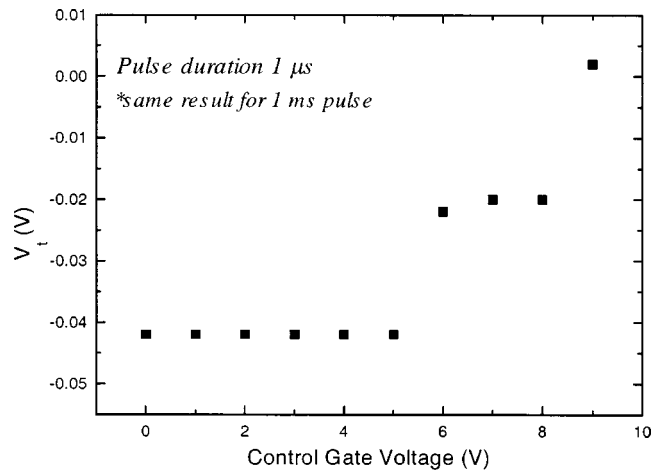


FIG. 4. Threshold voltage of one single-electron memory vs the pulse voltage applied to the control gate before the measurements. The threshold voltage shifted two steps at 6 and 9 V. The shift of each step is about 22 mV. Varying the pulse length from 1  $\mu$ s to 1 ms has no effect on the measurements. One more electron was charged into the storage node at each threshold voltage shift step.

switch circuit was used to allow the measurement within 2 s after the charging process.

The devices demonstrated a single-electron memory effect at room temperature. As shown in Fig. 3(a), when the charging voltage varies continuously from 1 to 9 V, the threshold voltage shifted discretely with an increment of 22 mV at 6 and 9 V. The charging of the dot seems to be independent of the charging time, when the charging pulse length varied from 1  $\mu$ s to 1 ms (Fig. 4). The discrete increase in the threshold voltage indicates a single-electron charging into the floating dot at 6 V and two electrons at 9 V, respectively. Due to the Coulomb blockade, after one electron is charged into the floating dot, the next electron will need a higher charging voltage to conquer the additional Coulomb energy. After each additional electron is charged, the threshold voltage would shift a certain amount due to the screening of the electron. This led to the discrete threshold voltage shift, a staircase relationship between the charging voltage, and the threshold voltage in Fig. 4. We did not observe any quantized or charging-time-independent threshold voltage

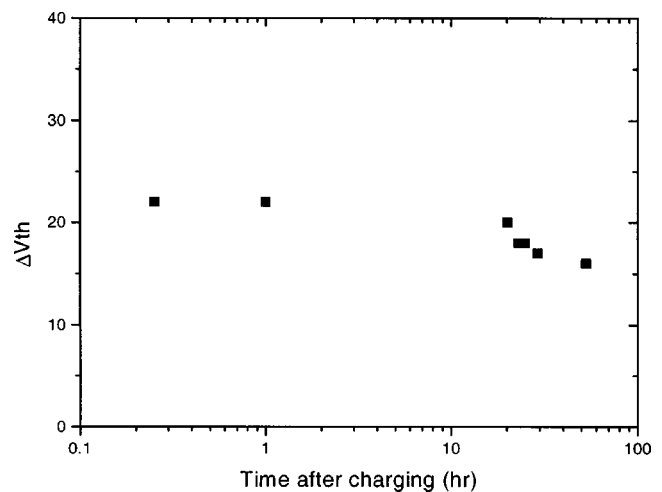


FIG. 5. Memory can keep the threshold voltage shift up to two days. However, after one day, the shifted threshold voltage started to shift back. We believe it was due to leaking somewhere in the poly-Si layer away from the floating dot.

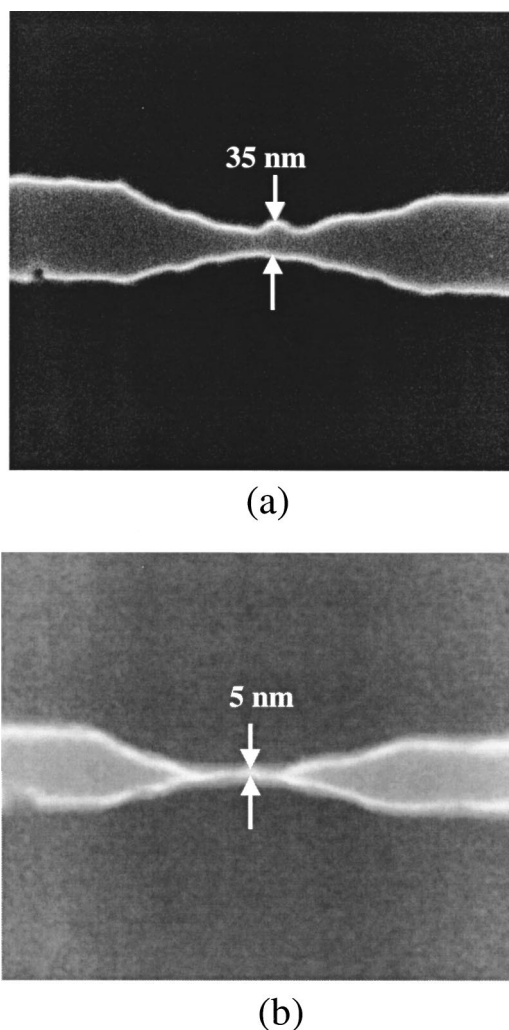


FIG. 6. (a) SEM picture of one Si quantum dot mold made by nanoimprint lithography and RIE etching. Dot size is about 35 nm. (b) After oxidation and HF etching the dot size reduced to 5 nm.

shifts in the devices, which have a continuous wide floating poly and a wide channel [Fig. 3(b)].

We did charge retention time measurements. We found that after an electron was charged to a quantum dot, the charge could store there for more than two days, as shown in Fig. 5. Compared to former work, which was only a few minutes to a few hours,<sup>2</sup> the improvement in retention charging comes from the improved SiO<sub>2</sub> quality. The tunneling oxide was grown in the very early stage of the fabrication before any patterning, which may have helped to give better SiO<sub>2</sub> quality.

The expected threshold voltage shifts due to single-electron charging can be calculated from the device dimensions. The device, whose characteristics are shown in Figs. 3 and 4, has a disk-shape floating dot with a 8 nm diam and a 2 nm thickness, which is located on top of the narrowest part of the channel. The narrowest part of the channel is about 20 nm wide. The device dimension was estimated from scanning-electron microscope (SEM) pictures and the oxidation rate. The width is smaller than the single-electron Debye screening length ( $\sim 70$  nm) in order to give one electron enough screening ability. The threshold voltage shift due to the screening of one electron inside the floating dot is given by  $\Delta V \approx e/(C_{fg} + C_{cg})$ ,<sup>1</sup> where  $C_{fg}$  is the capacitance be-

tween the floating dot and the control gate, and  $C_{cg}$  the capacitance between the channel and the control gate. In our devices,  $C_{cg}$  is much larger than  $C_{fg}$ . The  $C_{cg}$  can be estimated from the single-electron Debye screening length and the device dimension. The calculated values,  $C_{cg}$  at 5.9 aF and  $e/C_{cg}$  at 27 mV, are consistent with the experiment. For the devices we measured, the threshold shifts spread from 18 to 23 mV. The variation was due to the feature size variation on the mold. The mold was made by EBL, and we intentionally varied the doses for different sites on the mold. The total capacitance of the dot is about 0.7 aF and is calculated from the size of the floating dot and a tunneling oxide thickness of 2.4 nm. That makes the Coulomb blockage energy spacing, i.e.,  $e^2/C_{total}$ ,<sup>7</sup> about 0.2 eV. It is much larger than the thermal energy at room temperature (26 meV), which is why the memory works at room temperature.

It should be pointed out that the discrete threshold shift is not due to the traps. Threshold shift due to the traps will not give the staircase relationship shown in Fig. 4 and will have a charging time dependency.<sup>2</sup>

NIL is tailored for nanodevices fabrication, which requires patterning relatively complex structure with high resolution and good repeatability. Besides sub-10-nm resolution,<sup>8</sup> high throughput, low cost, and capability of submicron alignment over large area,<sup>9</sup> the freedom of combining with other techniques in mold fabrication can achieve more complex structure and better resolution. For example, in the SEME mold fabrication by using the imprint-oxidation-etching technique described in this letter, 5 nm size quantum dot mold was achieved (Fig. 6). The self-limiting oxidation effect<sup>10</sup> was utilized to reach the goal. Using other lithography tools, it is very difficult to directly pattern such a small feature with good repeatability. In contrast, NIL gives us the freedom to combine many fabrication techniques together in mold fabrication, and no matter how difficult it is to fabricate the mold, as long as the mold is made, the NIL patterning will have low cost, high throughput, and good fidelity.

In summary, we designed and fabricated Si single-electron memory using NIL. The memories work at room temperature by utilizing the single-electron charging effect. NIL is shown to be tailored for nanodevices and makes our SEME fabrication process more feasible for mass production.

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