RESONANT TUNNELING OF 1-DIMENSIONAL ELECTRONS ACROSS AN ARRAY OF 3-DIMENSIONALLY CONFINED POTENTIAL WELLS

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A lateral resonant tunneling field effect transistor has been fabricated with a gate electrode in the form of a railway such that the two rails form a lateral double barrier potential at the GaAs/AlGaAs interface. The ties confine the electrons in the third dimension forming an array of potential boxes or three dimensionally confined potential wells. The width of the ties and rails is 50nm; the spacings between the ties and between the two rails are 230nm and 150nm respectively. The ties are 750nm long and extend beyond the the two rails forming one dimensional wires on either side. Conductance oscillations are observed in the drain current at 4.2K as the gate voltage is scanned. Comparison with devices with a solid gate, and with a monorail gate with ties fabricated on the same wafer suggest that these conductance oscillations are electron resonant tunneling from one dimensional wires through the quasi-bound states of the three dimensionally confined potential wells. Comparison with a device with a two rail gate without ties (previously published) indicates that additional confinement due to the ties enhances the strength of the conductance oscillations.

The level of integration for Si insulated gate field effect transistors (IGFET) has dramatically increased over the last three decades through an increase in die size and decrease in minimum feature size. Commercial state of the art 4 Mb DRAMs have a minimum feature size of about 1.0μm. The practical limit of about 0.1μm for IGFET channel lengths primarily due to subthreshold drain current is expected to be reached in another one or two decades[1]. As a result, many investigators are currently searching for novel devices that depend on different physical principles and are operational at dimensions well below 0.1μm.

Much of this research has utilized thin (10nm) MBE grown layers of materials with different bandgaps (often AlGaAs/GaAs) to study quantum size effects. The most notable devices have been the superlattice[2] and the resonant tunneling diode[3]. MBE, however is primarily a layer growth technology and the electrons are confined only perpendicular to the wafer. The quantum size effects would be enhanced if confinement occurred in all three dimensions. Furthermore, once the AlGaAs and GaAs layers are grown, the height of the potential barriers and the depth of the wells are fixed.

R.T. Bate[4] first proposed a lateral surface superlattice that overcomes these problems. A grating or grid gate in a field effect transistor imposes a periodic potential on a heterojunction interface. The electrons at the heterojunction interface are confined in 2 or all 3 dimensions depending on whether a grating or grid gate is used. Furthermore, the periodic potential is tunable with the gate voltage. Warren, et al[5] has observed conductance oscillations at 1.2K in a Si/SiO grating gate lateral surface superlattice indicative of mini-bands formed by the periodic potential. Ismail, et al[6,7] has observed conductance oscillations in both a grating and grid gate lateral surface superlattice in GaAs/AlGaAs.

Chou, et al[8] first proposed a lateral double barrier resonant tunneling field effect transistor employing three nanometer finger gates in an otherwise conventional modulation doped field effect transistor (MODFET). The outer two gates control the amplitude of the potential barriers and the central gate controls the depth of the central well. Recently we have reported the observation at 4.2K of electron resonant tunneling in a similar device[9]. This device has only two nanometer finger gates, each 80nm wide separated by 100nm. This electrode introduces a double barrier single well potential at the GaAs/AlGaAs interface. Unlike the device previously proposed, the depth of the well cannot be controlled independently of the barrier heights. Conductance oscillations at 4.2K were observed in the drain current as the gate voltage or the drain voltage was scanned indicative of tunneling through the quasi-bound states in the central well.

In this letter we report on the observation of conductance oscillations in a railway gate device. This device differs from the one just described in that railway ties have been added to the two nanometer finger gates (fig. 1). This additional confinement prevents the electrons from scattering along the rails in the central well resulting in stronger conductance oscillations. Kroemer[10] has pointed out that a lack of confinement and hence quantization of energy levels in the dimensions perpendicular to the direction of tunneling can significantly reduce the strength of conductance oscillations because electrons with sufficient lateral momentum can scatter to higher quasi-bound states. The width of the ties and rails is 50nm; the

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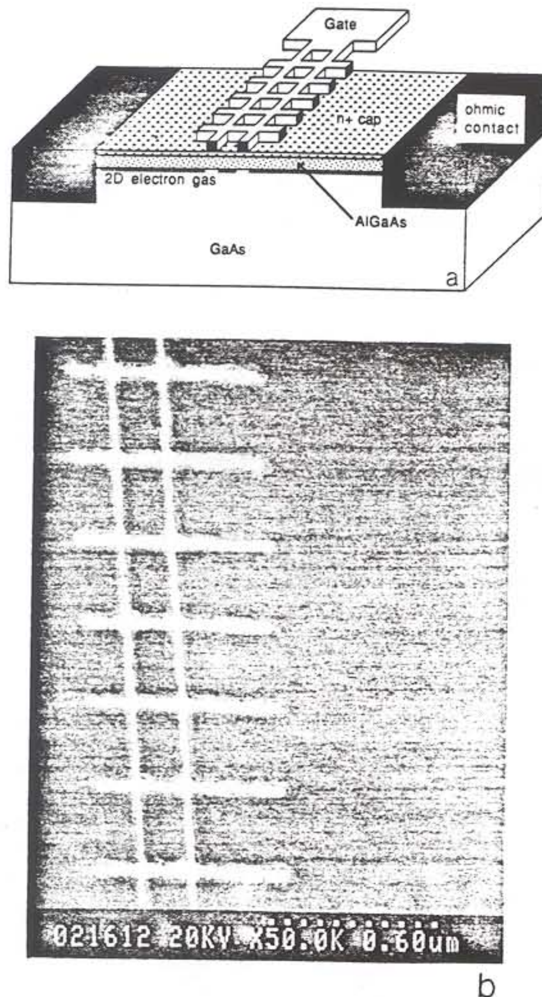

Fig. 1 (a) Schematic of a railway gate lateral resonant tunneling field effect transistor, (b) Scanning electron micrograph of the gate electrode. The width of the ties and rails is 50nm; the spacings between the ties and between the two rails are 230nm and 150nm respectively. The ties are 750nm long.

spacings between the ties and between the two rails are 230nm and 150nm respectively. The ties are 0.75μm long and extend beyond the two rails. The potential at the heterojunction interface creates an array of one dimensional electron wires on both sides of three dimensionally confined electron boxes.

The devices were fabricated on a semi-insulating substrate with four MBE layers: a 400nm undoped GaAs layer, a 6nm undoped AlGaAs buffer layer, a 38nm AlGaAs layer doped with Si, and a 10nm n+ GaAs cap. Optical lithography was used to define the ohmic contacts, the active regions, and the final metallization. The ohmic contact metallization was 40nm of Au, 10nm of Ge, 12.5nm of Ni, and 150nm of Au deposited sequentially with e-beam evaporation. This metallization was rapid thermal annealed at 450C for 30 sec. in a forming gas atmosphere. The devices were then isolated with an argon ion implantation masked by PECVD SiO. The gate fabrication was done with high resolution electron beam lithography. This custom electron beam system has been described previously[11]. The nanometer gate electrodes were written in 70nm thick PMMA. The PMMA was developed in 3:7 cellosolve:methanol and the gate electrode was formed by liftoff of e-beam evaporated TiAu (15nm:15nm). Note that no broad recess was necessary for the gate electrode because the n+ cap layer was very thin thereby simplifying the device fabrication. Finally, large source, gate and drain contact pads were formed by e-beam evaporation and liftoff of TiAu.

At room temperature the devices behaved as standard MODFETs with a peak extrinsic transconductance of 28S/m and threshold voltage of -1.0V. The extrinsic transconductance was limited by the high ohmic contact resistance due to the very thin n+ cap layer. At 4.2K the peak extrinsic transconductance increased to 38S/m with a threshold voltage of -0.95V. No current voltage (I-V) collapse was observed. At 4.2K the drain current was measured with a lock-in amplifier as the gate voltage was slowly scanned. As the gate voltage becomes less negative, the height of the barriers become smaller thereby changing the position and separation of the quasi-bound states. As these states pass through the fixed Fermi level, conductance oscillations should occur. A couple of conditions must be met before the quasi-bound states can be resolved. First, the electron mean free path must be longer than the double barrier. Typical electron mobilities at a GaAs/AlGaAs interface at 4.2K indicate an electron mean free path on the order of a micrometer. This is equivalent to the condition that the energy broadening, $\hbar/\tau$, where τ is the scattering time and $\hbar$ is the reduced Planck's constant, must be less than the separation of the quasi-bound states. For a 4.2K mobility of 250,000 $cm^2/(Vs)$, the energy broadening should be only 0.07meV. Second, thermal broadening must be less than the separation of the quasi-bound states. At 4.2K thermal broadening is 0.36meV. Assuming a 200nm parabolic well and a barrier height of 50meV, the separation of quasi-bound states in the central well can be estimated to be 3.3meV, substantially greater than the thermal broadening or the energy broadening

All measurements were made in the dark. Structure is clearly visible in the drain current and transconductance for the ladder gate device (fig. 2) unlike the solid gate control device which has a smooth turn on characteristic (fig. 3). The drain voltage for these measurements was 0.5meV (amplitude). The conductance oscillations in the drain current gradually disappear as the drain voltage is raised to 50mV (amplitude). This is expected because the drain voltage heats the electrons and serves as another source of broadening. Since the devices have a 10μm source drain spacing, approximately 5meV of heating occurs for each mean free path length of 1μm. This value is roughly consistent with the estimated separation of the quasi-bound states. This drain voltage is an order of magnitude larger than the drain voltage necessary to eliminate the conductance oscillations in the device with the two rail gate without ties (ref. 9) indicating that confinement of the

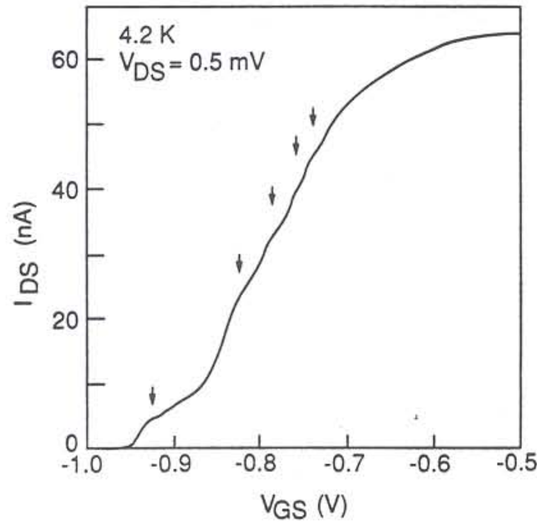

Fig. 2 The drain current vs. the gate voltage with a drain bias of 0.5mV at 4.2K for the railway gate lateral resonant tunneling field effect transistor. The arrows indicate the approximate location of the conductance oscillations.

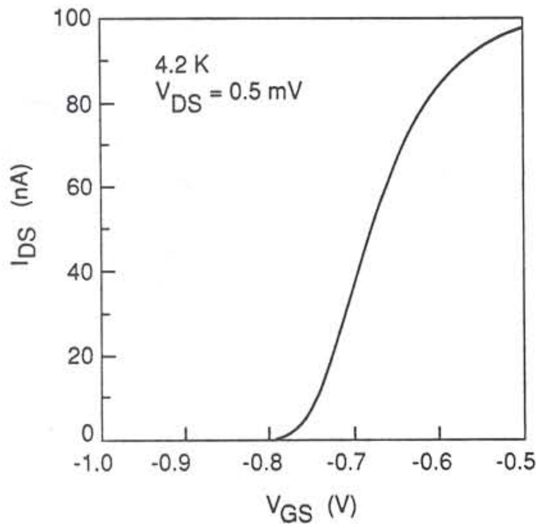

Fig. 3 The drain current vs. gate voltage with drain bias of 0.5mV at 4.2K for a solid gate control device (Lg = 0.9μm). No conductance oscillations are present.

electrons perpendicular to the direction of tunneling does enhance the strength of the conductance oscillations. The periodicity of the conductance oscillations becomes smaller as the gate voltage becomes less negative. This is consistent with the fact that increasing the gate voltage decreases the barrier heights and decreases the separation of the quasi-bound states. The separation of the states is roughly proportional to the square root of the depth of the well.

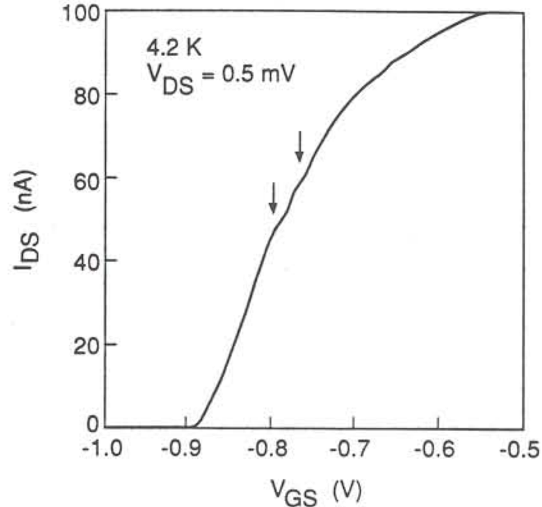

Fig. 4 The drain current vs. the gate voltage with a drain bias of 0.5mV at 4.2K for the device with a monorail gate and ties.

Because the railway ties extend beyond the two rails, the central electron box has a one-dimensional electron wire on each side. Some of the structure in figure 1 may be due to the variation of the density of states in the one-dimensional wires. In order to separate these effects, we fabricated additional devices with a monorail gate and railway ties. This device has no central electron box; it only has one dimensional wires on both sides of the monorail. At 4.2K, the drain current of this device does not display conductance oscillations near the device turn-on (fig. 4) where the railway gate device had the strongest oscillations. It is interesting that a couple of weak conductance oscillations are visible at a large drain current, but further study is necessary to determine their origin. In conclusion, we believe that the conductance oscillations seen in the drain current of the railway gate device are evidence of resonant tunneling of one dimensional electrons through a three dimensionally confined electron box. Furthermore, the additional confinement due to the railway ties does appear to enhance the strength of the conductance oscillations.

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